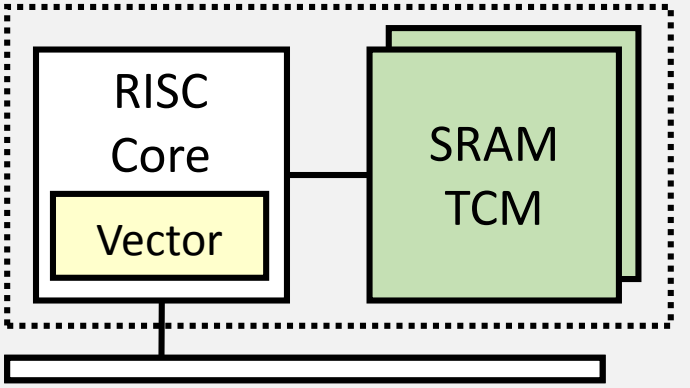
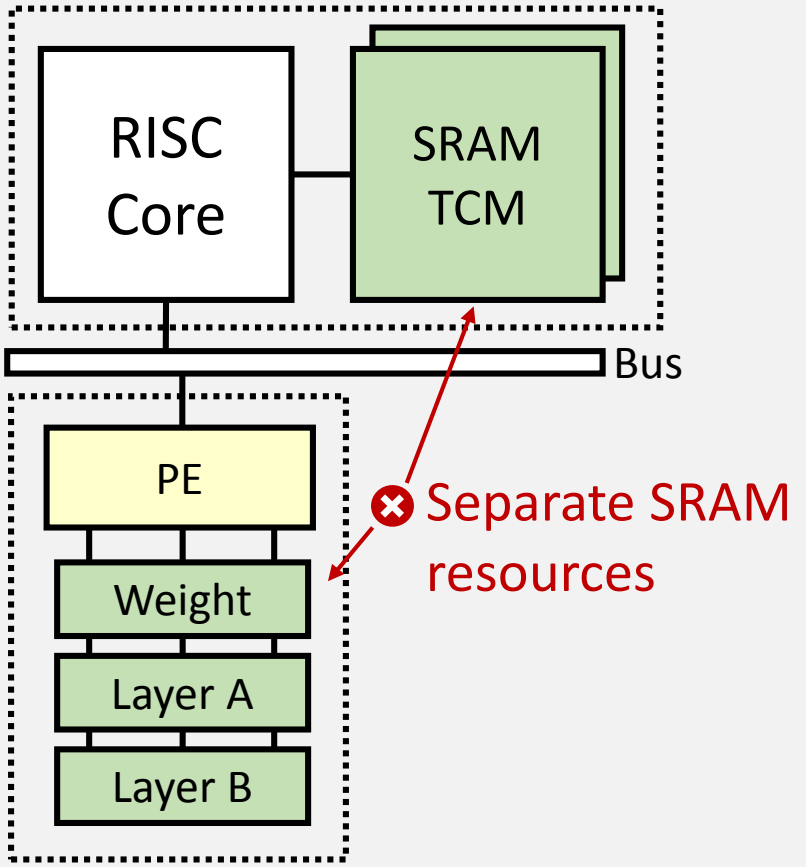
Accelerator Architecture		Physically	
		Loosely Coupled	Tightly Coupled
Logically	Tightly Coupled		VP
	Loosely Coupled	PE	PTLL-BNN

VP: Vector Processor

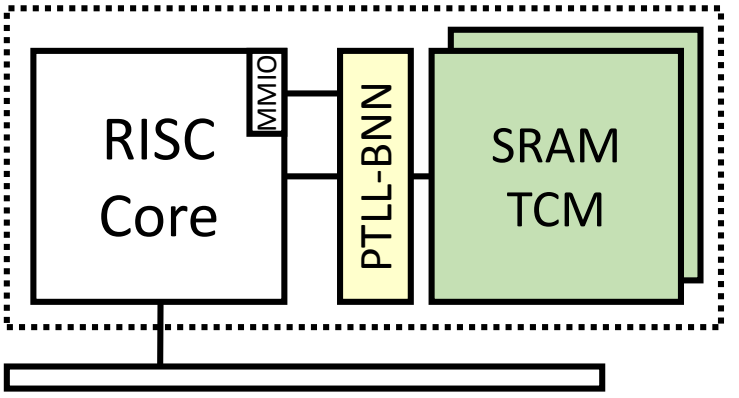


- Significant pipeline changes
- Significant compiler changes
- Load/store/loop overheads

PE: Peripheral Engine



★ PTLL-BNN (This Work)



- Shared SRAM resources
- Near-memory computing
  → no load/store/loop overhead
- SRAM and MMIO interfaces
  → no pipeline change
  → no compiler change