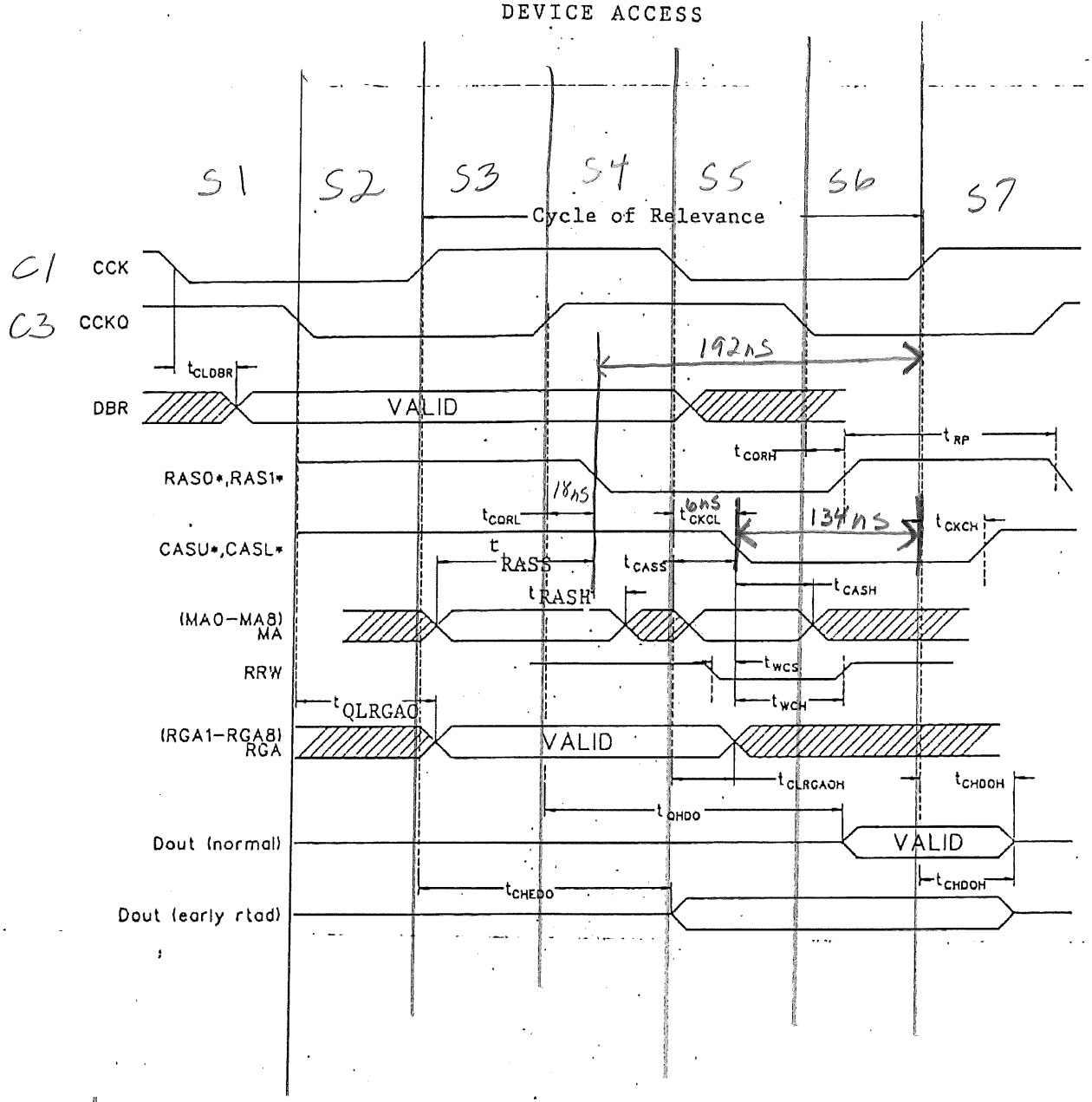
Each State ≈ 70ns

FIGURE 5

DEVICE ACCESS



t_{CORL} = 18ns MAX

Time from assertion of RAS to falling edge S6 = 192nS

commodore		TITLE IC, N-CHANNEL-HMOS DMA CONTROLLER (PAL) "FAT AGNUS" 8371	
SIZE A	DRAWING NO. 318071	REV A	SCALE / SHEET 12 OF