Corrected TTR Example

The goal is to correctly configure **UPA1 (bit 9) and UPA0 (bit 8)** for different memory regions.

💡 Memory Region Mapping

Memory Range	Access Type	UPA1 (Bit 9)	UPA0 (Bit 8)	Correct Value
0x10000000 - 0x1FFFFFFF	Instruction Fetch	**1**	**0**	$10000200
0x20000000 - 0x2FFFFFFF	Data Access	**0**	**1**	$20000100

💻 MC68040 Corrected Assembly Code

assembly

```
  MOVE.L  #$10000200, ITT0    ; Instruction TTR0 -> Base 0x10000000, UPA1=1 (bit 9), UPA0=0 (bit 8)

  MOVE.L  #$20000100, DTT0    ; Data TTR0 -> Base 0x20000000, UPA1=0 (bit 9), UPA0=1 (bit 8)


  MOVEC   TCR,D0          ; Read Translation Control Register

  ORI.L   #$00000001,D0     ; Enable MMU (User and Supervisor)

  MOVEC   D0,TCR          ; Write back to enable MMU

  NOP                 ; Small delay for MMU activation

  NOP

  MOVE.L  #$12345678, (0x20000000)  ; Store data at 0x20000000 (UPA1=0, UPA0=1)

  MOVE.L  (0x20000000), D1        ; Load data back (Verify UPA1=0, UPA0=1)

  JSR    0x10000000       ; Jump to code at 0x10000000 (UPA1=1, UPA0=0 should be active)

  STOP    #$2700          ; Halt processor (Supervisor mode)
```

🔍 Explanation

1. **Configure ITT0 (Instruction Transparent Translation Register 0)**
    - Maps instruction fetches from 0x10000000 - 0x1FFFFFFF
    - **UPA1 = 1 (Bit 9), UPA0 = 0 (Bit 8)**
    - **Correct value:** $10000200 ✅
2. **Configure DTT0 (Data Transparent Translation Register 0)**
    - Maps data accesses from 0x20000000 - 0x2FFFFFFF
    - **UPA1 = 0 (Bit 9), UPA0 = 1 (Bit 8)**
    - **Correct value:** $20000100 ✅
3. **Enable MMU**
    - Read **Translation Control Register (TCR)**
    - Set bit 0 ($00000001) to enable MMU
    - Write it back
4. **Perform Data Access**
    - Store and load from **0x20000000** to verify UPA1=0, UPA0=1.
5. **Perform Instruction Fetch**
    - JSR 0x10000000 jumps to 0x10000000, where **UPA1=1, UPA0=0 should be active**.

⚡ Notes

- This version **correctly sets UPA1 and UPA0** by using **bits 9 and 8**.
- **TTRs are the simplest way** to set these bits without needing a full MMU page table.
- If the MMU is **disabled**, UPA signals will default to 0.