數位電路設計 (Digital Circuit Design)

Lab2：組合電路之 HDL 模組撰寫與測試

(Writing and Testing the HDL Modules of Combinational Circuits)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉組合電路的設計原理，以 **gate-level modeling**、**dataflow modeling**、**behavioral modeling** 等不同方式撰寫其 HDL 電路模組，並撰寫測試模組。我們以二進位加/減法器及 Excess-3 加法器作為設計實例。

The main purpose of this Lab Unit is to be familiar with the design of Combinational Circuits. Please write their HDL circuit modules by gate-level modeling, dataflow modeling, and behavioral modeling, and write the testbench for these circuit modules. We take binary adder/subtractor and Excess-3 adder for practice.

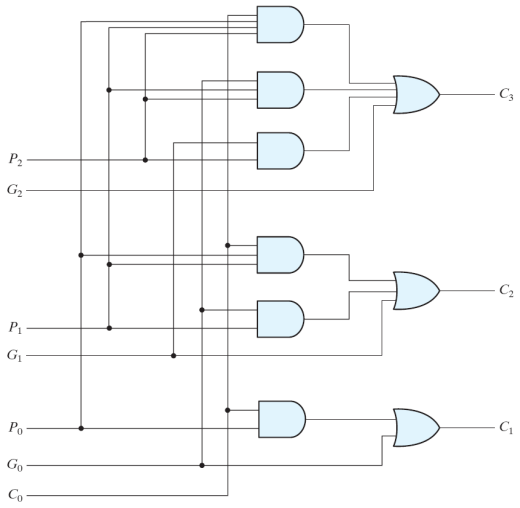
2. 撰寫 HDL 電路模組與測試模組 (Design of the HDL Circuit Modules and Testbench)

A. 前看進位加法器與前看借位減法器之設計 (Design of Carry Lookahead Adder, CLA, and Borrow Lookahead Subtractor, BLS)

(a) 四輸出前看進位產生器(4-output Carry Lookahead Generator, CLG)：

設計一個四輸出之前看進位產生器，輸入變數為 P_i、G_i、及 C_0，$i = 0, 1, 2, 3$，輸出變數為 C_j，$j = 1, 2, 3, 4$。其邏輯電路圖可參考圖一之三輸出前看進位產生器 (Figure 4.11，教科書第 180 頁) 擴充之。

Design a carry lookahead generator with four carry outputs. The input variables are P_i, G_i, and C_0, $i = 0, 1, 2, 3$, and the output variables are C_j, $j = 1, 2, 3, 4$. Its logic diagram can be extended from that of a carry lookhead generator with three carry outputs shown in Figure 1 (refer to Figure 4.11, page 180 of textbook).



圖一：三輸出前看進位產生器之邏輯電路圖

Figure 1: Logic diagram of a carry lookahead generator with three carry outputs

i. 請以 gate-level modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_CLG_gate (output [4:1] C, input [3:0] P, G, input C0)，檔案則命名為 Lab2_CLG_gate.v。

Please write the Verilog circuit module in gate-level modeling. The circuit module and port list should be named as Lab2_CLG_gate (output [4:1] C, input [3:0] P, G, input C0), and its file should be named as Lab2_CLG_gate.v .

ii. 請以 dataflow modeling 方式(**assign**)撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_CLG_dataflow (output [4:1] C, input [3:0] P, G, input C0)，檔案則命名為 Lab2_CLG_dataflow.v。

Please write the Verilog circuit module in dataflow modeling (**assign**). The circuit module and port list should be named as Lab2_CLG_dataflow (output [4:1] C, input [3:0] P, G, input C0), and its file should be named as Lab2_CLG_dataflow.v .

iii. 請以 behavior modeling 方式(**always**)撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_CLG_ behavior (output [4:1] C, input [3:0] P, G, input C0)，檔案則命名為 Lab2_CLG_behavior.v。

Please write the Verilog circuit module in behavior modeling (**always**). The circuit module and port list should be named as Lab2_CLG_ behavior (output [4:1] C, input [3:0] P, G, input C0), and its file should be named as Lab2_CLG_behavior.v .

iv. 請撰寫一測試模組，至少包含下述六組測資，來測試上述三個以不同方式撰寫之前看進位產生器電路模組。請將此測試模組命名為 t_Lab2_CLG，檔案則命名為 t_Lab2_CLG.v .

Please write a testbench, including at least the following six test data, to test the circuit modules of the carry lookahead generator which are described in three different ways above. The testbench module should be named as t_Lab2_CLG, and its file should be named as t_Lab2_CLG.v .

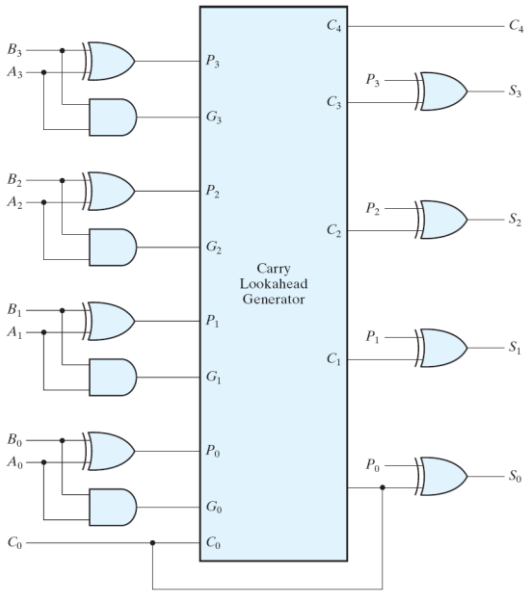
Inputs			Outputs			
P	G	C0	C4	C3	C2	C1
1101	0101	0	1	1	0	1
1100	1000	1	1	0	0	0
0101	1101	0	1	1	0	1
1000	1100	1	1	1	0	0
0101	0101	0	0	1	0	1
1011	1011	1	1	0	1	1

(b) 四位元前看進位加法器(4-bit Carry Lookahead Adder, CLA)：

設計一個四位元前看進位加法器，以產生兩個四位元二進位數字相加之結果。其輸入變數為四位元二進位被加數 ***A***、四位元二進位加數 ***B***、及進位輸入 ***Cin***，輸出變數為四位元二進位和值 ***Sum*** 與進位輸出 ***Cout***。請利用(a)中設計的前看進位產生器，電路圖如圖二所示 (參見 Figure 4.12，教科書第 181 頁)。

Design a 4-bit carry lookahead adder, which may produce the arithmetic sum of two 4-bit

binary numbers. The input variables are the 4-bit binary augend (被加數) ***A*** , the 4-bit addend (加數) ***B*****,** and the carry-in ***Cin***, and the output variables produce the 4-bit sum ***Sum*** and the carry-out ***Cout***. Use the CLG circuit module designed in (a) to build this adder. The circuit diagram of the 4-bit carry lookahead adder is shown in Figure 2 (Refer to Figure 4.12, page 181 of textbook).



圖二：四位元前看進位加法器之電路圖

Figure 1: Circuit diagram of a 4-bit carry lookahead adder

i. 請撰寫出此 CLA 之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_4_bit_CLA (output [3:0] Sum, output Cout, input [3:0] A, B, input Cin)，檔案則命名為 Lab2_4_bit_CLA.v。

Please write the HDL circuit module of the CLA. The circuit module and port list should be named as Lab2_4_bit_CLA (output [3:0] Sum, output Cout, input [3:0] A, B, input Cin), and its file should be named as Lab2_4_bit_CLA.v .

ii. 請撰寫此 CLA 之測試模組，至少以下述八組測資測試之。請將此測試模組命名為 t_Lab2_ 4_bit_CLA，檔案則命名為 t_Lab2_ 4_bit_CLA.v。

Please write the testbench of the CLA in which at least eight test data showed in the following figure should be included. The testbench module should be named as t_Lab2_4_bit_CLA, and its file should be named as t_Lab2_4_bit_CLA.v .

Inputs			Outputs	
A	B	Cin	Cout	Sum
1101	0101	0	1	0010
1100	1000	1	1	0101
0101	1101	0	1	0010
1000	1100	1	1	0101
0101	0101	0	0	1010
1011	1011	1	1	0111
1111	1111	1	1	1111
1111	0000	1	1	0000

(c) **四位元前看借位減法器(4-bit Borrow Lookahead Subtractor, BLS)：**設計一個四位元前看借位減法器，以產生兩個四位元二進位數字相減之結果。其輸入變數為四位元二進位被減數 ***X***、四位元二進位減數 ***Y***、及借位輸入 ***Bin***，輸出變數為四位元二進位差值 ***Diff*** 與借位輸出 ***Bout***。請利用(a)中設計的前看進位產生器來設計此 BLS。(Hint: 作法可參考作業練習題說明。)

Design a 4-bit borrow lookahead subtractor, which may produce the arithmetic difference of two 4-bit binary numbers. The input variables are the 4-bit binary minuend (被減數) ***X*** , the 4-bit subtrahend (減數) ***Y***, and the borrow-in ***Bin***, and the output variables produce the 4-bit difference ***Diff*** and the borrow-out ***Bout***. Use the CLG circuit module designed in (a) to build this subtractor. (Hint: Refer to the description in the homework exercise.)

i. 請撰寫出此 BLS 之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_4_bit_BLS (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案則命名為 Lab2_4_bit_BLS.v。

Please write the HDL circuit module of the BLS. The circuit module and port list should be named as Lab2_4_bit_BLS (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_4_bit_BLS.v .

ii. 請撰寫此 BLS 之測試模組，至少以下述八組測資測試之。請將此測試模組命名為 t_Lab2_4_bit_BLS，檔案則命名為 t_Lab2_4_bit_BLS.v。

Please write the testbench of the BLS in which at least eight test data showed in the following figure should be included. The testbench module should be named as t_Lab2_4_bit_BLS, and its file should be named as t_Lab2_4_bit_BLS.v .

Inputs			Outputs	
X	Y	Bin	Bout	Diff
1101	0101	0	0	1000
1100	1000	1	0	0011
0101	1101	0	1	1000
1000	1100	1	1	1011
0101	0101	0	0	0000
1011	1011	1	1	1111
0000	1111	0	1	0001
0000	1111	1	1	0000

B. **Excess-3 加法器(Excess-3 Adder)**

設計一個可將兩個 Excess-3 數字及進位輸入相加的組合電路。其輸入變數為 Excess-3 數字 ***A*** 與 ***B***，以及進位輸入 ***Cin***；輸出變數為 Excess-3 和值 ***Sum*** 與進位輸出 ***Cout***。(Hint: 作法可參考作業練習題說明。)

Design a combinational circuit for the arithmetic addition of two decimal digits represented by Excess-3 code, together with an input carry. The input variables are 4-bit Excess-3

digits, ***A*** and ***B***, and the input carry ***Cin***, and the output variables are 4-bit sum in Excess-3, ***Sum***, and the output carry, ***Cout***. (Hint: Refer to the description in the homework exercise.)

i. 請以 bevhavior modeling 方式撰寫 Excess-3 加法器之 HDL 電路模組，其模組名稱與 port list 請訂為 Lab2_Excess_3_adder_behavior (ouput [3:0] Sum, output Cout, input [3:0] A, B, input Cin)，檔案命名為 Lab2_ Excess_3_adder_behavior.v。
Please write the HDL circuit module of Excess-3 Adder in behavior modeling. The circuit module and port list should be named as Lab2_Excess_3_adder_behavior (ouput [3:0] Sum, output Cout, input [3:0] A, B, input Cin), and its file should be named as Lab2_Excess_3_adder_behavior.v .

ii. 請撰寫此 Excess-3 adder 之測試模組，至少以下述六組測資測試之。請將此測試模組命名為 t_Lab2_Excess_3_adder_behavior，檔案則命名為 t_Lab2_Excess_3_adder_behavior.v。
Please write the testbench of the Excess-3 adder in which at least six test data showed in the following figure should be included. The testbench module should be named as t_Lab2_Excess_3_adder_behavior, and its file should be named as t_Lab2_Excess_3_adder_behavior.v .

Inputs			Outputs	
A	B	Cin	Cout	Sum
0011	0011	0	0	0011
0011	0011	1	0	0100
1000	0111	0	0	1100
1000	0111	1	1	0011
1100	1100	0	1	1011
1100	1100	1	1	1100

C. 注意事項：(Notes)

- 請用 ModelSim Student Edition 10.4a 做為開發環境。
  Develop your lab in ModelSim Student Edition 10.4.a.
- 請務必依照上述各項目之規定命名模組及檔案。
  Be sure to name the modules and files as described above.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar TestBench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：word 檔，命名為 Lab2_學號_姓名

包含下列項目：配分含隱藏測資之測試及 Demo 狀況

Hand in a word file, named Lab2_StudentID_Name , including the following items:
(Scores include answering problems in demo and the testing of extra data.)

(1) 詳述如何擴充圖一之三輸出前看進位產生器得到四輸出前看進位產生器，包括：布林代數式、邏輯電路圖。附上 2A(a)iv (四輸出前看進位產生器) 之模擬結果波形圖，並說明三個以不同方式撰寫之四輸出前看進位產生器電路模組之波形圖是否有差異及是否正確。(30%)

Describe the design process of the 4-output carry lookahead generator (CLG) by extending from the 3-input CLG, including the Boolean expressions, the logic diagram, etc. Attach the waveforms of the simulation results for the three modules of the 4-output carry lookahead generator (CLG) tested in 2A(a)iv, and determine whether the waveforms are correct or not and explain the difference of the waveforms, if any. (30%)

(2) 針對四位元前看進位加法器，附上 2A(b) ii (4-bit CLA) 之模擬結果波形圖，並說明是否正確。(20%)

Attach the waveform of the simulation results for the module of the 4-bit carry lookahead adder tested in 2A(b) ii, and explain whether it is correct or not. (20%)

(3) 詳述四位元前看借位減法器之電路設計流程，如：列出相關布林代數式(如：*Pi*、*Gi*、*Bi*、*Di* 等)。附上 2A(c) ii (4-bit BLS) 之模擬結果波形圖，並說明是否正確。(20%)

Describe the design process of the 4-bit borrow lookahead subtractor (BLS), for examples, deriving the Boolean expressions of *Pi*, *Gi*, *Bi*, and *Di*. Attach the waveform of the simulation results for the module of the 4-bit BLS tested in 2A(c)ii, and explain whether it is correct or not. (20%)

(4) 詳述 Excess-3 加法器之電路設計，畫出電路方塊圖。附上 2B ii (Excess-3 加法器) 之模擬結果波形圖，並說明是否正確。(20%)

Describe the design process of the Excess-3 adder and draw the block diagram of the circuit. Attach the waveform of the simulation results for the module of the Excess-3 adder tested in 2B ii, and explain whether it is correct or not. (20%)

(5) 心得與感想、及遭遇到的問題或困難 (10%)

Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab. (10%)

B. Verilog modules 檔案繳交：10 files

Hand in the following Verilog modules: 10 files

Lab2_CLG_gate.v、Lab2_CLG_dataflow.v、
Lab2_CLG_behavior.v、t_Lab2_CLG.v、
Lab2_4_bit_CLA.v、t_Lab2_4_bit_CLA.v、
Lab2_4_bit_BLS.v、t_Lab2_4_bit_BLS.v、
Lab2_ Excess_3_adder_behavior.v、t_Lab2_Excess_3_adder_behavior.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (word file) and the corresponding HDL code (.v files) onto e-Campus platform.

- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** 或是 **rar 檔**(禁止上傳其他檔案格式)，並以「Lab2_學號_姓名」的方式命名，如：「Lab2_0816000_王大明」。
  Please compress the word file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file or **rar** file (other format is not accepted), and name the zip file as "Lab2_StudentID_Name" , for example, "Lab2_0816000_Kent Chang".

- 作業繳交截止日期為 **2020/5/25 (一) 23:55**，**不接受逾期繳交**。
  The deadline for handing in lab report and Verilog files is **May 25 (Monday) 23:55. No late hand-in is allowed.**

- **Demo** 時間暫定為 **2020/5/27 (三) 1:00pm~9:00pm**，之後會再發公告通知大家上網填寫 Demo 時間表。未繳交作業者，將無法參加 Demo；有繳交作業但未 Demo 者，亦不予計分。
  The **demo time** is arranged at **2020/5/27 (Wednesday) 1:00PM~9:00PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. Those who have not hand-in their lab reports and Verilog files will not be able to demo their work, and those who have not demo their lab assignments will get zero score.

- **禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。**
  Any assignment work by fraud will get a zero point.