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Design Project

Report Title	Amplifier Design Project
Group Number	
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Table of Content

1. Introduction

The final report for the design project, Amplifier Design Project, is presented herein. The lab took place on March 27th, 2024 and is due on April 7th, 2024. This lab tests all course material regarding Bipolar-Junction Transistors (BJT), and requires the implementation of a multistage amplifier. The circuit was simulated using Multisim and all calculations can be found in the appendix below (Pg 10).

2. Objectives

The objective of this lab was to design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfills a set of specifications. Bipolar-Junction Transistors in active mode are utilized to create the multistage amplifier. Results were checked with values obtained from the simulated circuit and the specifications requirements below:

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: no larger than $\mathbf{10}\ \boldsymbol{mA}$;
- No-load voltage gain (at 1 kHz): $|\boldsymbol{Avo}| = \mathbf{50}$ ($\pm$ 10%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with RL = 1 $k\Omega$): no smaller than 90% of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): no smaller than 4 V peak
- to peak;
- Input resistance (at 1 kHz): no smaller than $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz ($-\boldsymbol{3dB}$ response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than $\mathbf{220}\ \boldsymbol{k\Omega}$ from the E24 series;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

Notes:

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, Rs, must be 600 Ω for all tests.

3. Circuit under Test

Figure 1 below is a schematic diagram of the test circuit. Thus the amplifier circuit consists of three stages, two Common-Emitter amplifiers back to back and an Emitter-Follower. The two CE amplifiers were chosen to achieve the no load gain of 50 since using a singular CE amplifier would cause too much distortion. The total gain was split between the two CE amplifiers to supply around 7.1 each. This was found from the square root of 50 as the total gain is the product of the gain from each stage, and since voltage gain from a CC (stage 3) is approximately 1. Therefore total gain would be *7.1 x 7.1 x 1 ≈ 50.*

The signal source consists of a signal voltage *Vs* with a peak-to-peak voltage of *100 mV* (50 mV_{pk}) and frequency of *1 kHz*, as well as a signal resistor R_s of *600 Ω*. V_1 represents the V_{cc} DC voltage of *10 V.*

Emitter and collector resistors were chosen first by calculating the current and input resistance of each stage. Emitter resistor R_{E5} was chosen to be a smaller value so it doesn't

significantly affect the loading properties of the load stage. The emitter degeneration resistors for the first two stages were chosen next by comparing it to the 7.1 gain needed. Finally the six biasing resistors in the voltage dividers were chosen. The resistance was chosen to be large enough to supply supple negative feedback while still allowing enough current to pass through. A low resistance would cause the input resistance to decrease as well, creating a large loading impact between each stage.

Each stage utilizes a *2N3904 BJT* (Q_1, Q_2, Q_3), biasing resistors for the voltage divider, and collector and emitter resistors. Electrolytic capacitors C_1, C_3, and C_5 are used to bypass AC signals from flowing backwards and have a capacitance of *10 μF.* These coupling capacitors are used in between stages since input resistances are large. The overall gain of the amplifier could be affected by small changes in the emitter degeneration resistor which is why capacitors C_2, C_4, and C_6 are instead *100 μF,* as a higher capacitance is needed for emitter degeneration. The values for the resistors and capacitors are listed in **Tables 1, 2, 3** below:

R_1 [$k\Omega$]	R_2 [$k\Omega$]	R_3 [$k\Omega$]	R_4 [$k\Omega$]	R_5 [$k\Omega$]	R_6 [$k\Omega$]
91	68	91	68	91	200

Table 1: Biasing Resistor Values

R_{C1} [$k\Omega$]	R_{C2} [$k\Omega$]	R_{E1} [$k\Omega$]	R_{E2} [$k\Omega$]	R_{E3} [$k\Omega$]	R_{E4} [$k\Omega$]	R_{E5} [$k\Omega$]	R_L [$k\Omega$]
15	13	15	1.5	15	1.3	1	1

Table 2: Collector and Emitter Resistor Values

C_1 [μF]	C_2 [μF]	C_3 [μF]	C_4 [μF]	C_5 [μF]	C_6 [μF]
10	100	10	100	10	100

Table 3: Capacitor Values

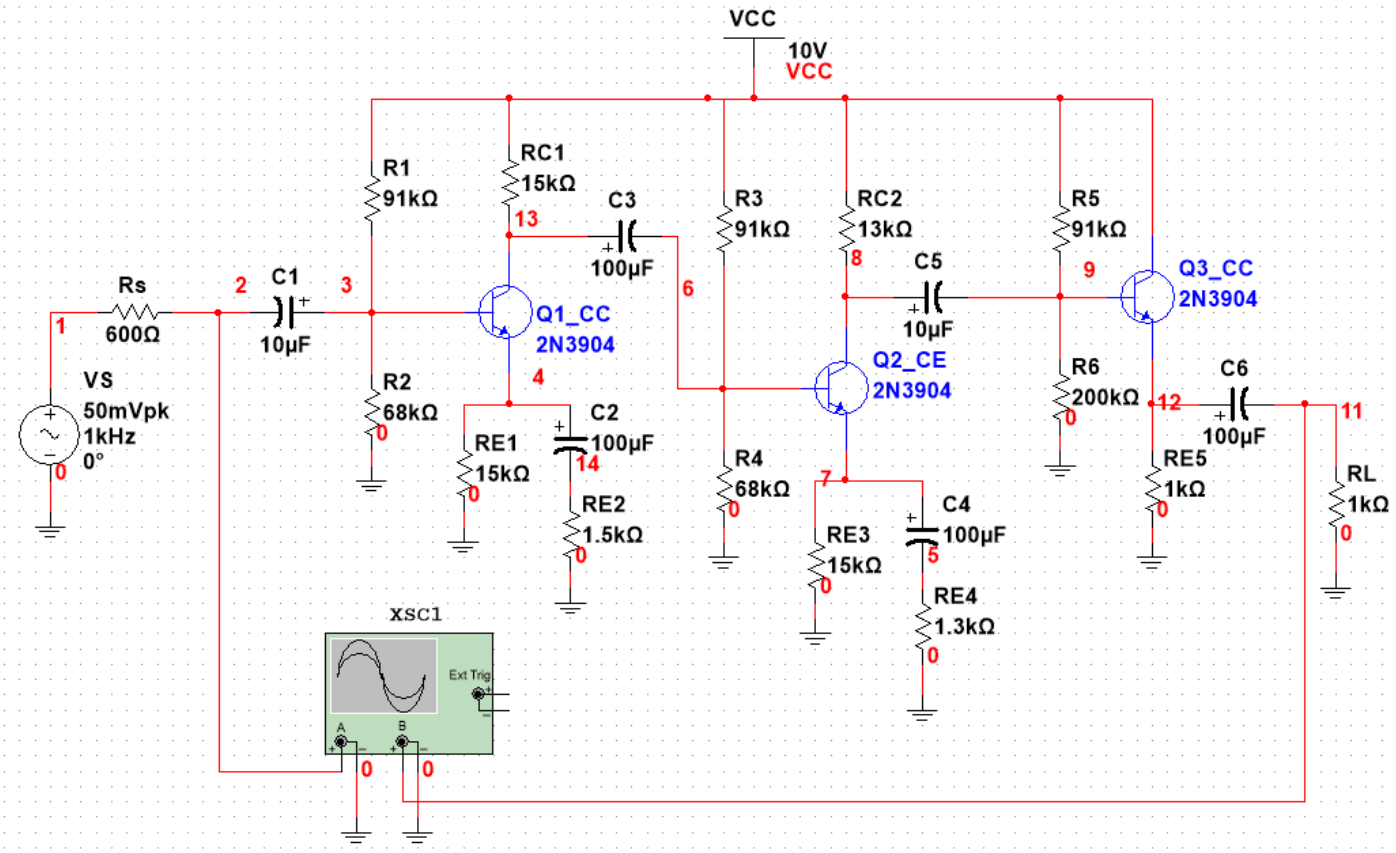
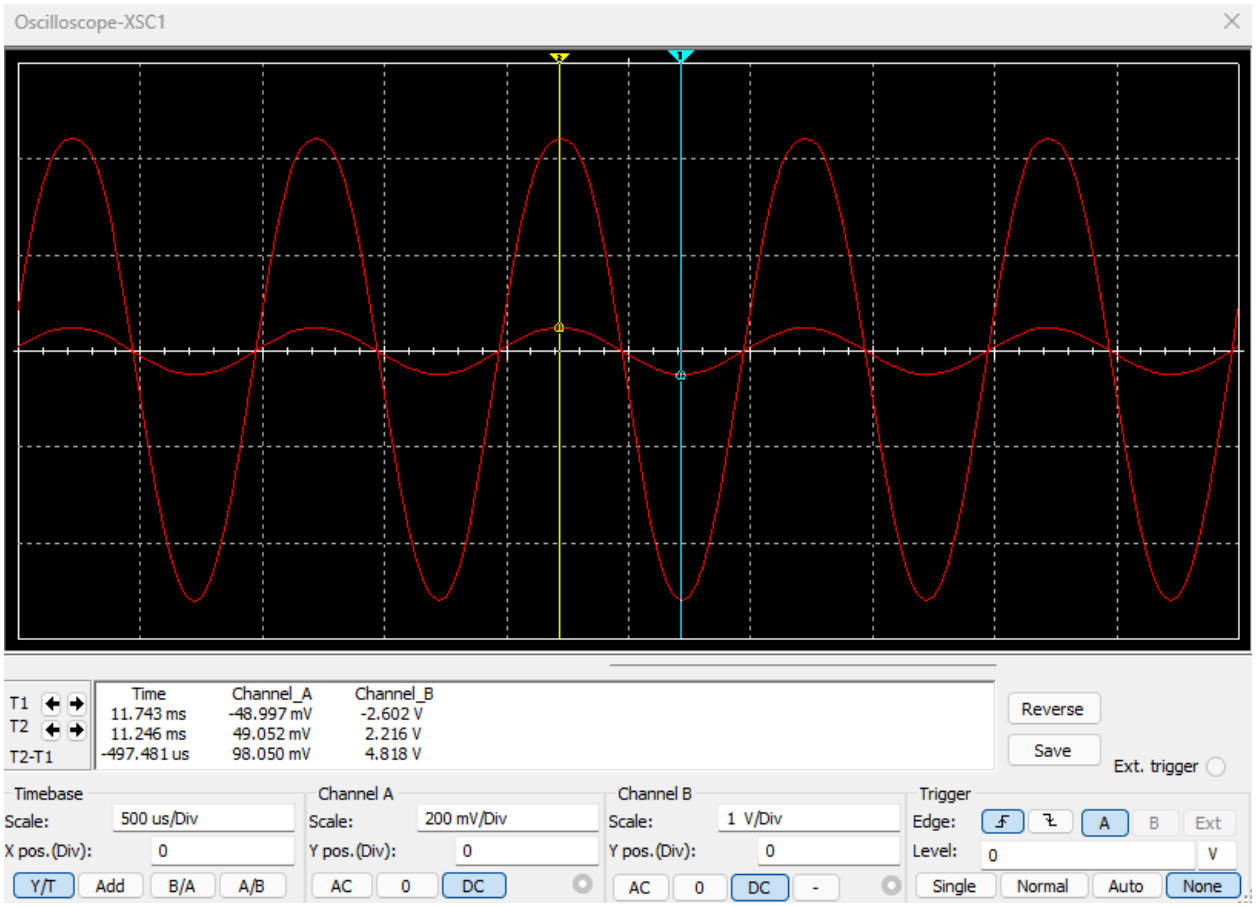


Figure 1: Three-stage amplifier following a CE-CE-CC configuration.

4. Experimental Results

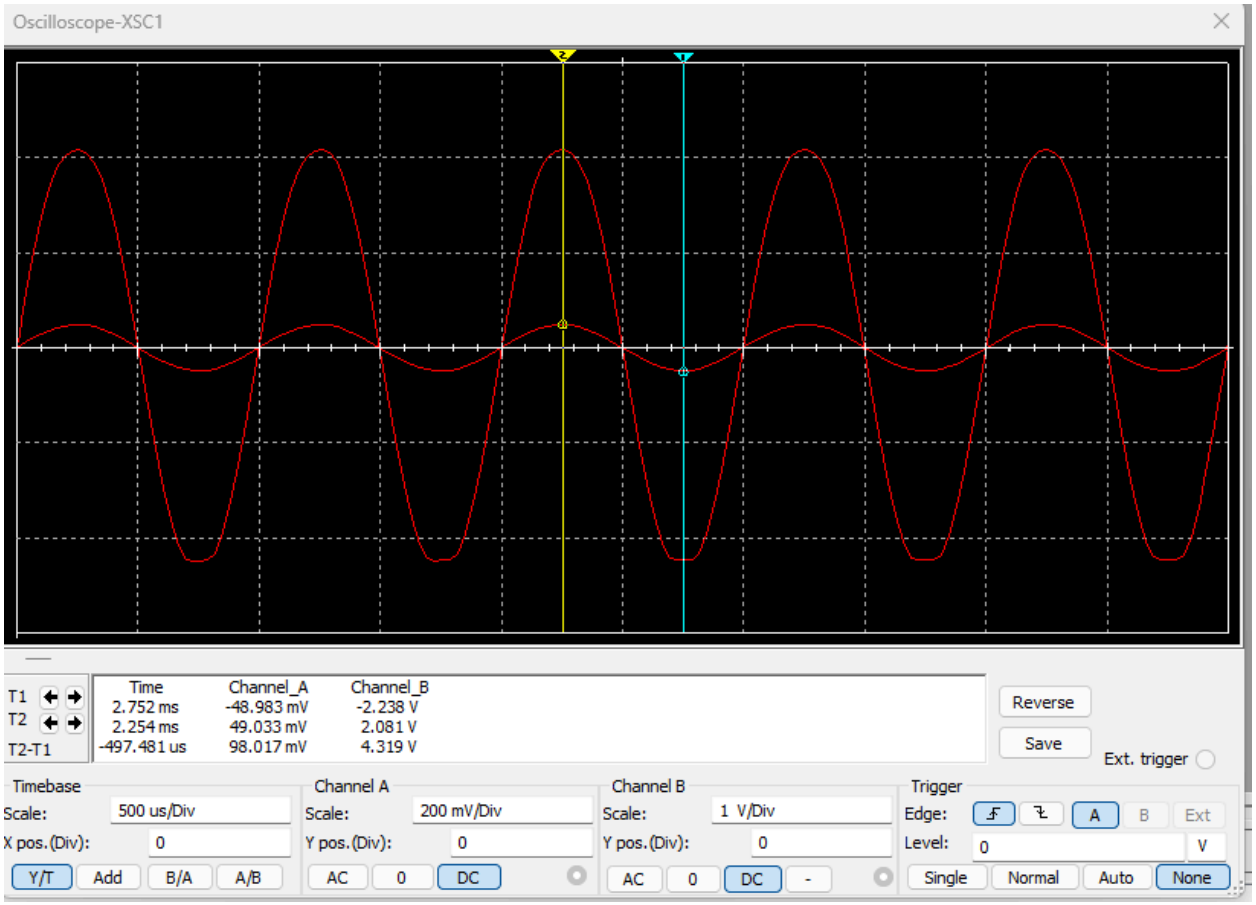
The circuit in **Figure 1** was constructed and simulated in Multisim. The V_i and V_o waveforms were then captured with the parameters of the no-load gain A_{vo} and loaded gain A_v measured and calculated. Quiescent current drawn from Vcc, the frequency response, and the input resistance were then found and compared to specifications list. **Graph 1, 2, 3, Table 4, 5, 6,** and **Figure 2** and **3** report the results.



Graph 1: Simulated results of V_i and V_o for **Figure 1** with **no-load** (RL = ∞).

$\mathbf{V_{i,pp}}$ [V]	$\mathbf{V_{o,pp}}$ [V]	$\mathbf{A_{vo}}$ [V/V]
0.098	4.818	49.163

Table 4: Simulated results of **no-load** voltage swing for **Figure 1** (RL = ∞).



Graph 2: Simulated results of V_i and V_o for **Figure 1** with **load** (RL = 1 kΩ).

$\mathbf{V_{i,pp}}$ [V]	$\mathbf{V_{o,pp}}$ [V]	$\mathbf{A_v}$ [V/V]
0.098	4.319	44.071

Table 5: Simulated results of **loaded** voltage swing for **Figure 1** (RL = 1 kΩ).

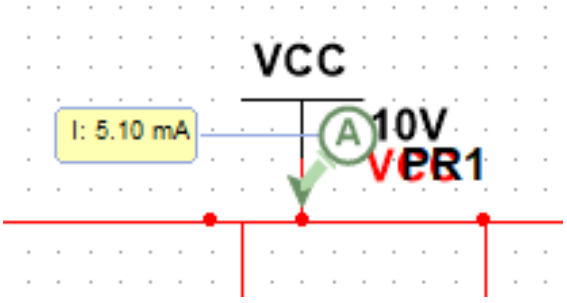
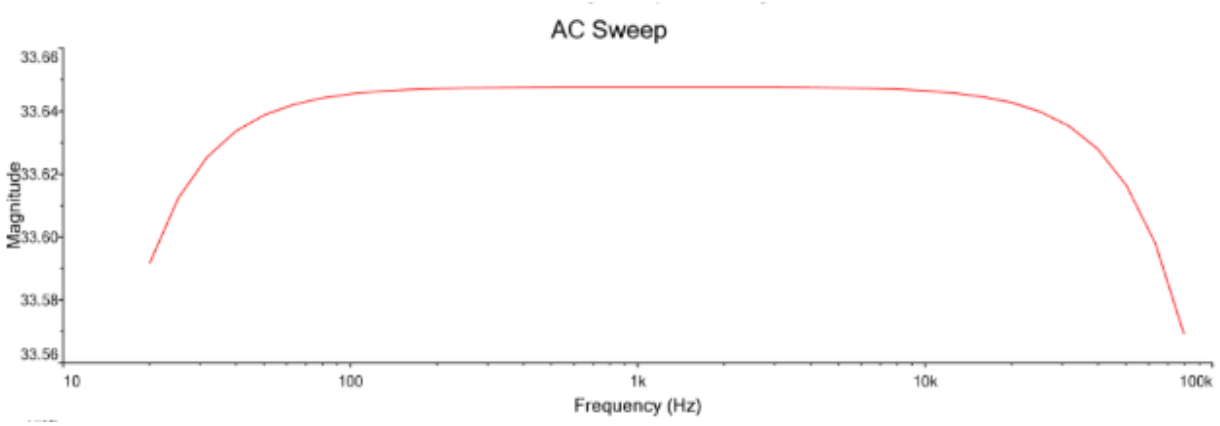


Figure 2: Quiescent current drawn from *Vcc* in **Figure 1** (*I ≤ 10 mA*).



Graph 3: Frequency response graph of **Figure 1**.

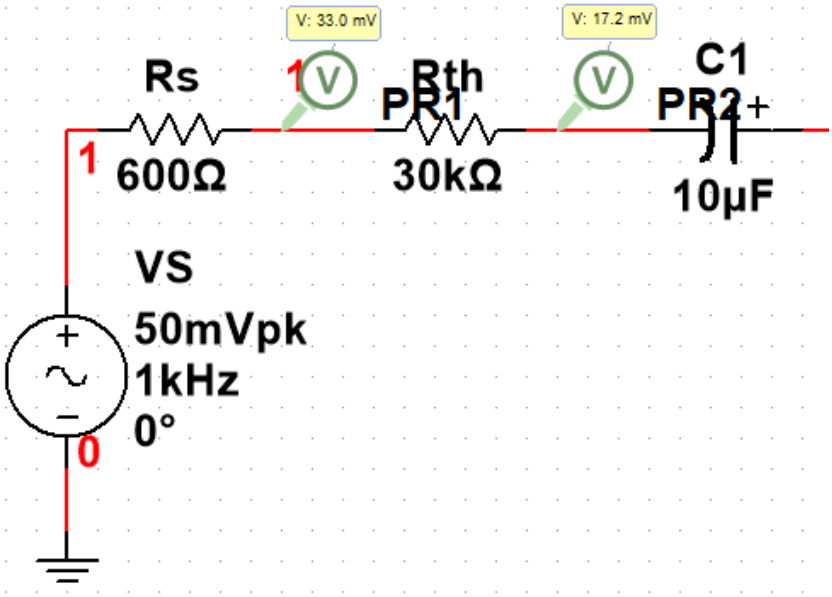


Figure 3: Voltage values of V_i and V_{th}.

R_{th} [kΩ]	V_{th} [mVrms]	V_i [mVrms]	$R_{in,measured}$ [kΩ]	$R_{in,\ calculated}$ [kΩ]
30	33	17.2	32.658	31.195

Table 6: Values from **Figure 3** used to measure $R_{in.}$

5. Conclusions and Remarks

Specification	Calculated Value	Tested Value	% Error	Achieved?
Quiescent current drawn from the power supply: no larger than $\mathbf{10\ mA}$;	5.23 mA	5.10 mA	2.549%	Yes
No-load voltage gain (at 1 kHz): $\lvert Avo \rvert$ = **50** (± **10**%);	50.41	49.163	2.5365%	Yes
Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;	8 V	4.818 V_{pp}	66.044%	No
Loaded voltage gain (at 1 kHz and with RL = 1 $k\Omega$): no smaller than **90**% of the no-load voltage gain;	47.57	44.071	7.9395%	Yes
Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): no smaller than 4 V peak to peak;	4 V	4.319 V_{pp}	7.386%	Yes
Input resistance (at 1 kHz): no smaller than $\mathbf{20\ k\Omega}$;	31.195 kΩ	32.658 kΩ	4.4798%	Yes
Frequency response: 20 Hz to 50 kHz ($-3dB$ response);	–	**Graph 3**	–	Yes

When comparing values measured from **Figure 1** to values manually calculated, it is seen that the majority of the specifications have been met with a relatively small percent error. The maximum no-load output voltage swing is the only specification not met as the tested value is not greater than 8 V peak to peak. This could be due to error in calculations or in the simulation where the biasing of each stage may differ. Another likely case is that the operating point chosen is too close to the threshold voltage as the output voltage is not able to swing a full 8 volts. This could also be resolved if a lower frequency was used as V_S as it would allow the output voltage to swing more. The other percent errors could be due to calculation errors such as rounded resistance values to meet the E24 series requirement. Besides the one discrepancy, all other specifications were met with a percent error less than 10%, meaning that the circuit and calculations used were proven effective and successful.

6. Appendix - Calculations

No load Voltage gain: $|A_{Vol}| = 50 \pm 10\%$

Max No load Output Voltage Swing : $V_{pp} \geq 8V$

Loaded Voltage gain ($R_L = 1k\Omega$) : $A_V \geq 90\%$ of A_{Vo}

Max loaded output voltage swing ($R_L = 1k\Omega$) : $V_{pp} \geq 4V$

Input resistance : $R_{in} \geq 20k\Omega$

Must be CE to CE to CC

Gain Distribution

$V_{CC} = 10V$
$I_{DC} \leq 10mA$
$A_{Vo} = 50 \pm 5$ (10%)
$V_o \geq 8\ V_{pp}$
$V_L \geq 4\ V_{pp}$
$R_{in} \geq 20k\Omega$
all $R \leq 220k\Omega$

$A_{Vototal} = A_{V_1} \cdot A_{V_2} \cdot A_{V_3}$
Voltage Gain of CC ≈ 1 $\therefore A_{V_3} \approx 1$
$50 = A_{V_1} \cdot A_{V_2} \cdot 1$
$\sqrt{50} \approx 7.1$
$A_{V_1} = A_{V_2} = 7.1$
↳ $A_{V01} = \frac{V_2}{V_1} = -7.1$
$A_{V02} = \frac{V_4}{V_3} = -7.1$

negative since CE is inverting.
-ve x -ve x +ve = +ve
∴ Final output is Non-inverting

Stage 1 & 2 (CE)

$A_{V01} = A_{V02}$
∴ I_{C1} & I_{C2} = 400μA from load line.

$g_m = \frac{I_C}{V_T} = \frac{400\mu A}{26mV} = 0.01545$
$I_B = 5.5\mu A$
$\beta = \frac{400mA}{2.5\mu A} = 114.3$

$I_{B,DC} = 2\mu A$ (for quiescent)

Stage 3 (CC)

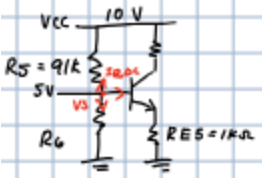
Assuming $R_{E3} = 1k\Omega$ (same as R_L)

$g_m = \frac{10mA}{26mV} = 0.385$
$I_C = 10mA$ } from load line
$I_B = 65\mu A$ }
$\beta = \frac{I_C}{I_B} = \frac{10mA}{65\mu A} = 153.8$

Using 91kΩ for R_3
- From E24 series
- V_B shouldn't be affected
- Divider current >> I_B

$I_{B,DC} = 30\mu A$ (quiescent)

KCL @ Vs



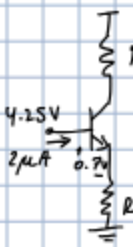
$$\frac{5-10}{91k} + \frac{5}{R_6} + 30\mu A = 0$$

$$-24.945\mu + \frac{5}{R_6} = 0$$

$$R_6 = \frac{5V}{24.945\mu A}$$

$R_6 = 200\ k\Omega$

Stage 2 KVL



$$-4.25 + 0.7 + I_E \cdot R_{E3} = 0 \qquad (I_E = (1+\beta)I_B)$$

$$-3.55 + (1+119.3)\,2\mu\, R_{E3} = 0$$

$R_{E3} \approx 15k\Omega$

$$I_{C,DC} = \frac{V_{CC}}{R_C + R_{E3}}$$

$$R_C + R_{E3} = \frac{10V}{400\mu A} = 25k\Omega$$

$$R_C = 25k - 15k$$

$R_C = 10k\Omega$

From Stage 8: $R_{in_2} = R_S \| R_6 \| \frac{\beta}{g_m} + (\beta+1)R_E$

$= 91k \| 200k \| \frac{158.8}{0.385} + (154.8)(1k)$

$= 44.57\ k\Omega$

$$\frac{1}{R_C} = \frac{1}{R_{C2}} + \frac{1}{R_{in3}}$$

$R_{C2} \approx 13\ k\Omega$

R_E for Stage 1 & 2

$$A_{V01} = \frac{V_3}{V_1} = \frac{-g_{m2}(R_{C2} \| R_{in3})}{1 + g_{m2}R_E}$$

$$-7.1 = \frac{-0.0154(13k \| 44.57k)}{1 + (0.0154)R_E}$$

$R_{E_{1,2}} = 1353\ \Omega$

$$R_{in_{L3}} = 91k \| 200k \| \frac{158.8}{0.385} + (154.8)(500)$$

$= 39.67\ k\Omega$

$$A_{V2} = \frac{-0.0154\,(13k \| 39.67k\Omega)}{1 + 0.0154(1353)}$$

$A_{V2} = -6.7$

R_{E4} for Stage 2

$R_E = 1353\Omega \approx 1.3k\Omega$

$1.3k = \frac{1}{\frac{1}{R_{B3}} + \frac{1}{R_{E4}}}$

$\frac{1}{1.3k} = \frac{1}{15k} + \frac{1}{R_{E4}}$

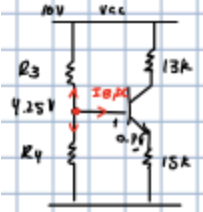
$R_{E4} \approx 1.3k\Omega$ (rounded down since lower R_E results to more gain)

Biasing Resistors

Divider current >> I_B

Assume $R_B = 91k\Omega$

KVL @ V_B



$\frac{4.25-10}{91k} + \frac{4.25}{R_4} + 2\mu A = 0$

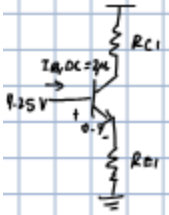
$R_4 \approx 93k\Omega$

$R_{in2} = R_3 \| R_4 \| \frac{\beta}{g_m} + (\beta+1) R_E$

$= 91k \| 68k \| \frac{114.3}{0.0154} + (115.3)(1353)$

$\approx 31.433k\Omega$

KVL for Stage 1



$-4.25 + 0.7 + I_E \cdot R_{E1} = 0$

$(1+\beta) I_B R_{E1} = 3.55$

$(114.3 + 1)(2\mu) R_{E1} = 3.55$

$R_{E1} \approx 15k\Omega$

$I_{C,DC} = \frac{V_{CC}}{R_{E1}+R_C}$

$R_C + R_{E1} = \frac{10V}{400\mu A} = 25k\Omega$

$R_C = 25k - 15k$

$R_C = 10k\Omega$

$R_C = R_{C1} \| R_{in2}$

$10k = \frac{1}{\frac{1}{R_{C1}} + \frac{1}{31.433}}$

$R_{C1} \approx 15k\Omega$

$A_{V1} = \frac{-g_m (R_{C1} \| R_{in2})}{1 + g_m R_E}$

$-7.1 = \frac{-0.0154 (14k \| 31.433k)}{1 + 0.0154 R_E}$

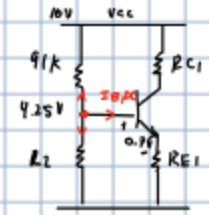
$R_E \approx 1.3k\Omega$

$R_E = R_{E1} \| R_{E2}$

$\frac{1}{1.3k} = \frac{1}{R_{E2}} + \frac{1}{15k}$

$R_{E2} \approx 1.5k\Omega$

KCL @ V_2



$$\frac{4.25-10}{91k} + \frac{4.25}{R_2} + 2\mu A = 0$$

$R_2 \approx 68\,k\Omega$

$$R_{in} = 91k \parallel 68k \parallel \frac{\beta}{g_m} + (\beta+1)R_E$$
$$= 91k \parallel 68k \parallel \frac{100}{0.0154} + (100+1)(12.99)$$
$$\approx 31.193k\Omega$$

Capacitors

- C_2, C_4, C_6 must be large to maintain gain. ($100\mu F$)
- C_1, C_3, C_5 can be lower since $R_{in1}, R_{in2}, R_{in3}$ are already high. ($10\mu F$)
- frequency: $20Hz - 50kHz$
- $Z = \frac{1}{j\omega C}$

Worst case: $f = 20Hz$

$C_{2,4,6}$:
$$Z = \frac{1}{j2\pi fc} = \frac{1}{j2\pi(20)(100\mu F)} = 79.6\,\Omega$$

$C_{1,3,5}$:
$$Z = \frac{1}{j2\pi(20)(10\mu F)} \leq 796\,\Omega$$

Best case: $f = 50kHz$

$C_{2,4,6}$:
$$Z = \frac{1}{j2\pi fc} = \frac{1}{j2\pi(50k)(100\mu F)} = 31.8m\Omega$$

$C_{1,3,5}$:
$$Z = \frac{1}{j2\pi(50k)(10\mu F)} \leq 0.32\,\Omega$$

From Calculated impendance, the selected capacitors $10\mu F$ & $100\mu F$ should maintain gain.

Final Gain:

$A_{V0} = -7.1 \times -7.1 \times 1 = 50.41$ within 10% of 50

$A_V = -6.7 \times -7.1 \times 1 = 47.57$ within 90% of A_{V0}

Quiescent current:

$$I_{DC,total} = I_{C1} + I_{B1} + I_{C2} + I_{B3} + I_{C3} + I_{B5}$$
$$= \beta I_{B1} + \frac{V_{CC}}{R_1+R_2} + \beta I_{B2} + \frac{V_{CC}}{R_3+R_4} + \beta I_{B3} + \frac{V_{CC}}{R_5+R_6}$$
$$= 5.23\,mA < 10\,mA$$