```
# synthesized BLIF
.model lion9_syn
.inputs x0 x1
.outputs v6_4
.latch    v6_0  s0   0
.latch    v6_1  s1   0
.latch    v6_2  s2   1
.latch    v6_3  s3   0

.gate INVX1   A=s1 Y=n16
.gate AND2X1  A=s3 B=n16_Y=n17
.gate NOR2X1  A=n16_B=x0 Y=n18_1
.gate AND2X1  A=n18_1 B=s3 Y=n19
.gate INVX1   A=x1 Y=n20
.gate AND2X1  A=n20 B=x0 Y=n21
.gate AND2X1  A=n21 B=s3 Y=n22
.gate NOR2X1  A=s3 B=x0 Y=n38
…
<omitted gate descriptions>
…
.gate OR2X1   A=n38 B=n8 Y=n39
.gate OR2X1   A=n39 B=n25 Y=n40
.gate OR2X1   A=n40 B=n19 Y=n18
.gate OR2X1   A=n34 B=n25 Y=n42
.gate OR2X1   A=n42 B=n22 Y=n43
.gate OR2X1   A=n43 B=n17 Y=n23
.end
```