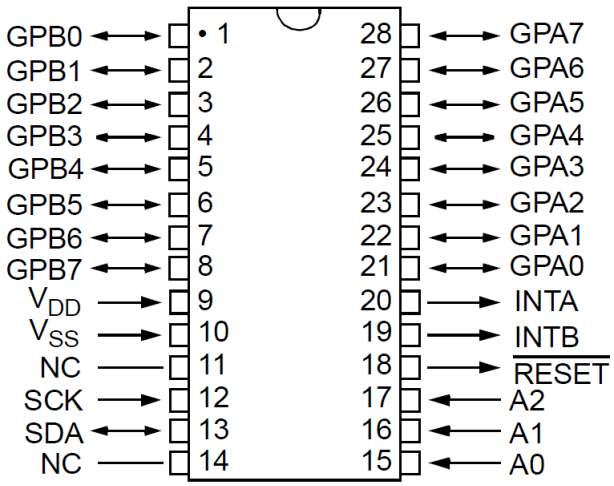
MCP23017 16-Bit I/O Expander with I2C Interface

Prof. Short

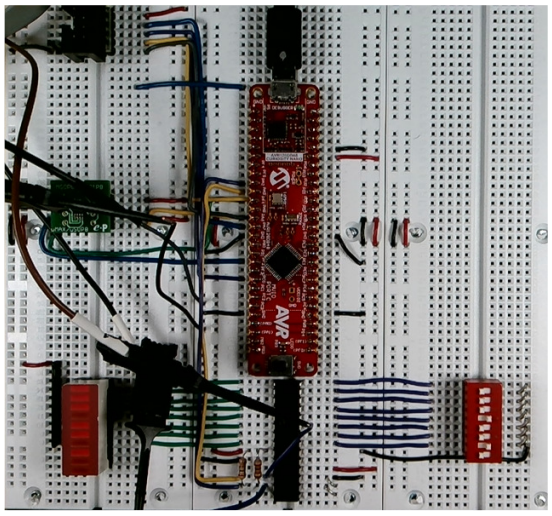
Sources

- The figures in this lecture and some text are taken from the following two references.
- Microchip MCP23017/MCP23S17 16-Bit I/O Expander with Serial Interface (data sheet).
- Microchip AN1043 Unique Features of the MCP23X08/17 GPIO Expanders (application note).

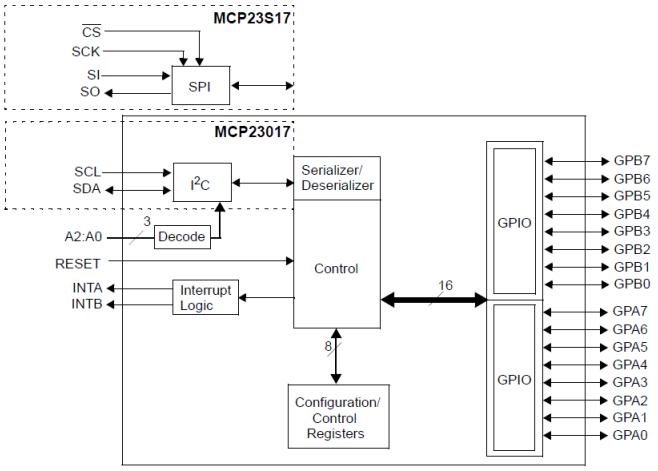
MCP23017 in DIP Pinout



Prototype Layout



MCP23017 Functional Block Diagram



IOCON: I/O Expander Configuration Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—
bit 7							bit 0

bit 7 **BANK:** Controls how the registers are addressed
1 = The registers associated with each port are separated into different banks.
0 = The registers are in the same bank (addresses are sequential).

bit 6 **MIRROR:** INT Pins Mirror bit
1 = The INT pins are internally connected
0 = The INT pins are not connected. INTA is associated with PORTA and INTB is associated with PORTB

bit 5 **SEQOP:** Sequential Operation mode bit
1 = Sequential operation disabled, address pointer does not increment.
0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew Rate control bit for SDA output
1 = Slew rate disabled
0 = Slew rate enabled

IOCON: I/O Expander Configuration Register

bit 3 **HAEN:** Hardware Address Enable bit (**MCP23S17** only) (Note 1)
1 = Enables the MCP23S17 address pins.
0 = Disables the MCP23S17 address pins.

bit 2 **ODR:** Configures the INT pin as an open-drain output
1 = Open-drain output (overrides the INTPOL bit.)
0 = Active driver output (INTPOL bit sets the polarity.)

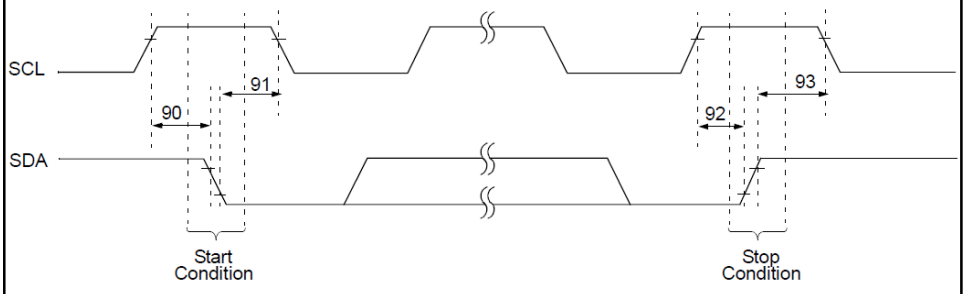
bit 1 **INTPOL:** This bit sets the polarity of the INT output pin
1 = Active-high
0 = Active-low

bit 0 **Unimplemented:** Read as '0'

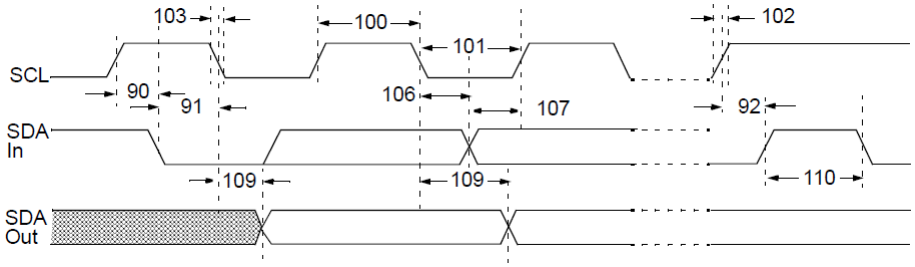
Note 1: Address pins are always enabled on the MCP23017.

Note: Unlike all other registers which are not shared between the two ports (Port A and Port B), there is one register (IOCON). which is shared between the ports and affects both equally.

MCP23017 I2C Bus START/STOP Bits Timing



MCP23017 I2C Bus Data Timing



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MCP23017 I2C Byte and Sequential Write

S - Start
SR - Restart
P - Stop
W - Write
R - Read
OP - Device opcode
ADDR - Device register address
D_{OUT} - Data out from MCP23017
D_{IN} - Data in to MCP23017

Byte: S | OP | W | ADDR → D_{IN} → P

Sequential: S | OP | W | ADDR → D_{IN} .... D_{IN} → P

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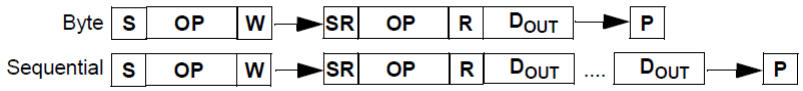
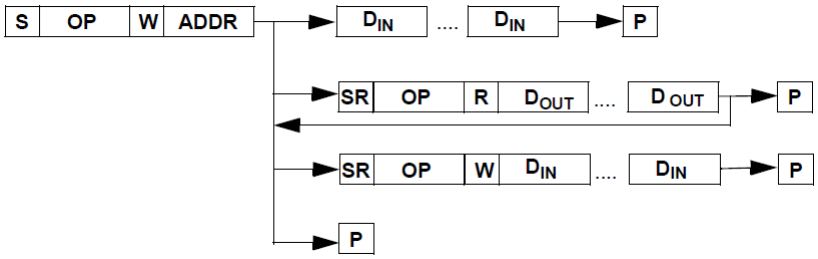
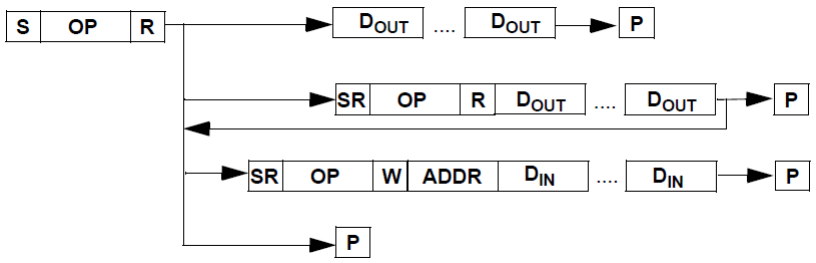
MCP23017 I2C Byte and Sequential Read



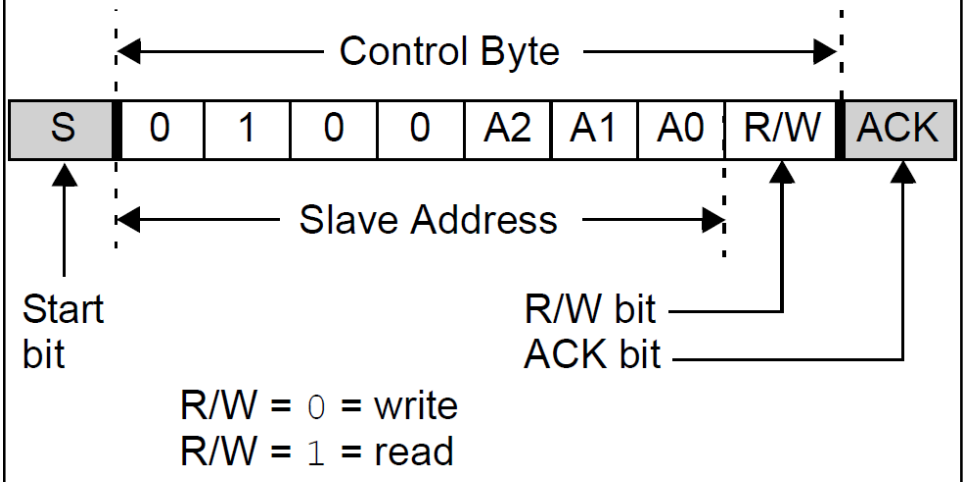
MCP23017 I2C Sequential Write/Read



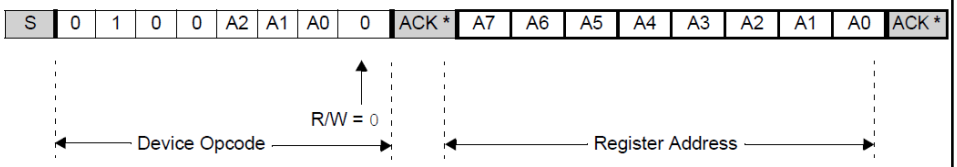
MCP23017 I2C Sequential Write/Read (cont.)



I2C Control Byte Format



I2C Addressing Registers



*The ACKs are provided by the MCP23017.

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GPIO Expander with an I2C Interface

- Initialization
  - Configure IOCON register to set BANK = 1 for separate ports. Note IOCON address is 0x0A at reset.
  - Configure IODIRA to set GPA port as all inputs.
  - Configure IODIRB to set GPB port as all outputs.
  - Configure GPPUA to enable pull ups at GPA inputs.
- Main loop
  - Read GPIOA register to get switch values at GPA port.
  - Reverse pin order of input bits.
  - Write OLATB register to control bargraph at GPB port.

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Address Map

8-Bit Mode:

When in 8-bit mode, the ports' registers are separated:

- Port A register addresses range from 00h – 0Ah
- Port B register addresses range from 10h – 1Ah

16-bit Mode:

When in 16-bit mode, the ports' registers are interleaved to emulate 16-bit wide registers:

- Port A and Port B register addresses range from 00h – 15h. The registers are still addressed as 8-bit ports, meaning that the 16-bit mapping pair is always an even number (e.g., IODIR starts at 00h, IPOL starts at 02h, etc.)

8-bit Mode		16-bit Mode	
Register Name	Address (hex)	Register Name	Address (hex)
IODIRA	00	IODIRA	00
IPOLA	01	IODIRB	01
GPINTENA	02	IPOLA	02
DEFVALA	03	IPOLB	03
INTCONA	04	GPINTENA	04
IOCON	05	GPINTENB	05
GPPUA	06	DEFVALA	06
INTFA	07	DEFVALB	07
INTCAPA	08	INTCONA	08
GPIOA	09	INTCONB	09
OLATA	0A	IOCON	0A
IODIRB	10	IOCON	0B
IPOLB	11	GPPUA	0C
GPINTENB	12	GPPUB	0D
DEFVALB	13	INTFA	0E
INTCONB	14	INTFB	0F
IOCON	15	INTCAPA	10
GPPUA	16	INTCAPB	11
INTFB	17	GPIOA	12
INTCAPB	18	GPIOB	13
GPIOB	19	OLATA	14
OLATB	1A	OLATB	15

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Using #defines to Make the Addresses and Control Bytes Easier to Recognize

```
// Defines for GIO, b1 means when 8-bit mode, BANK = 1
#define IOCONaddr_b0    0x0A    // address at reset, default 16-bit mode
#define IOCONaddr_b1    0x05
#define IODIRAaddr_b1   0x00
#define IODIRBaddr_b1   0x10
#define GPPUAaddr_b1    0x06
#define GPIOAaddr_b1    0x09
#define OLATBaddr_b1    0x1A
#define WRITE_opcode    0x40
#define READ_opcode     0x41
```

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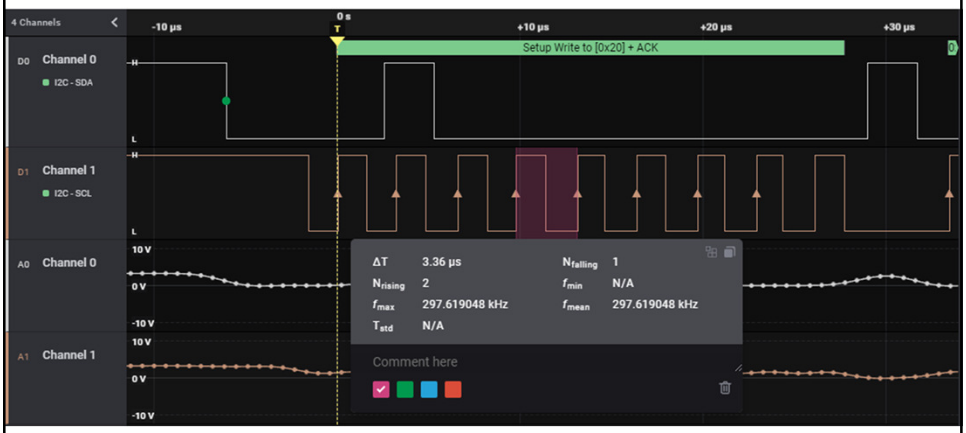
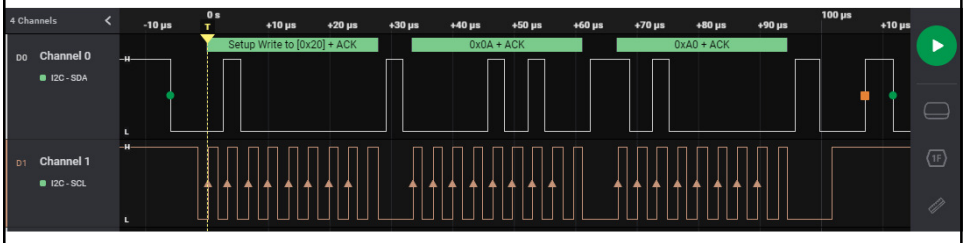
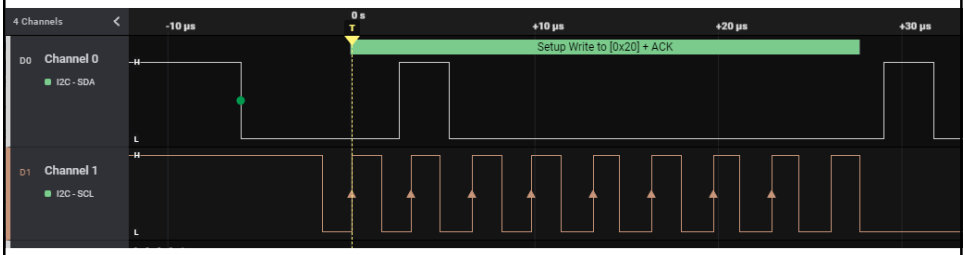
BAUD = 0; Frequency = 297.6 kHz



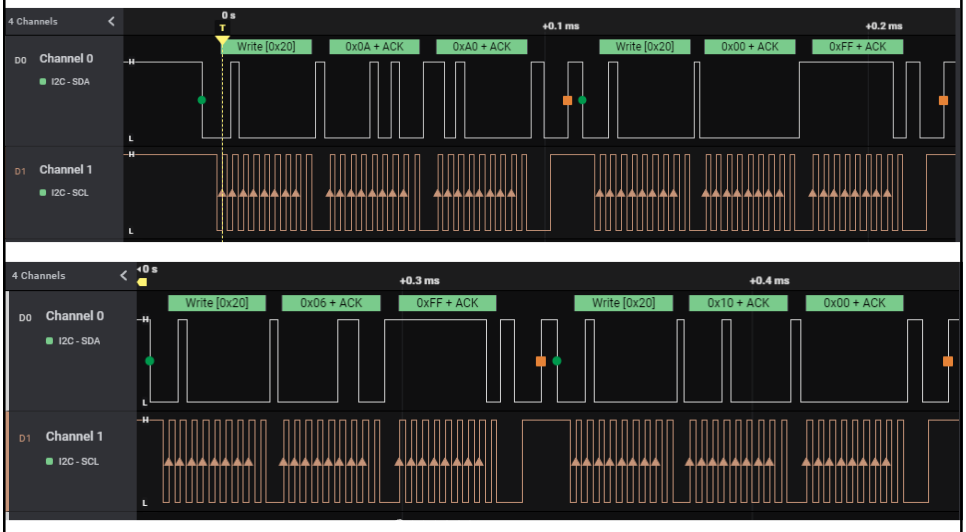
First I2C Transaction Between Master and Slave – Writing IOCON



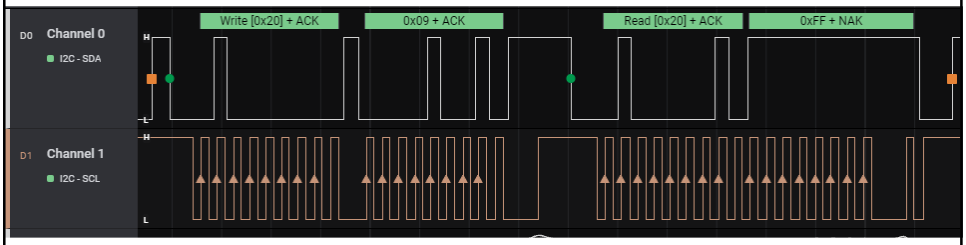
Writing IOCON Zoomed



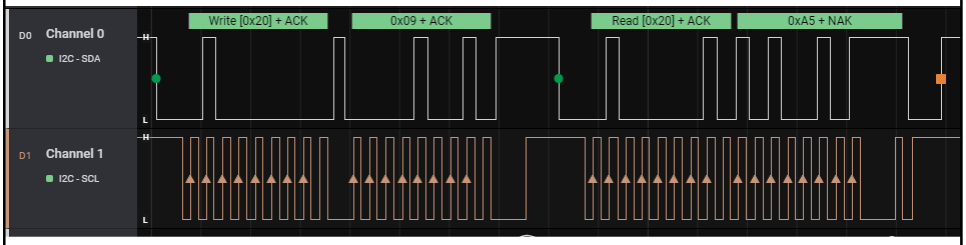
Initialization of MCP23017



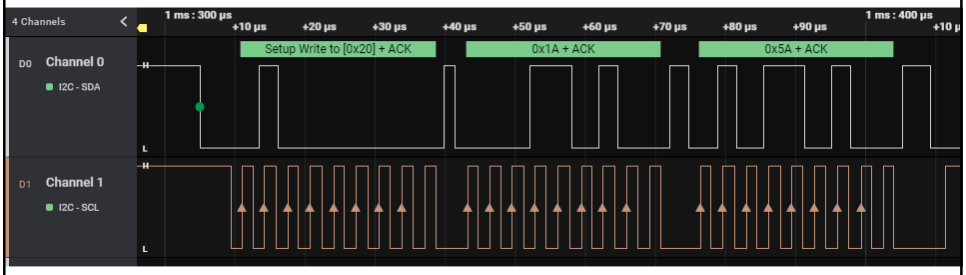
Reading Switches – 0xFF



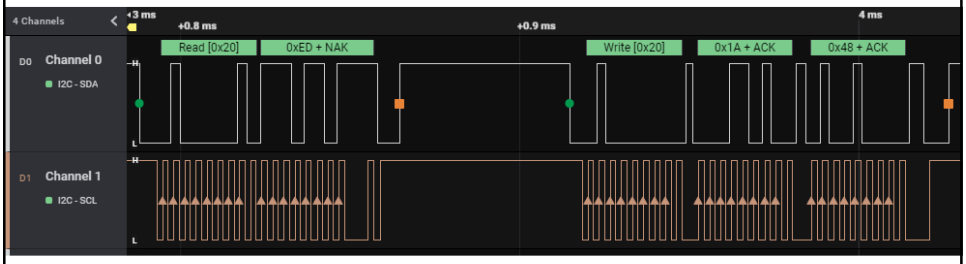
Reading Switches – 0xA5



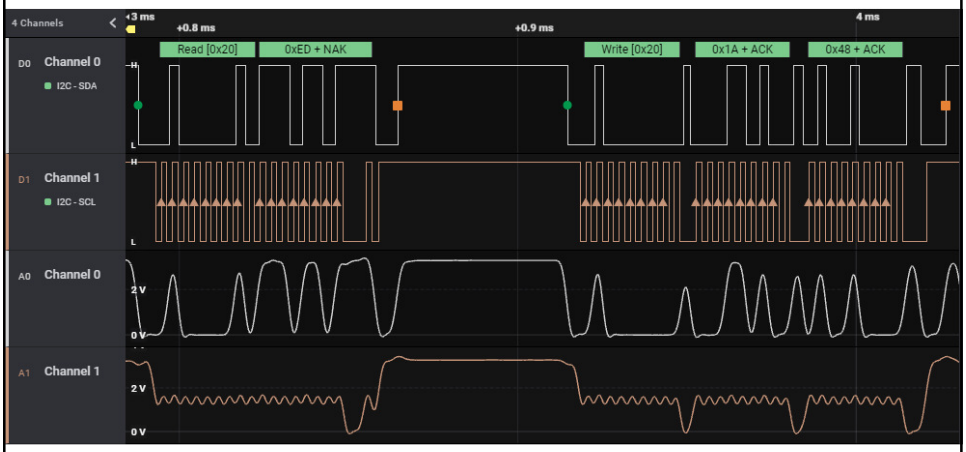
Writing Reversed Data to Bargraph – 0xA5



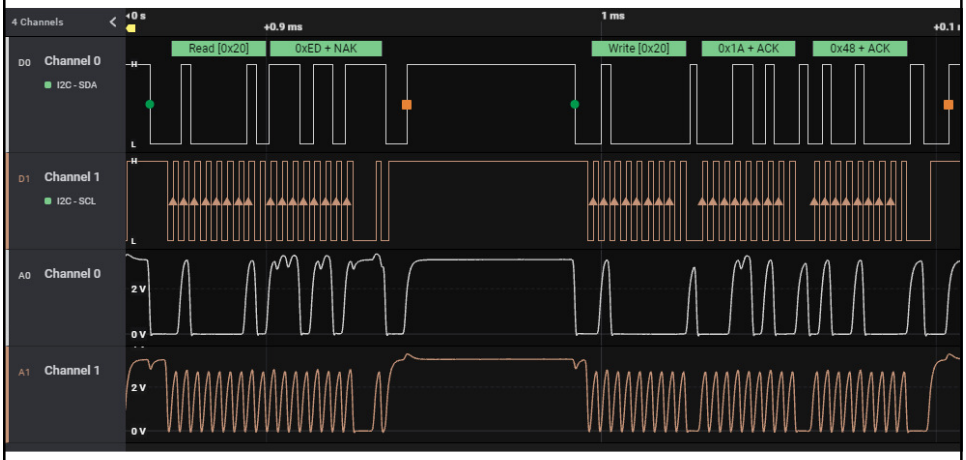
Reading Switches – 0xB7



Reading Switches Transaction – Digital and Analog Measurements 1.56 MS/s



Reading Switches Transaction – Digital and Analog Measurements 6.25 MS/s



Relative Rise and Fall Times

Trying to Measure Rise Time with Rpu = 19.5 kohm