# Serial Digital Data Networks

*This table provides top-level characteristics for serial interface standards by which two or more digital devices can be connected for communication. Design engineers can use the table to compare interface options for their application based on the design constraints like number of signal lines, network size, speed, distance, noise immunity, fault tolerance and reliability.*

Dallas Semiconductor offers 1-Wire® serial protocol to designers interested in implementing a low-cost, minimal contact interface. A key benefit provided with this low-cost, master/slave architecture is the delivery of slave-device power on the same line used for digital communication. A 1-Wire master can easily be implemented on a microcontroller unit (MCU) with only a single I/O pin by using software. Bridge chips for $I^2C$*, UART serial (RS-232), and USB-to-1-Wire are also available that off-load host-side 1-Wire protocol implementation and provide optimized 1-Wire waveform characteristics.

| | 1-Wire | $I^2C$* | SMBus™ | SPI™ | MicroWire/PLUS™ | M-Bus (EN1434) | CAN (ISO11898) | LIN Bus |
|---|---|---|---|---|---|---|---|---|
| Network Concept | single master, multiple slaves | multiple masters, multiple slaves | multiple masters, multiple slaves | single master, multiple slaves | single master, multiple slaves | single master, multiple slaves | multiple masters, multiple slaves | single master, multiple slaves |
| Number of Signal Lines | 1 (IO) | 2, (SCL, SDA) | 2, (SMBCLK, SMBDAT) | 4, (CS\, SI, SO, SCK) | 4, (CS\, DI, DO, SK) | 2 (lines can be swapped) | 2 (CAN_H, CAN_L, terminated) | 1 (LIN) |
| Optional signals | N/A | N/A | SMBSUS#, SMBALERT# | N/A | N/A | N/A | 2nd GND, Power, Shield | N/A |
| Network Size | Up to 300 m (with suitable master circuit) | Limited by max. 400pF bus capacitance requirement | Limited by max. 400pF bus capacitance requirement | N/A (circuit board level) | N/A (circuit board level) | Max. 350m per segment of max. 250 slaves; max. 180nF | 40m @1M bps1000m @ 50k bps (example) | Up to 40m, max. 10nF total load |
| Network Interface | open drain, resistive or active master pull-up | open drain, resistive or active master pull-up | open drain, resistive or active master pull-up | Push-pull with tristate | Push-pull with tristate | M to S: voltage drive S to M: current load | Differential open drain/source or open coll./emitter | open drain, resistive master pull-up |
| Network Voltage | From 2.8 to 6.0 V, device specific | From 1.8 to 5.5V, device specific | 2.7V to 5.5V | From 1.8V to 5.5V, device specific | From 1.8V to 5.5V, device specific | ~40V | $V_{DD}$-VD (diode drop); ~4.5V max. | 8 to 18V |

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|---|---|---|---|---|---|---|---|---|
| Logic Thresholds | Vary with network voltage | Fixed level: >1.5V, >3.0 V $V_{DD}$-related level: <30%, >70% of $V_{DD}$ | <0.8V, >2.1V | $V_{DD}$-related level: <20% (30%), >70% of $V_{DD}$ (inconsistent) | Fixed level: <0.8V, >2.0V; $V_{DD}$-related level: <20% (30%), >70% (80%) of $V_{DD}$ (inconsistent) | Master to slave: 24V, 36V nominalSlave to master: <1.5mA, >11mA | Differential: <50mV (recessive), >1.5V (dominant); driver specification | $V_{DD}$-related level: <20%, >80% of $V_{DD}$ (driver spec.)<40%, >60% of $V_{DD}$ (receiver spec.) |
| Transmission | LS bit first, half-duplex | MS bit first plus Acknowledge bit, half-duplex | MS bit first plus Acknowledge bit, half-duplex | MS bit first, full-duplex | MS bit first, full-duplex | LS bit first, half-duplex, acknowledge response | MS bit first, half-duplex | LS bit first, half-duplex |
| Address Format | 56 bits | 7 bits, (10 bits defined but not implemented) | 7 bits, (10 bits defined but not implemented) | N/A | N/A | 8 bits (primary address), 64 bits (secondary address) | Message identifier 11 bits (standard format), 29 bits (extended format) | Message identifier 8 bits, including 2 parity bits |
| Network Inventory | Automatic, supports dynamic topology change | N/A; slave addresses hard-coded in firmware | ARP, Address Resolution Protocol (Rev. 2.0 only) | N/A; slave select (CS\) hard-coded in firmware | N/A; slave select (CS\) hard-coded in firmware | Automatic | N/A; message-based protocol, not address based | N/A; message-based protocol, not address based |
| Gross Data Rate | Standard: ~0 to 16.3k bps Overdrive: ~0 to 142k bps) | Standard: ~0 to 100k bps; Fast: ~0 to 400k bps; High-Speed: ~0 to 3.4M bps | 10k to 100k bps | ~0 to ~10 M bps (device specific) | ~0 to ~5 M bps (device specific) | 300, 2400, 9600 bps | ~0 to 1M bps | ~1k to ~20k bps |
| Access Time | Standard: ~ 5.4ms Overdrive: ~0.6ms (at maximum speed) | Standard: ~95µsFast: ~23µs(at maximum speed) | ~95µs @ 100k bps | N/A | N/A | Primary address, 2400 bps: 13.75ms (short frame), 27.5ms (long frame) | At 1M bps 19µs (standard) or 39µs (extended) from start of frame to 1st data bit | At 20k bps 1.7ms from start of frame to 1st data bit |
| Data Protection | 8-bit and 16-bit CRC | N/A | PEC Packet Error Code (Rev.1.1, 2.0) | N/A | N/A | Even parity, check sum, frames | 15-bit CRC, frames, frame acknowledge | Check sum, frames |
| Collision Detection | Yes, through non-matching CRC | Yes (multi-master operation only) | Yes (Rev. 2.0 only) | N/A | N/A | Yes ("medium" and "strong" collisions) | Yes: CSMA/CD | Yes, through check sum |
| Slave supply | Parasitic (typical), $V_{DD}$ (exception) | $V_{DD}$ only | $V_{DD}$ only | $V_{DD}$ only | $V_{DD}$ only | Parasitic and/or local supply | $V_{DD}$ only, local or remote source | Parasitic only |

*Purchase of $I^2C$ components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a

**More Information**

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|---|---|---|---|
| DS2401: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2408: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2431: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2432: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2480B: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2490: | QuickView | Full (PDF) Data Sheet | Free Samples |
| DS2502: | QuickView | Full (PDF) Data Sheet | Free Samples |