**Design Task 3:** My way of verifying whether changing CLK_OUT using the main clock prescaler also changes CLK_CPU is by setting a delay using an avr-libc delay function that toggles between for 1Hz. Then I can start with CLK_OUT where I use default frequency of 4 MHz with prescaler and then I can record the CLK_CPU frequency from what was done from avr-libc delay function generated in my chosen output I/O pin which has LED0 as the output. Then I will use a different prescaler value to change the clock frequency at CLK_OUT. Then I will observe if there's any change in the frequency generated from the avr-libc delay function compared to before. This will help me determine whether changing CLK_OUT using the main clock prescaler also changes CLK_CPU generated from the delay functions by observing whether the LED0 blinks normally or if it blinks faster or slower than normal. I can even measure based on whether the CLK_CPU changed using an oscilloscope by observing my chosen I/O pin.

**Design Task 4:** My way of verifying on the toggle bit at one of three different rates: every 52.08333, 104.1666, or 208.333 us is to rely on the oscilloscope at one of the I/O pin that I want to output one of three different rate. In this case, since I configured PC3 as my output pin where I want to check my toggle rate, I will turn on and off either two of the DIP switches to verify whether my corresponding 3 pulse widths to be outputted are correct by observing from the oscilloscope.

**Design Task 5:** My way of verifying whether the output frequency output is correct is by relying on the oscilloscope where I will be able to check on the waveform output from PA7. Then I will be able to configure whether the displayed approximate frequency on the oscilloscope is mainly correct or not as it should by seeing if it's approximately closed to 32.768 kHz.