

**Design Task 1:** The way that I will verify for design task 1 is by using the Saleae Logic Analyzer where I will place one of the probes of one of the channels into PB0 (TX pin). I will then be able to then verify if my program works by seeing if the character that is to be transmitted is actually transmitted by seeing if the Tera Term terminal displays the character continuously. This would mean the ASCII character transmitted was successful. Also I will verify that the bit time is correct by measuring the toggle time between each of the 8 bits that is part of the ASCII character that is displayed on the Saleae Logic Analyzer waveform output. After that, the 1 ms delay will be verified by measuring the timeframe between when all the bits of that same ASCII character are done being transmitted and when all the bits of that same ASCII character are going to be transmitted.

**Design Task 2:** The way that I will verify for design task 2 is by using the Saleae Logic Analyzer where I will place one of the probes of one of the channels into PB1 (RX pin). I will then be able to then verify if my program works by seeing if the character that is to be received is actually received. This will be done by actually entering the ASCII character into Tera Term and seeing if it was transmitted by seeing the Saleae Logic Analyzer waveform output that is connected to the RX pin. If it displays after I type in a character into a Tera Term terminal and there is a sample output of that character displayed in the waveform, it shows that character has successfully been transmitted.

**Design Task 3:** The way that I will verify for design task 3 is by using the Saleae Logic Analyzer where I will place one of the probes of one of the channels into PB1 (RX pin). I will then be able to then verify if my program works by seeing if the character that is to be received is actually received. This will be done by actually entering the ASCII character into Tera Term and seeing if it was transmitted by seeing the Saleae Logic Analyzer waveform output that is connected to the RX pin. If it displays after I type in a character into a Tera Term terminal and there is a sample output of that character displayed in the waveform, it shows that character has successfully been transmitted. This is pretty similar to task 2 except I'm using interrupts as another approach.

**Design Task 4:** The way I will verify for design task 4 is by using a Saleae logic analyzer where I will use two channel probes. One will be placed for PB0 (TX pin) and another will be placed for the PB1 (RX pin). I will then type the character as long as it's lowercase into Tera Term terminal which will then be received. Then I will check on the PB1 (RX pin) with the Saleae logic analyzer waveform output to see if it displayed the correct corresponding character as an uppercase letter which will tell me my program works successfully for task 4.

**Design Task 5:** The way I will verify for design task 5 is by using a Saleae logic analyzer where I will then type in a line of ASCII characters (80 max) into Tera Term and pass it to the PB1 (RX pin). And I will verify if those series of characters are received by seeing the waveform of that channel connected to the RX pin. If successfully received, I will then be able to verify if those characters are successfully displayed into the Tera Term terminal after transmission. Also I will test the case where if I enter the carriage character in a series of ASCII characters, I will see if the cursor actually goes into the new line of the Tera Terminal using the Tera Term.