

## Laboratory 03: Clock Control Module CLKCTRL and Software Delays

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Prof. Ken Short

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## Laboratory 03 Laboratory Tasks

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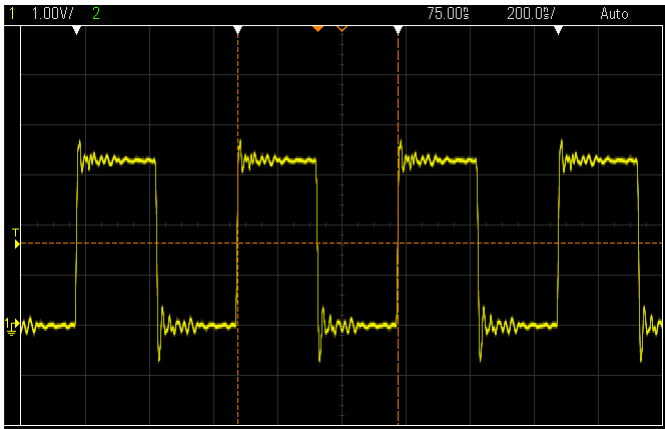
- ❑ Design Task 1: Generating a Clock Frequency at CLKOUT (PA7).
- ❑ Design Task 2: Determining Whether Changing CLK\_OUT (or CLK\_PER) Using The Main Clock Prescaler Also Changes CLK\_CPU.
- ❑ Design Task 3: Toggling a Bit Every 52.08, 104.16, and 208.33 us Using an avr-libc Library Function.
- ❑ Design Task 4: 32.768 kHz CLK\_MAIN.

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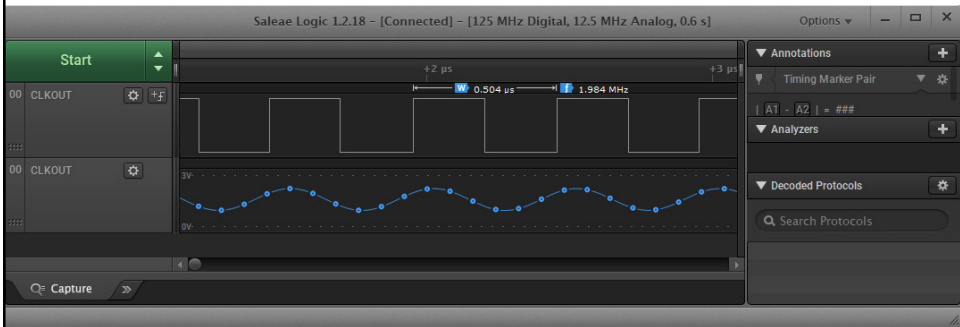
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MSO-X 3012A Looking at 2 MHz CLKOUT



Saleae Logic 1.x Looking at 2 MHz CLKOUT



Saleae Logic 2.x Looking at 2 MHz CLKOUT (Alpha Version)



Timing Markers

- P0 → Δ280 ns
- 0-A = 359.9448 ms
- 0-B = 359.94508 ms

Measurements

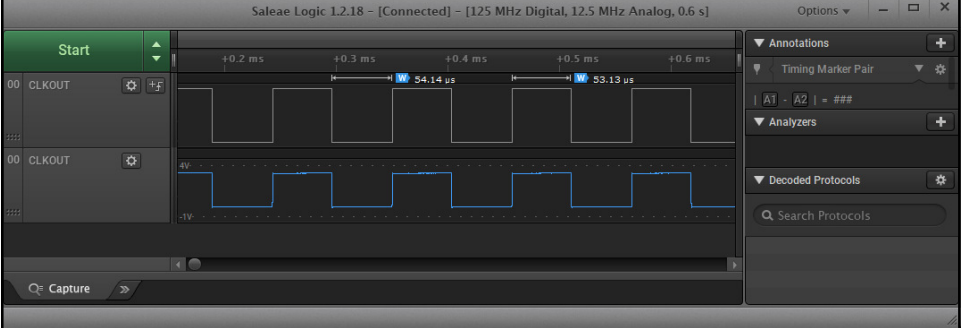
Session 0 x + 160 ns

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Saleae Logic 1.x Looking at Toggling Every 52 us



Annotations

- Timing Marker Pair
- A1 - A2 = ###

Analyzers

Decoded Protocols

Search Protocols

Capture

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