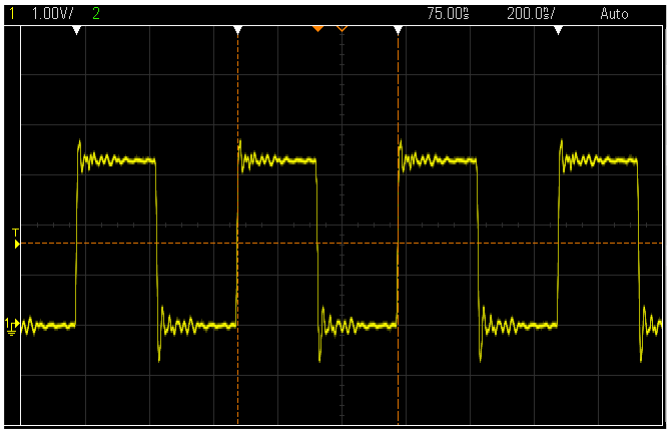
Laboratory 03: Clock Control Module CLKCTRL and Software Delays

Prof. Ken Short

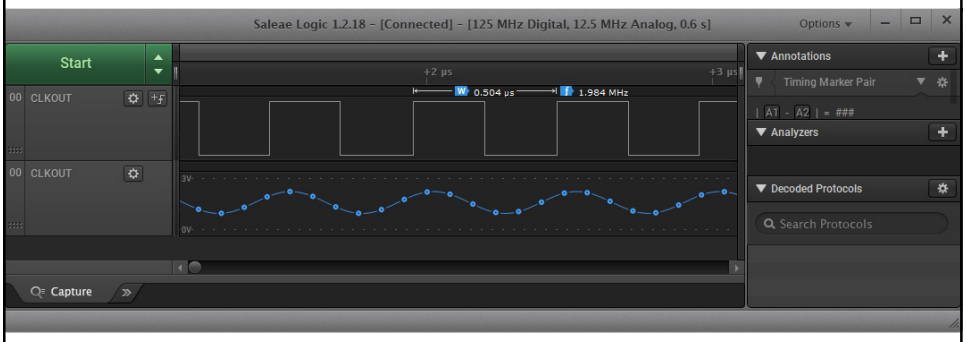
Laboratory 03 Laboratory Tasks

- Design Task 1: Generating a Clock Frequency at CLKOUT (PA7).
- Design Task 2: Determining Whether Changing CLK_OUT (or CLK_PER) Using The Main Clock Prescaler Also Changes CLK_CPU.
- Design Task 3: Toggling a Bit Every 52.08, 104.16, and 208.33 us Using an avr-libc Library Function.
- Design Task 4: 32.768 kHz CLK_MAIN.

MSO-X 3012A Looking at 2 MHz CLKOUT

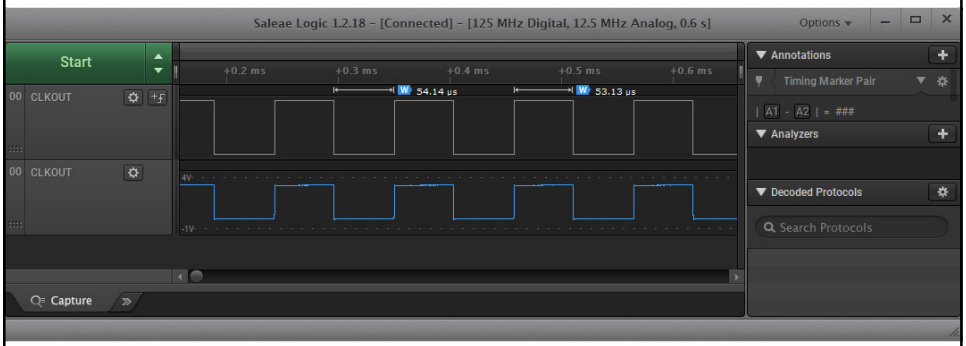


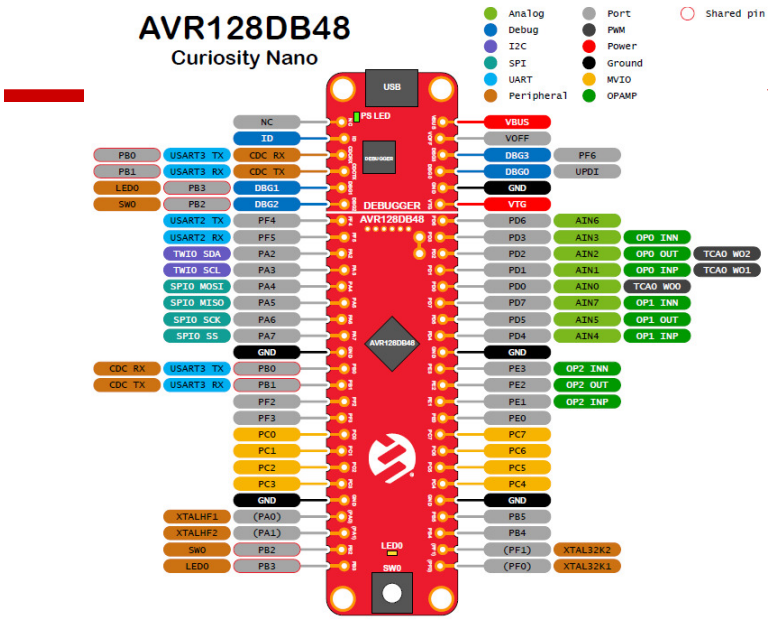
Saleae Logic 1.x Looking at 2 MHz CLKOUT



Saleae Logic 2.x Looking at 2 MHz CLKOUT (Alpha Version)

Saleae Logic 1.x Looking at Toggling Every 52 us





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