

## Laboratory 05: AVR128DB48 USART Module in Asynchronous Serial (RS232) Mode and Saleae Logic Analyzer

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2/27/2022

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### Overview

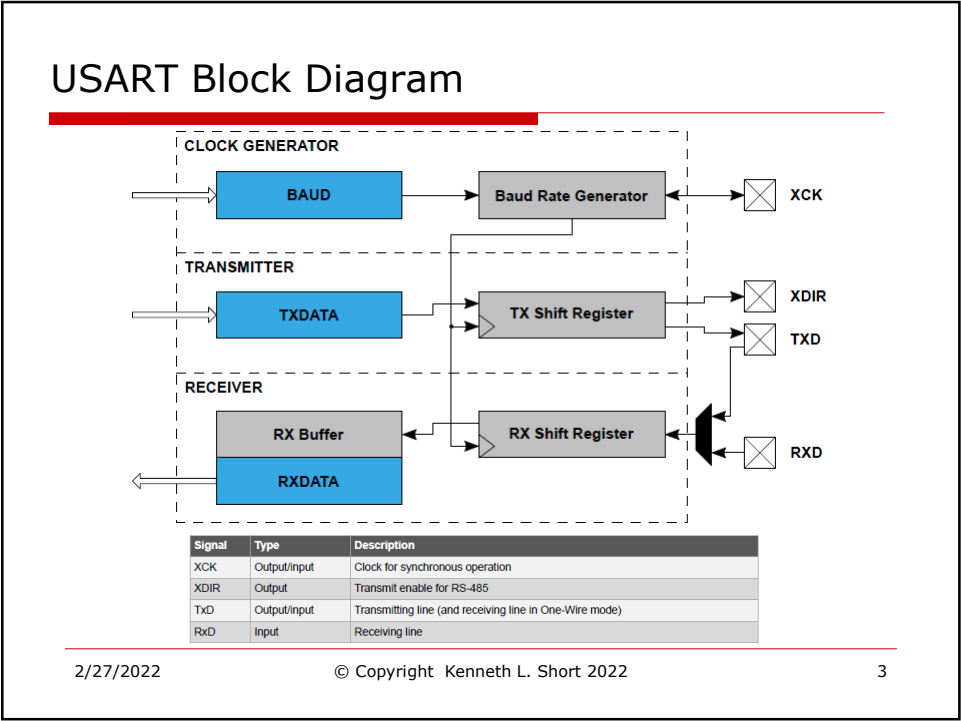
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- ❑ The AVR128DB48 has five USART modules for serial asynchronous and synchronous communication.
- ❑ These USARTs can be configured to achieve serial communications using the asynchronous (RS232) protocol.
- ❑ The lecture notes and the assigned reading from the AVR128DB48 Data Sheet provide details on the USART's asynchronous serial operation.

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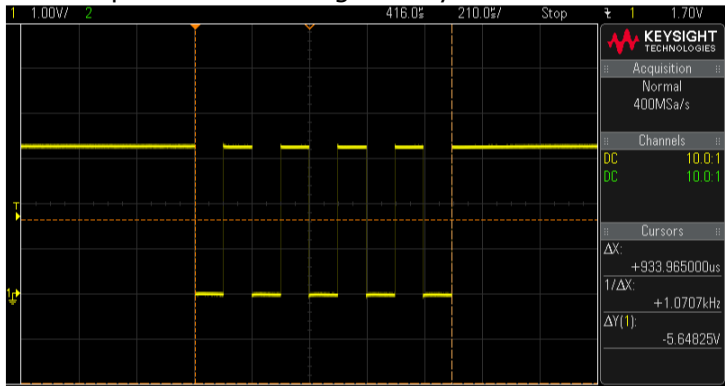
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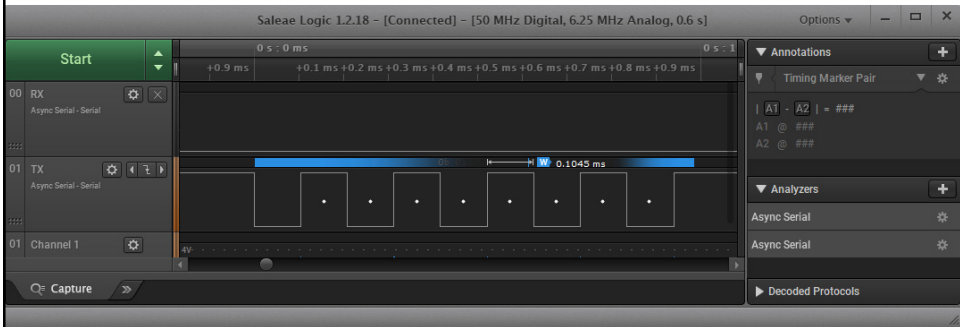
- Desgin Tasks
- ❑ Design Task 1: Using USART3 to Transmit a Single Character and Using the Saleae Logic Analyzer to Verify the Transmission.
  - ❑ Design Task 2: Using USART3 to Transmit Characters A to Z via Asynchronous Serial.
  - ❑ Design Task 3: Loopback of Tx to Rx.
  - ❑ Design Task 4: Echo of Characters Sent by a PC Using a USB Port.
  - ❑ Design Task 5: Echo of Characters Sent by a PC Using an Actual RS232 Port.
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Design Task 1: Using USART3 to Transmit a Single Character and Using the Saleae Logic Analyzer to Verify the Transmission.

- Write a program named USART3\_async\_test. This program transmits a single character each time it is run. The character transmitted is observed using both the oscilloscope and Saleae logic analyzer.



Saleae Logic Analyzer



## A screenshot of a Tera Term VT window titled "COM7 - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main area displays a grid of ASCII characters arranged in approximately 20 rows and 30 columns. The first column contains uppercase letters A through Z, followed by a blank space. Subsequent columns contain various symbols and characters, including digits, punctuation, and control characters like carriage return and line feed. The bottom status bar shows the date "2/27/2022", copyright information "© Copyright Kenneth L. Short 2022", and the page number "7".

Saleae Logic 1.2.18 - [Connected] - [50 MHz Digital, 6.25 MHz Analog, 0.6 s]

Options ▾

Start

0 s : 0 ms

00 RX Async Serial - Serial

01 TX Async Serial - Serial

01 Channel 1

Q Capture

Annotations

Timing Marker Pair

A1 - A2 | = ###

A1 @ ###

A2 @ ###

Analyzers

Async Serial

Async Serial

Decoded Protocols

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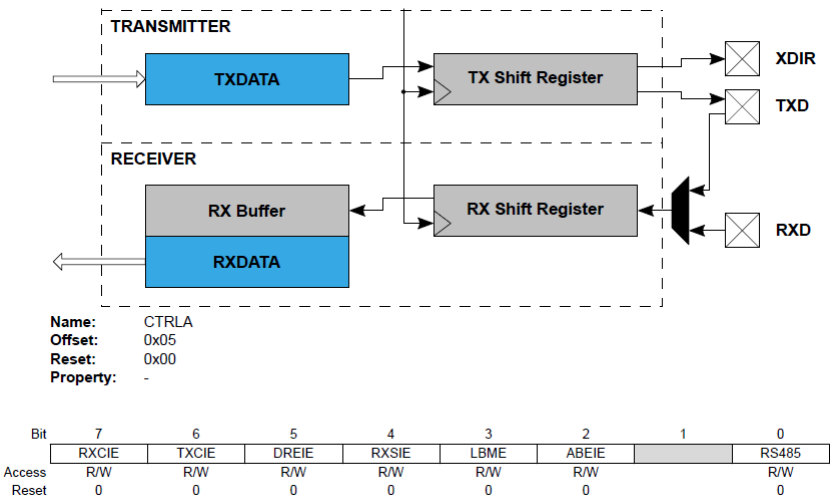
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### Design Task 3: Loopback of Tx to Rx

- ❑ One simple way to check whether a serial communications design works is to connect the transmitting line directly to the receiving line. This is called a loopback test.
- ❑ Normally, you would simply connect USART’s Tx signal to its Rx signal. That way any character sent by your program should be received by your program.
- ❑ However, since we are using USART3 and its RX and TX pins are also connected to the Curiosity’s Virtual Serial Port (CDC) we cannot do this.
- ❑ Instead you must use the Loop-back Mode Enable (LBME) feature of the UART module that enables an internal connection between the TXD pin and the USART’s receiver and the RX input pin of the USART receiver is disconnected. The LBME bit is in CTRLA.

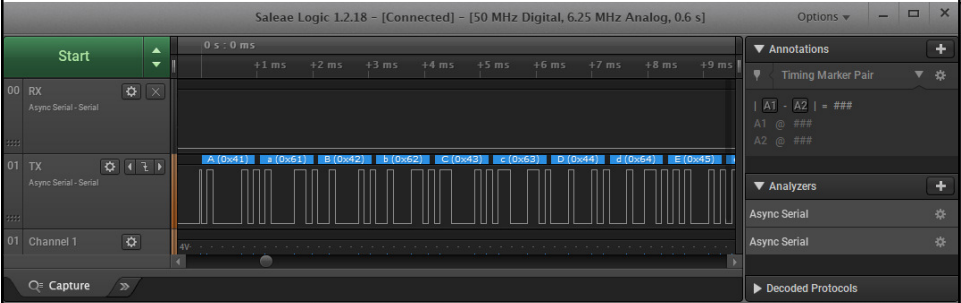
### Loop Back Mode (LBM) Inside the AVR128DB48



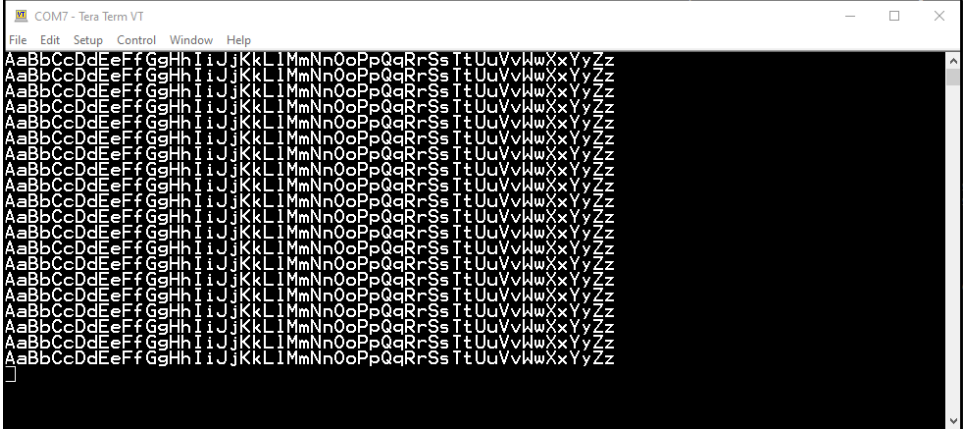
### Repeatedly Streaming A to Z With Each Character Followed By Its Lower Case Version



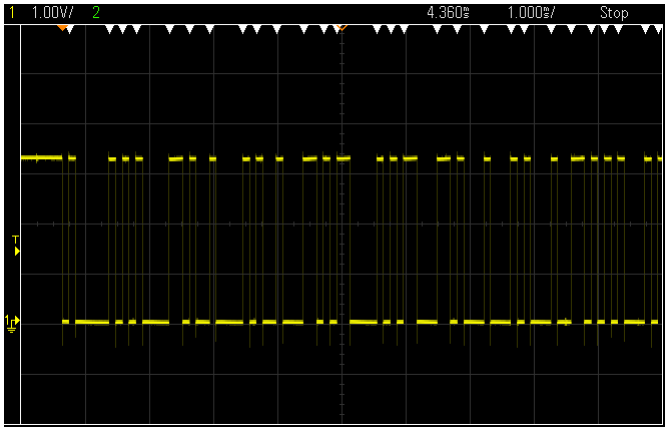
### A to Z With Each Character Followed By Its Lower Case Version on Saleae Logic Analyzer



### A to Z With Each Character Followed By Its Lower Case Version and Formatting Characters



### Why You Want a Protocol Aware Instrument



## Design Task 4: Echo of Characters Sent by a PC Using a USB Port.

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- This is similar to what you did with your software receiver and transmitter, only you are doing it in hardware using the USART.

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## Design Task 5: Echo of Characters Sent by a PC Using an Actual RS232 Port.

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- Instead of using the virtual port as in Design Task 4, you will be using an actual RS232 serial port on the back of the computer. This port is designed COM1 and is available using the DB9 connector on the back of the computer.
- You must use an Analog Devices ADM3202 Low Power, 3.3V, RS232 Line Drivers/Receivers IC to translate between COM1's RS232 logic levels and the Curiosity Nano board's 3.3V logic levels.

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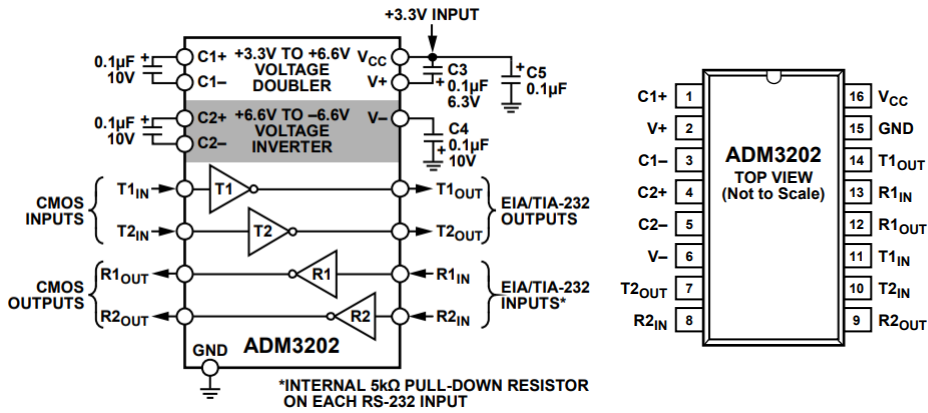
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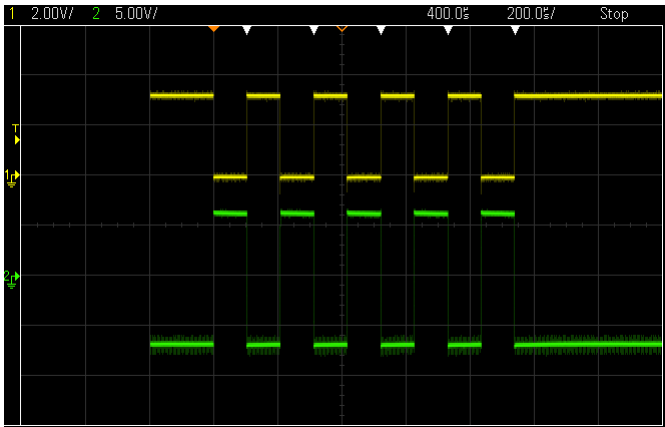
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## Analog Devices ADM3202 Low Power, 3.3 V, RS-232 Line Drivers/Receivers



## ADM3202 Driver Output



## ADM3202 Pin Function Description

Mnemonic	Description
V <sub>CC</sub>	Power Supply Input (3.3 V ± 0.3 V).
V+	Internally Generated Positive Supply (+6 V nominal).
V-	Internally Generated Negative Supply (−6 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+, C1-	External Capacitor 1 is connected between these pins. A 0.1 μF capacitor is recommended but larger capacitors up to 47 μF can be used.
C2+, C2-	External Capacitor 2 is connected between these pins. A 0.1 μF capacitor is recommended but larger capacitors up to 47 μF can be used.
TX <sub>IN</sub>	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels.
TX <sub>OUT</sub>	Transmitter (Driver) Outputs. These are RS-232 signal levels (typically ±9 V).
RX <sub>IN</sub>	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
RX <sub>OUT</sub>	Receiver Outputs. These are CMOS output logic levels.