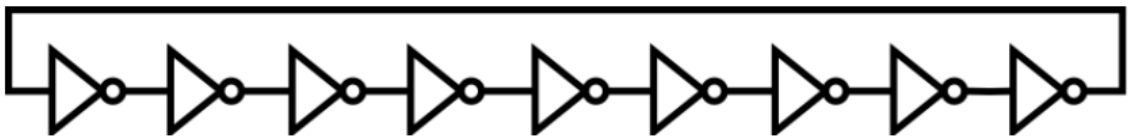
Jason Waseq
6/10/15

Digital Logic Breadboard: Ring Oscillator Timing Analysis & Edge-Triggered Flip-Flop Construction

Purpose of the Assignment:
This lab immerses you in hands-on digital logic design by having you build two fundamental circuits on a breadboard: a 9-stage ring oscillator to measure the propagation delay of discrete inverter gates, and an edge-triggered D flip-flop constructed from basic logic ICs. Through careful wiring, multimeter checks, and oscilloscope measurements, you'll quantify real-world gate delays and observe how signal transitions propagate through a feedback loop. In the flip-flop exercise, you'll implement and verify positive or negative edge triggering using minimal NAND/NOR gates or latch ICs, driving LEDs to indicate input and output states. Together, these tasks deepen your understanding of timing constraints, circuit layout best practices, and the dramatic convenience FPGAs offer compared to manual breadboarding.



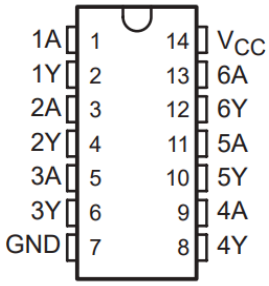
9-stage Ring Oscillator

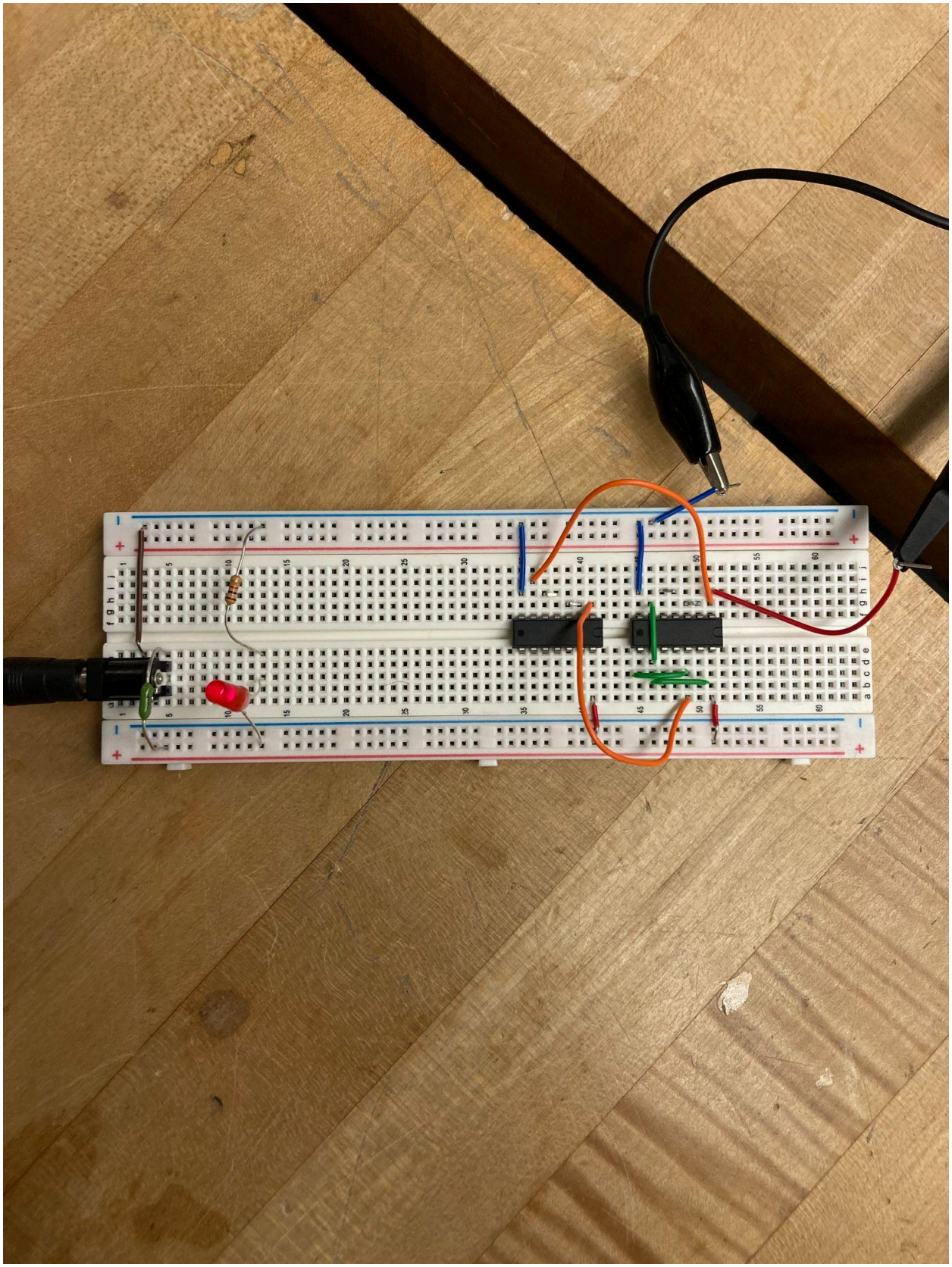
https://www.ti.com/lit/ds/symlink/sn74ls04.pdf?ts=1749997999793&ref_url=https%253A%252F%252Fwww.google.com%252F

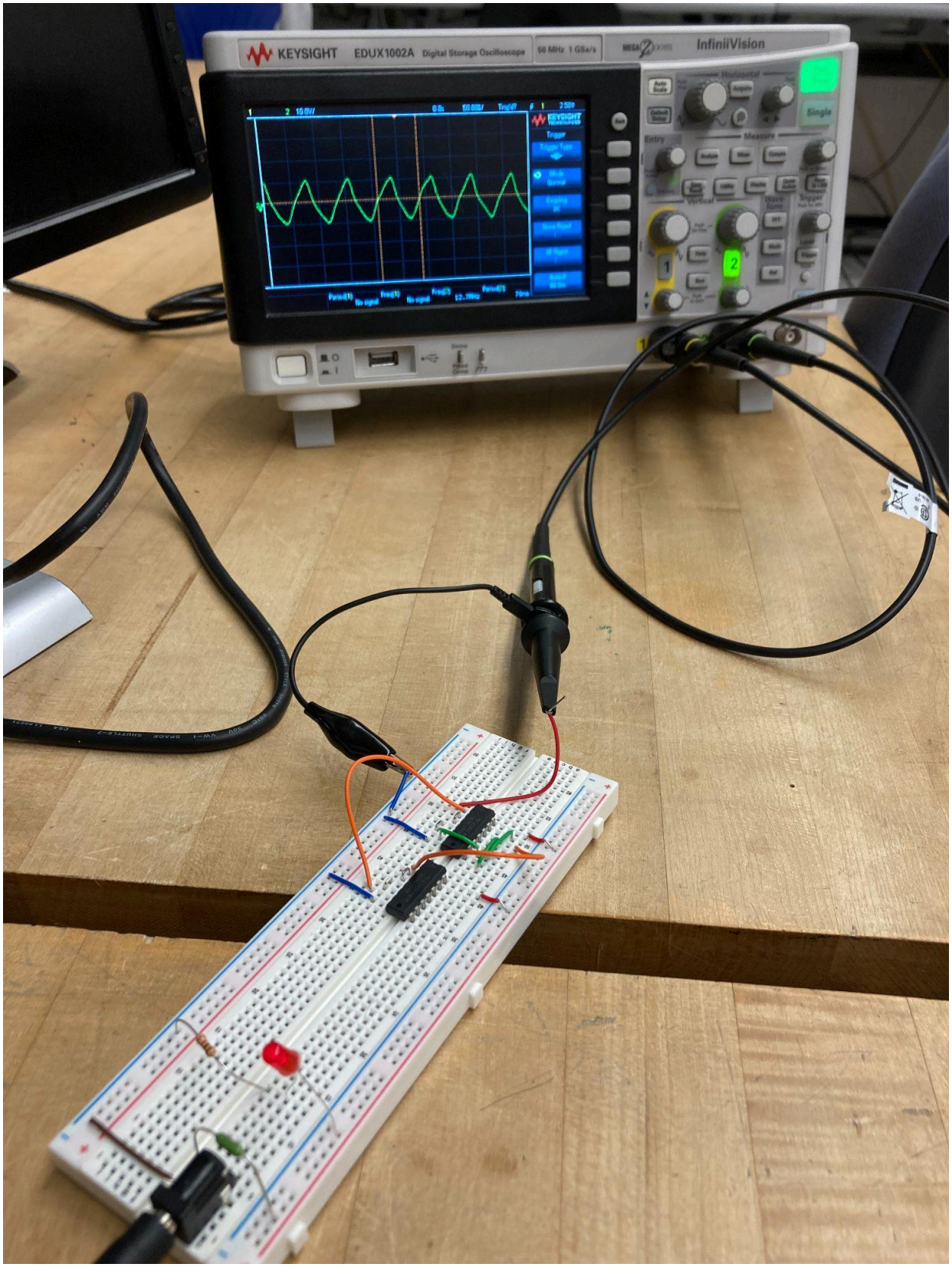
SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS

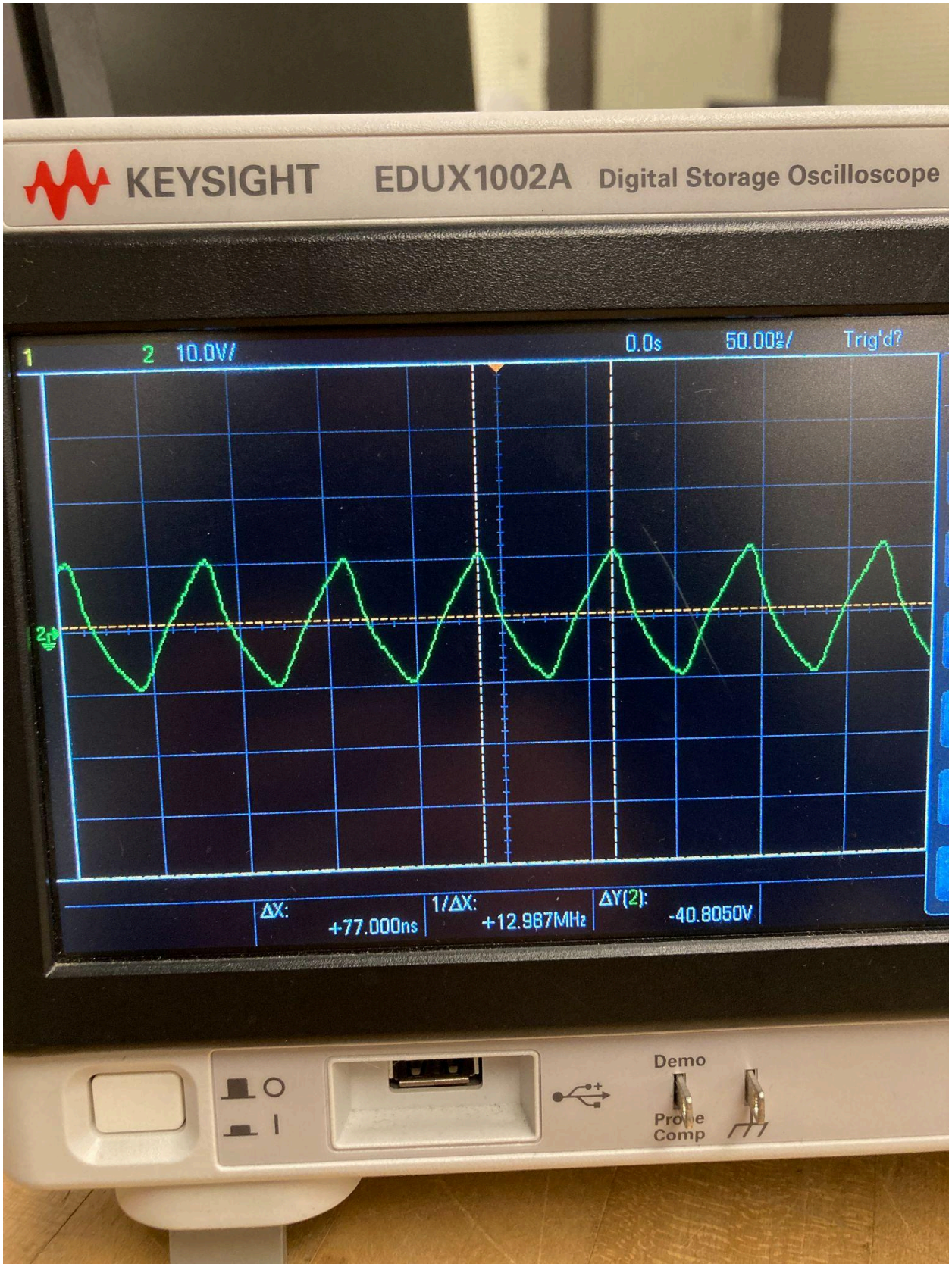
SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

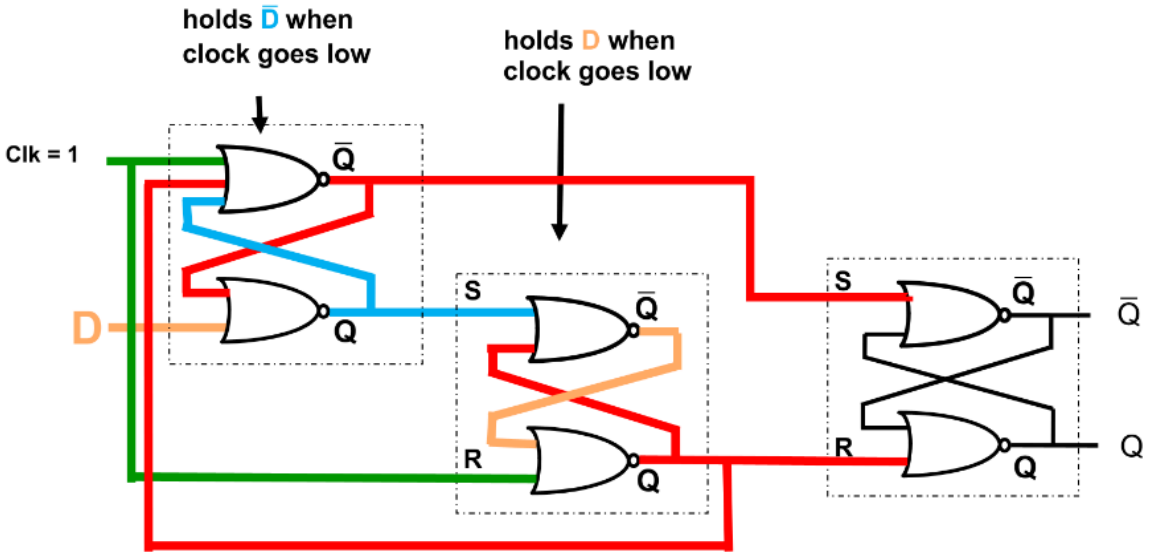





KEYSIGHT
EDUX1002A
Digital Storage Oscilloscope
50 MHz 1 GSa/s
InfiniiVision
Single



Propagation Delay = 77ns / (2 * 9) = 4.28ns



https://www.ti.com/lit/ds/symlink/sn5402.pdf?ts=1750012509793&ref_url=https%253A%252F%252Fwww.google.com%252F

SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE
(TOP VIEW)