Report HW 0 ECE-111

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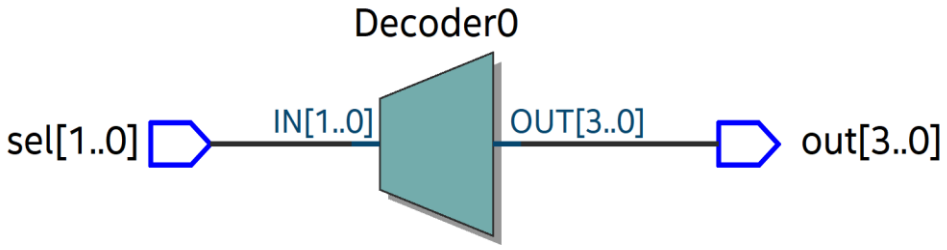
2-to-4 decoder

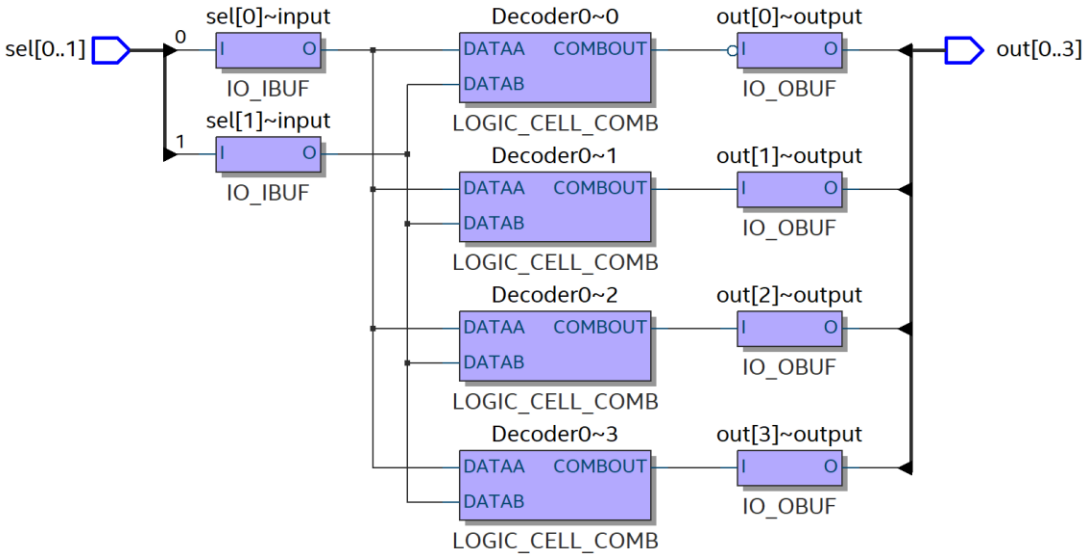
1. **Behavioral level**
   a. **SystemVerilog Code**

```
// 2to4 Decoder behavioral level code
module decoder_2to4_behavioral(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 always @(sel or out)
  begin
   case (sel)
    2'b00  : out = 4'b0001;

    // Student to add remainder of the code
    2'b01 : out = 4'b0010;
    2'b10 : out = 4'b0100;
    2'b11 : out = 4'b1000;
    default: out = 4'b0000;

   endcase
  end
endmodule
```

   b. **RTL Schematic**



c. Post mapping schematic



d. Resource Usage

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	2
2		
3	Combinational ALUT usage for logic	4
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
4		
5	Dedicated logic registers	0
6		
7	I/O pins	6
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	sel[0]~input
12	Maximum fan-out	4
13	Total fan-out	18
14	Average fan-out	1.13

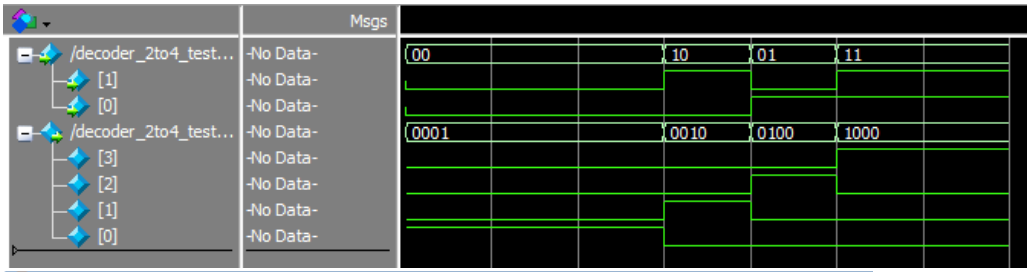
Number of ALUT: 4 (6 I/O pins)

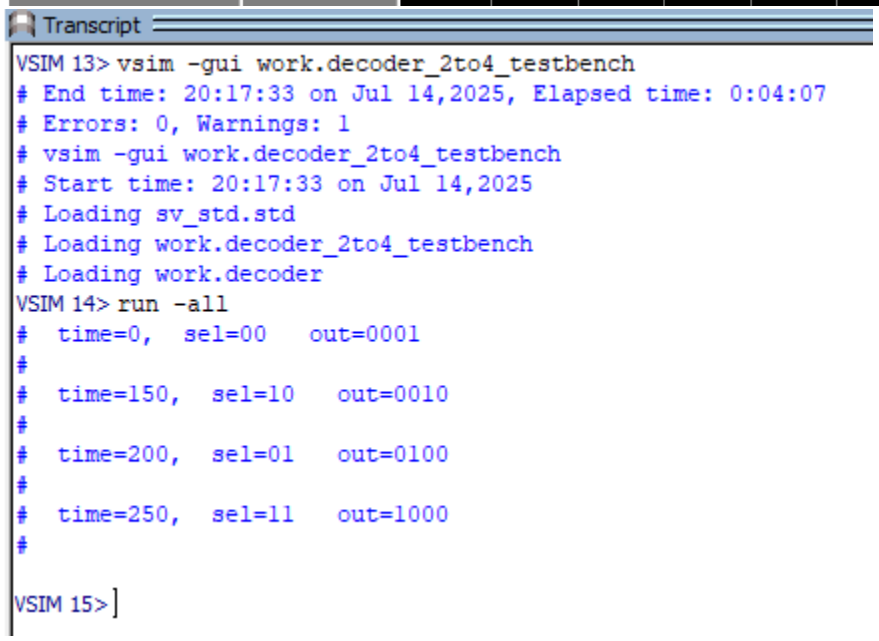
4 ALUTs each for the output, which there are 4 outputs

Number of Functions: 4 (2 input function)

Require 4 2-input function for each output (2 input for sel_0 sel_1)

e. Modelsim simulation results





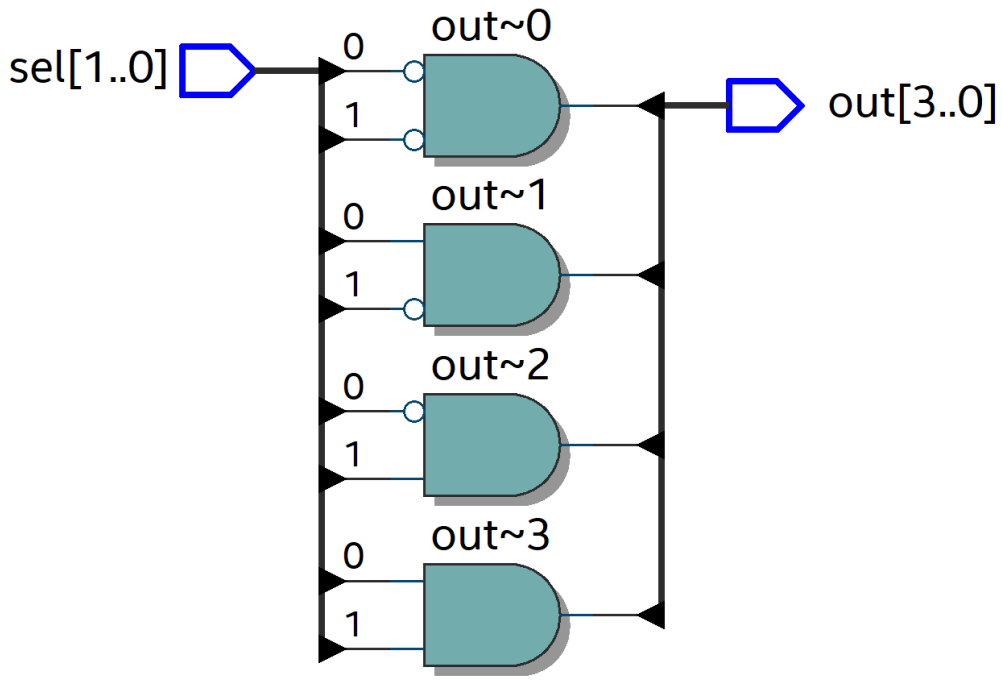
The decoder transform the 2 bit input into 1 in the corresponding position.

2. Dataflow level

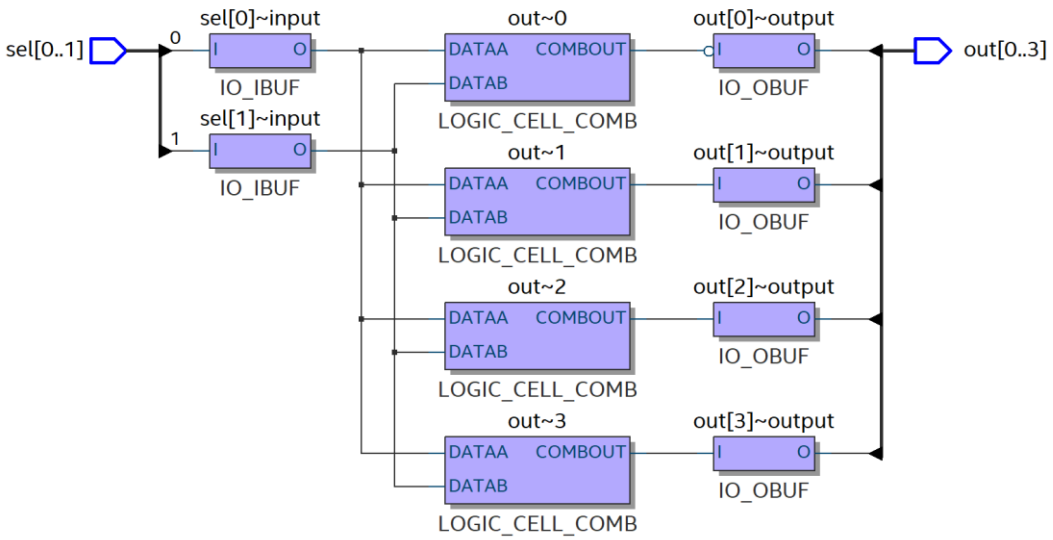
a. SystemVerilog Code

```
// 2to4 Decoder dataflow level code
module decoder_2to4_dataflow(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 assign out[0] = (!sel[0]) && (!sel[1]);
 // Student to add remainder of the assign statements
  assign out[1] = (!sel[1]) & sel[0];
  assign out[2] =  sel[1] & (!sel[0]);
  assign out[3] =  sel[1] &  sel[0];
endmodule
```

b. RTL schematic



c. Post mapping schematic



d. Resource usage

Analysis & Synthesis Resource Usage Summary

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3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
4		
5	Dedicated logic registers	0
6		
7	I/O pins	6
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	sel[0]~input
12	Maximum fan-out	4
13	Total fan-out	18
14	Average fan-out	1.13

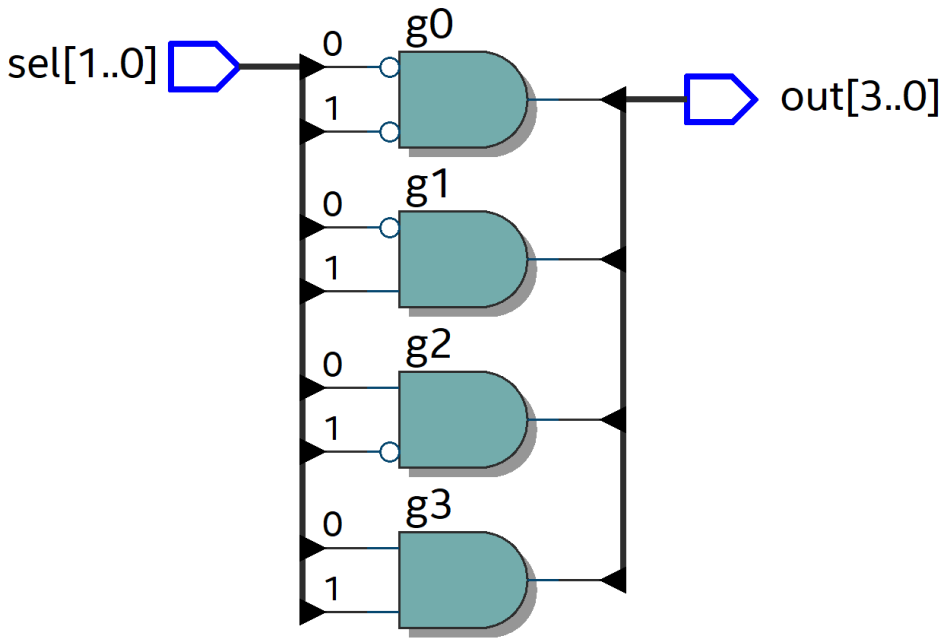
e. Modelsim simulation result (same as behavioral level simulation result)

3. Gatelevel

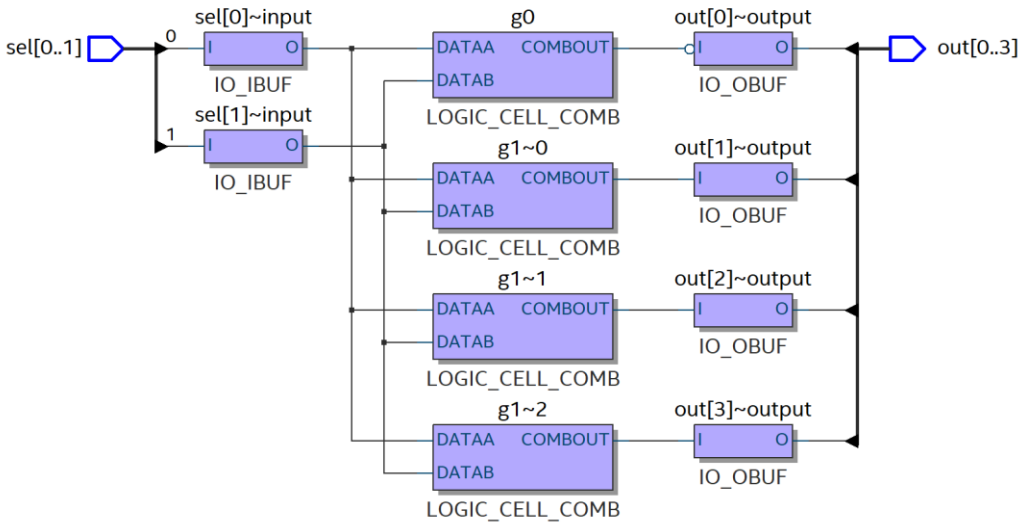
a. **SystemVerilog Code**

```
// 2to4 Decoder gatelevel code
module decoder_2to4_gate(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 wire w0, w1;
 not i0(w0, sel[0]);
 not i1(w1, sel[1]);
 and g0(out[0], w1, w0);
 and g1(out[1], sel[1], w0);
 and g2(out[2], w1, sel[0]);
 and g3(out[3], sel[1], sel[0]);
endmodule
```

b. **RTL schematic**



c. **Post mapping schematic**



d. Resource usage

Analysis & Synthesis Resource Usage Summary

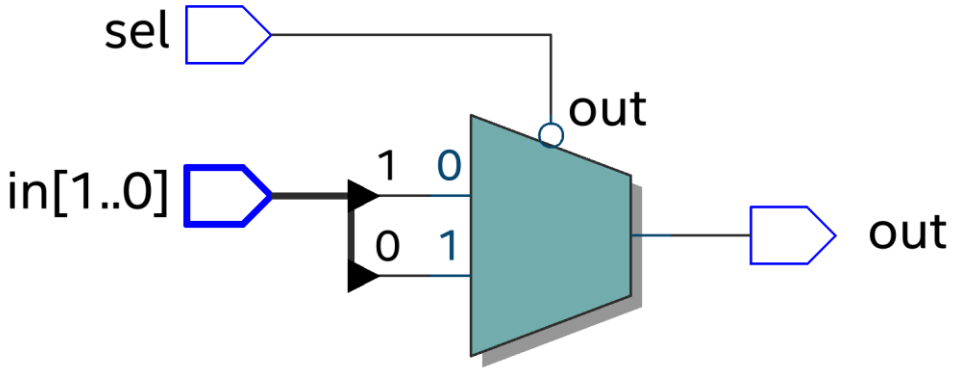
<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	2
2		
3	Combinational ALUT usage for logic	4
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
4		
5	Dedicated logic registers	0
6		
7	I/O pins	6
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	sel[0]~input
12	Maximum fan-out	4
13	Total fan-out	18
14	Average fan-out	1.13

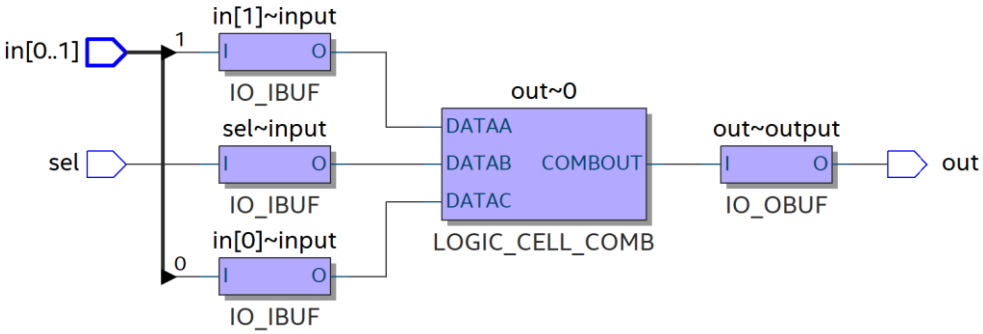
e. Modelsim simulation result (same as behavioral level simulation result)

2-to-1 Mux

1. **Behavioral level**
    a. **RTL schematic**



    b. **Post mapping schematic**



    c. **Resource usage**

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1
2		
3	Combinational ALUT usage for logic	1
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
4		
5	Dedicated logic registers	0
6		
7	I/O pins	4
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	out~0
12	Maximum fan-out	1
13	Total fan-out	8
14	Average fan-out	0.89

Number of ALUT: 1 (4 I/O pins)

2:1 MUX design need only one ALUT for the single output

Number of Functions: 1 (3 input function)

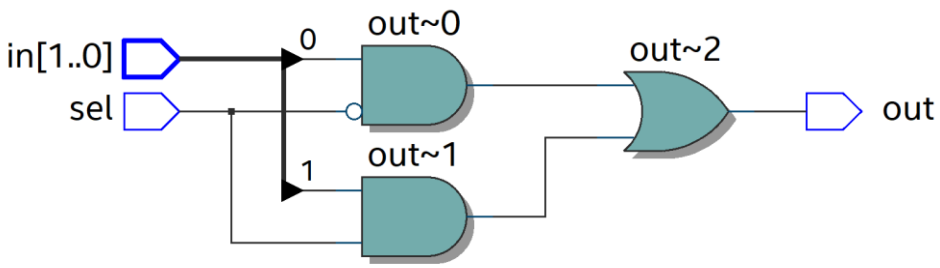
Require 1 3-input function for the single output, with 3 input in_0, in_1, and sel

d. Modelsim simulation result

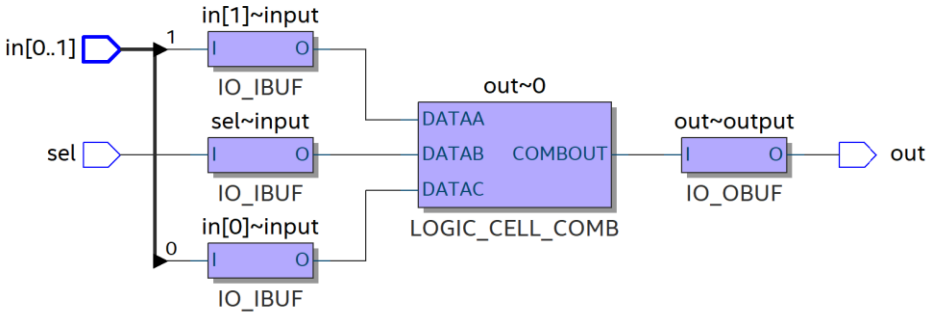
```
Transcript
# Start time: 20:46:27 on Oct 14,2025
# Loading sv_std.std
# Loading work.mux_2x1_testbench
# Loading work.mux_2x1
add wave -position end  sim:/mux_2x1_testbench/tb_in
add wave -position end  sim:/mux_2x1_testbench/tb_sel
add wave -position end  sim:/mux_2x1_testbench/tb_out
VSIM 39> run -continue
VSIM 40> run -all
#  time=0,   in=00  sel=0  out=x
#
#  time=2,   in=00  sel=0  out=0
#
#  time=150,   in=01  sel=0  out=0
#
#  time=152,   in=01  sel=0  out=1
#
#  time=200,   in=10  sel=0  out=1
#
#  time=202,   in=10  sel=0  out=0
#
#  time=250,   in=00  sel=1  out=0
#
#  time=300,   in=01  sel=1  out=0
#
#  time=350,   in=10  sel=1  out=0
#
#  time=352,   in=10  sel=1  out=1
#

VSIM 41>
```

The 2-to-1 mux choose one of the two value based on the select value 0 or 1.

2. **Dataflow level**
    a. **RTL schematic**



    b. **Post mapping schematic**



c. **Resource usage**

Analysis & Synthesis Resource Usage Summary

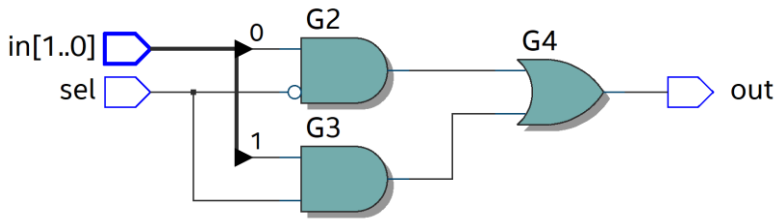
<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1
2		
3	Combinational ALUT usage for logic	1
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
4		
5	Dedicated logic registers	0
6		
7	I/O pins	4
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	out~0
12	Maximum fan-out	1
13	Total fan-out	8
14	Average fan-out	0.89

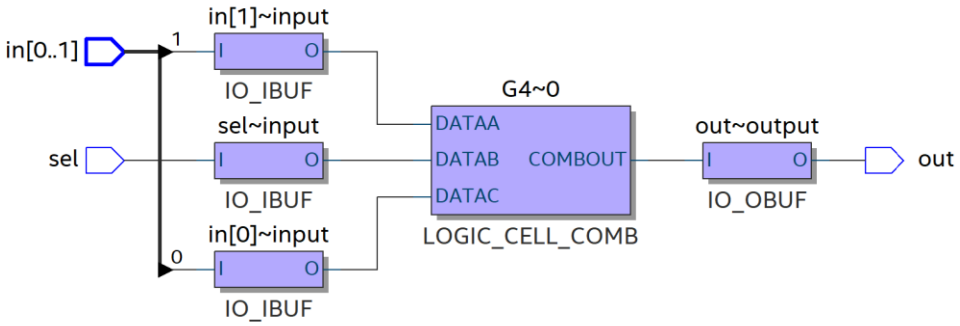
d. **Modelsim simulation result (same as behavioral level simulation result)**

3. **Gatelevel**

a. **RTL schematic**



b. Post mapping schematic



c. Resource usage

Analysis & Synthesis Resource Usage Summary

<<Filter>>

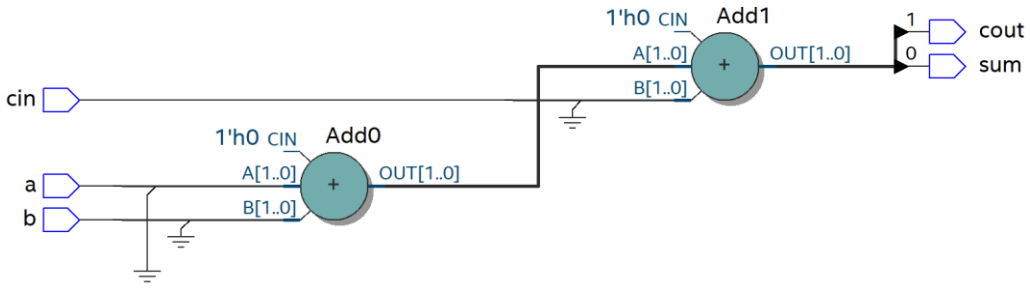
	Resource	Usage
1	Total fan-out	8
2	Total DSP Blocks	0
3	Maximum fan-out node	G4~0
4	Maximum fan-out	1
5	I/O pins	4
6	Estimate of Logic utilization (ALMs needed)	1
7	Dedicated logic registers	0
8	Combinational ALUT usage for logic	1
1	-- 4 input functions	0
2	-- 5 input functions	0
3	-- 6 input functions	0
4	-- 7 input functions	0
5	-- <=3 input functions	1
9	Average fan-out	0.89
10		
11		
12		
13		
14		

d. Modelsim simulation result (same as behavioral level simulation result)

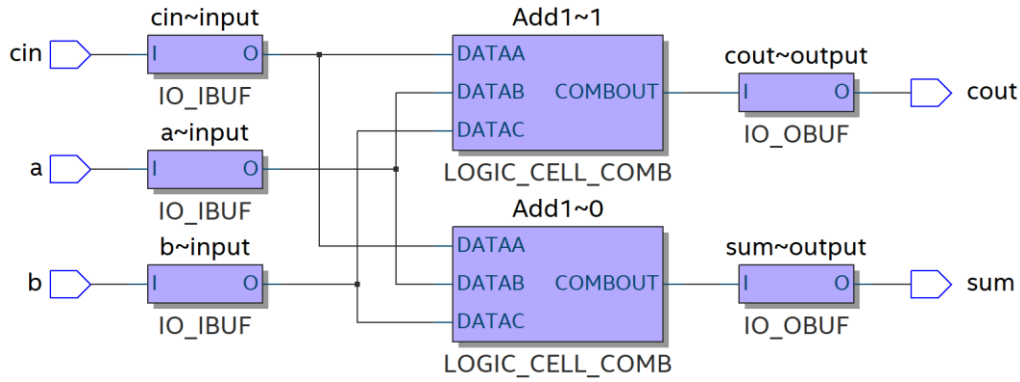
Full Adder

1. Behavioral level

a. RTL schematic



b. Post mapping schematic



c. Resource usage

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1
2		
3	Combinational ALUT usage for logic	2
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
4		
5	Dedicated logic registers	0
6		
7	I/O pins	5
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	cin~input
12	Maximum fan-out	2
13	Total fan-out	13
14	Average fan-out	1.08

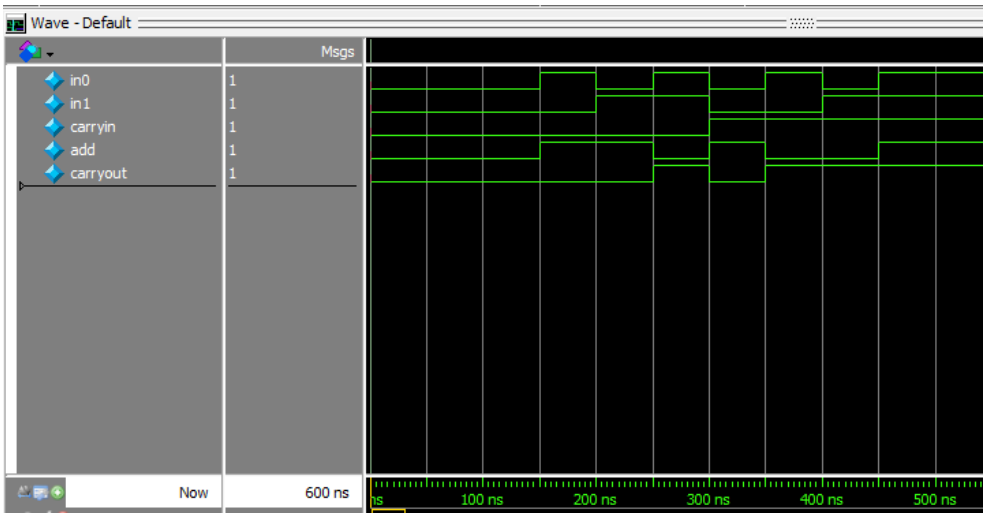
Number of ALUT: 2 (5 I/O pins)

Full adder design need two ALUT for adding with 3 input and 2 output pins.

Number of Functions: 2 (3 input function)

Each output depends on all three inputs, thus 2 functions with 3 inputs

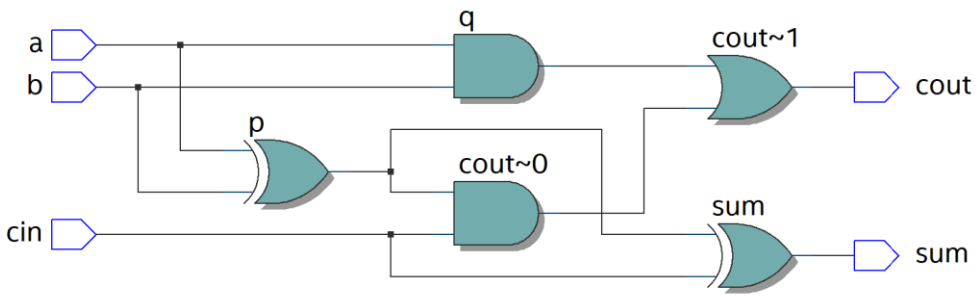
d. Modelsim simulation result



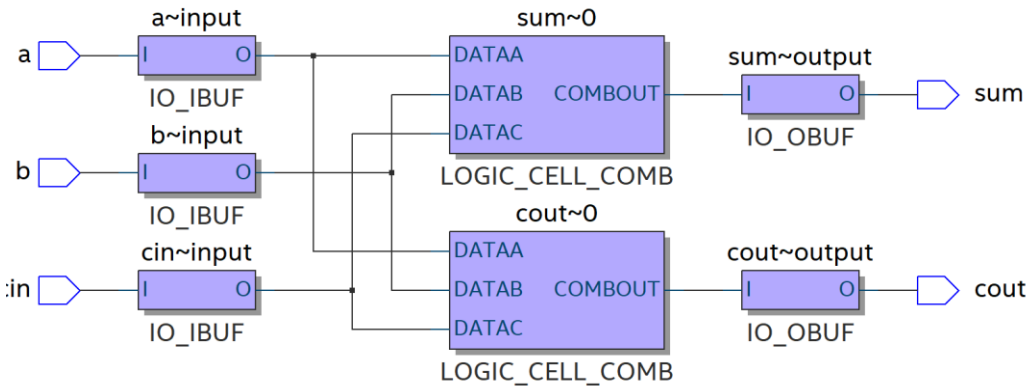
```
Transcript
# Errors: 0, Warnings: 2
# vsim -gui work.fulladder_testbench
# Start time: 21:16:52 on Jul 14,2025
# Loading sv_std.std
# Loading work.fulladder_testbench
# Loading work.fulladder
add wave -position end  sim:/fulladder_testbench/in0
add wave -position end  sim:/fulladder_testbench/in1
add wave -position end  sim:/fulladder_testbench/carryin
add wave -position end  sim:/fulladder_testbench/add
add wave -position end  sim:/fulladder_testbench/carryout
VSIM 48> run -all
#  time=0   a=0   b=0   c=0   sum=0   cout=0
#
#  time=150   a=1   b=0   c=0   sum=1   cout=0
#
#  time=200   a=0   b=1   c=0   sum=1   cout=0
#
#  time=250   a=1   b=1   c=0   sum=0   cout=1
#
#  time=300   a=0   b=0   c=1   sum=1   cout=0
#
#  time=350   a=1   b=0   c=1   sum=0   cout=1
#
#  time=400   a=0   b=1   c=1   sum=0   cout=1
#
#  time=450   a=1   b=1   c=1   sum=1   cout=1
#
```

The full adder takes in two value with a carryin bit and return the sum for the current digit with a carryout bit if needed.

2. **Dataflow level**
    a. **RTL schematic**



    b. **Post mapping schematic**



c. Resource usage

Analysis & Synthesis Resource Usage Summary

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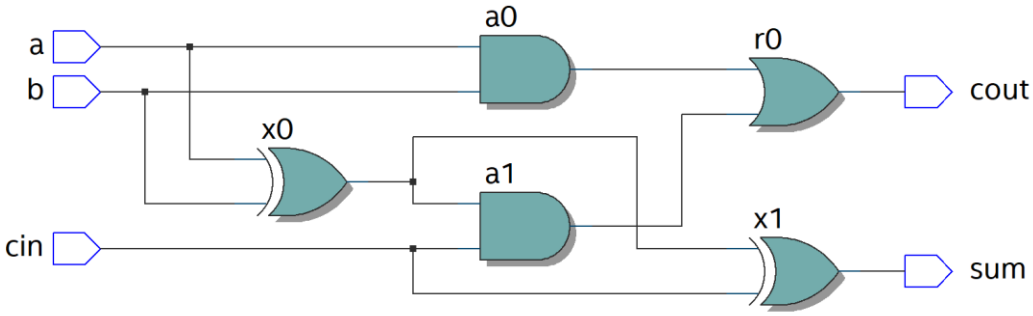
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
4		
5	Dedicated logic registers	0
6		
7	I/O pins	5
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	a~input
12	Maximum fan-out	2
13	Total fan-out	13
14	Average fan-out	1.08

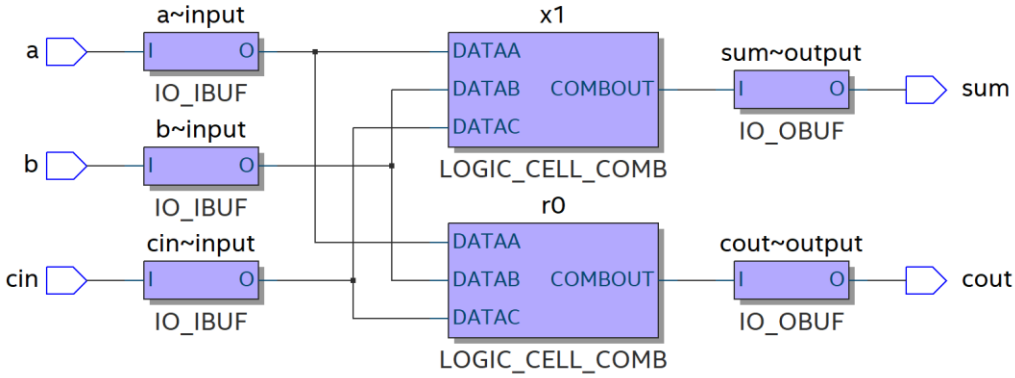
d. Modelsim simulation result (same as behavioral level simulation result)

3. Gatelevel

a. RTL schematic



b. Post mapping schematic



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5	Dedicated logic registers	0
6		
7	I/O pins	5
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	a~input
12	Maximum fan-out	2
13	Total fan-out	13
14	Average fan-out	1.08

d. Modelsim simulation result (same as behavioral level simulation result)