

Personal Info

Address

13750 100 Ave
Surrey, BC, Canada
V3T 5E2

Phone

+12368684445
+97455929557

E-mail

jgafooruni@gmail.com

Linkedin

linkedin.com/in/jassimga4/

Programming Languages

C++
SystemVerilog HDL
Assembly
HTML/CSS
Python

Membership

IEEE – Institute of Electrical and Electronics Engineers
EGBC – Engineers and Geoscientists of British Columbia

Languages

English - Native
Tamil - Intermediate
Arabic - Beginner

Jassim Abdul Gafoor

Completed *Integrated Engineering* with 4 years education and an additional 10 months work experience (Co-op). I am a quick learner and will apply my extensive knowledge to solve challenging problems in a creative manner.

Education

2016 Aug - 2021 May **UNIVERSITY OF BRITISH COLUMBIA, Vancouver, BC, Canada**
Bachelor of Applied Science | Integrated Engineering

Experience

- 2019 Jul - **TELUS Vancouver, Canada** (A leading telecommunication provider)
- 2020 Apr **Co-op Student | HTML/CSS, Confluence, Jira**
- Handled the data migration project of 3000+ documents from MS SharePoint to Confluence platform
 - Gathered various business requirements from end-users and consolidated as technical requirements for the development team
 - Utilized the dormant Enterprise Bridge software to migrate less complex data (9000+) from MS SharePoint
 - Performed QA/QC of developed environment
 - Standardized the processes and procedures to ensure data integrity and created required templates

Projects

- 2021 May **Composition and Rendering | Blender**
- Modelled various 3D objects in blender to create a composition
 - Rendered scenes and video with ultra-realistic ray traced rendering engine
- 2021 Feb **Clock Buffer Design | Cadence Virtuoso and MATLAB**
- Designed signal buffer layout to minimize clock skew between different domains
 - Modelled delay and fanout of 4 different stages to meet rise/fall timing requirements
- 2021 Jan **Bragg interferometer | KLayout, Lumerical Interconnect, MATLAB, and Python**
- Calculated Transfer Matrix Model in MATLAB to simulate design
 - Used KLayout to fabricate in silicon foundry and tested in lab
- 2020 Dec **Chip Layout 45nm architecture | Cadence and SystemVerilog**
- Synthesized a Finite State Machine module to control a user-driven lighting system
 - Created CMOS layout of integrated circuit using Cadence Virtuoso toolkit
- 2019 Jan **Simple iPod | SystemVerilog, Assembly and C**
- Built a basic iPod with music playing and volume controls in an FPGA
 - Devised flash controller module for reading files from flash
- 2018 Jan **MEMS Gyroscope Project | AutoDesk Inventor, Solidworks and Clewin**
- Designed a Micro Gyroscope (0.2mmx0.2mm)
 - Generated mask layouts in Clewin for fabrication with SOI-MUMPS process
- 2017 Apr **Marketing Infographics for UBC Clubs | Adobe Photoshop**
- Designed various posters and infographics for Paper Invention Club
 - Created sponsorship package and logo for UBC Thunderbikes team