File: c:\Users\Jason\Documents\VHDL\grat_to_binary\gray_bin_csop\src\csop.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : csop
4   -- Design      : gray_bin
5   -- Author      : Jason
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    c:\Users\Jason\Documents\VHDL\gray_to_binary\gray_bin\src\csop.vhd
11  -- Generated   : Wed Feb 15 17:37:58 2023
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  --{{ Section below this comment is automatically maintained
22  --   and may be overwritten
23  --{entity {csop} architecture {csop}}
24
25  library IEEE;
26  use IEEE.std_logic_1164.all;
27
28  entity gray_bin is
29       port(
30           g3 : in STD_LOGIC;
31           g2 : in STD_LOGIC;
32           g1 : in STD_LOGIC;
33           g0 : in STD_LOGIC;
34           b3 : out STD_LOGIC;
35           b2 : out STD_LOGIC;
36           b1 : out STD_LOGIC;
37           b0 : out STD_LOGIC
38           );
39  end gray_bin;
40
41  --}} End of automatically maintained section
42
43  architecture csop of gray_bin is
44  begin
45
46      -- enter your statements here --
47      b3 <=
48      (g3 and not g2 and not g1 and not g0) or
49      (g3 and not g2 and not g1 and     g0) or
50      (g3 and not g2 and     g1 and not g0) or
51      (g3 and not g2 and     g1 and     g0) or
52      (g3 and     g2 and not g1 and not g0) or
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```
53      (g3 and     g2 and not g1 and     g0) or
54      (g3 and     g2 and     g1 and not g0) or
55      (g3 and     g2 and     g1 and     g0);
56
57      b2 <=
58      (not g3 and     g2 and not g1 and not g0) or
59      (not g3 and     g2 and not g1 and     g0) or
60      (not g3 and     g2 and     g1 and not g0) or
61      (not g3 and     g2 and     g1 and     g0) or
62      (    g3 and not g2 and not g1 and not g0) or
63      (    g3 and not g2 and not g1 and     g0) or
64      (    g3 and not g2 and     g1 and not g0) or
65      (    g3 and not g2 and     g1 and     g0);
66
67      b1 <=
68      (not g3 and not g2 and     g1 and not g0) or
69      (not g3 and not g2 and     g1 and     g0) or
70      (not g3 and     g2 and not g1 and not g0) or
71      (not g3 and     g2 and not g1 and     g0) or
72      (    g3 and     g2 and     g1 and not g0) or
73      (    g3 and     g2 and     g1 and     g0) or
74      (    g3 and not g2 and not g1 and not g0) or
75      (    g3 and not g2 and not g1 and     g0);
76
77      b0 <=
78      (not g3 and not g2 and not g1 and     g0) or
79      (not g3 and not g2 and     g1 and not g0) or
80      (not g3 and     g2 and     g1 and     g0) or
81      (not g3 and     g2 and not g1 and not g0) or
82      (    g3 and     g2 and not g1 and     g0) or
83      (    g3 and     g2 and     g1 and not g0) or
84      (    g3 and not g2 and     g1 and     g0) or
85      (    g3 and not g2 and not g1 and not g0);
86
87  end csop;
88
89
90
```