Jason Tan

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EDUCATION

Computer Science, Bachelors of Science (BS) ***August 2012 – June 2016***

- University of California, San Diego - GPA: 3.82 La Jolla, CA

PROJECT EXPERIENCE

DocIt **December *2017***

- MEAN Full-Stack Developer -

• Designed and developed a clean, single-page web app for anonymous-based, creative writing and reading. Established a responsive, paper-esque layout design and added a dynamic feed to load viewable, published works.

Fractalize ***August 2017***

- Client-side JavaScript Scripter -

• Built a dynamic escape-time fractals generator website. Researched and applied mathematical recurrence relations for five types of fractals into coloring algorithms affected by user input.

TScorify ***March 2016***

- Front-End and Spark/Scala Application Developer -

• Implemented a Spark/Scala application to produce keyword lists associated to text files of a given data set; formulated a custom TF-IDF scoring algorithm to accurately score words based on relative frequencies.

• Incorporated a web application to display resulting keyword data graphically in a word "cloud".

GlassMADA (Memory Assistive Display for Persons with Alzheimer's) ***December 2015***

- GoogleGlass Android App and Front-End Developer -

• Integrated Scandit framework for QR scanning to perform passive QR scanning, providing users visual reconfirmation of personal information such as relationship details between the user and family members.

• Created MADA Timeline, a website made for the user with Alzheimer's and his/her caretaker to review and filter collected contextual data: past photos' Google geolocations and timestamps.

Battle Blocks ***June 2015***

- Game Designer and C++ Server-Side Engineer -

• Designed and engineered entire server-side gameplay logic and a Bullet physics engine for 3D object simulation.

• Optimized gameplay features such as processing game events, dynamic block object creation/deletion, and damage systems by 24% in execution time and 80% in memory complexity.

KJ ***March 2015***

- System Verilog Hardware Architect -

• Engineered a 3-stage pipelined CPU that runs on a 8-bit ISA and eight general registers. Optimized and tested by executing three different programs in ModelSim's hardware simulation.

• Reduced clock cycles per instruction to 1 by introducing data forwarding to avoid data hazards and asynchronous reading to avoid branch hazards, resulting in no stalling nor flushing.

WORK EXPERIENCE

MarketSource, Inc. ***July 2016 – October 2017***

- Electronics & Entertainment Lead - San Francisco, CA

• Managed team responsibilities, schedules, and tasks. Trained associates for electronics and mobility sales experience and knowledge. Acquired guest needs from face-to-face interactions and promoted sales regarding mobile technologies, smart home devices, and digital services.

TECHNICAL SKILLS

Languages: Java, JavaScript, NodeJS, MongoDB, AngularJS, HTML/CSS, SQL, C++, Scala, C, Python, (System) Verilog

Technologies: Git, npm, Heroku, PostgreSQL, gulp, bower, Unix, JSP, mLab, MS Excel