

# Jason Tan

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## EDUCATION

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**B.S. Computer Science** – University of California, San Diego

**August 2012 – June 2016**

GPA: 3.82 – Graduated with Cum Laude recognition

La Jolla, CA

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## PROJECT EXPERIENCE

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### Fractalize

**August 2017**

- Client-side JS Scripter -

- Developed a dynamic escape-time fractals generator website. Fractal output is affected by user inputs, providing the ability to discover how certain variables may change the mathematical recurrence relation for each pixel point and ultimately, the entire fractal.

### TScorify

**March 2016**

- Spark Application, Scala Developer -

- Implemented a Spark/Scala application to produce keyword lists associated to text files of a given data set; formulated a custom TF-IDF scoring algorithm to accurately score words based on relative frequencies.
- Incorporated a web application to display resulting keyword data graphically in a word "cloud".

### GlassMADA (Memory Assistive Display for Persons with Alzheimer's)

**December 2015**

- GoogleGlass Android and Website HTML/JS Developer -

- Integrated Scandit framework for QR scanning to perform passive QR scanning, providing users visual reconfirmation of personal information such as relationship details between the user and family members.
- Introduced MADA Timeline, a website made for the user with Alzheimer's and his/her caretaker to review and filter collected contextual data: past photos' Google geolocations and timestamps.

### Battle Blocks

**June 2015**

- Game Designer and C++ Server-Side Engineer -

- Established efficient game APIs and game packets for client-server interaction; designed player-oriented gameplay aspects such as Build Mode where players customize their vehicle for combat.
- Designed and built entire server-side gameplay logic and a Bullet physics engine for 3D object simulation.
- Optimized gameplay features such as processing game events, dynamic block object creation/deletion, and damage systems by 24% in execution time and 80% in memory complexity.

### KJ

**March 2015**

- System Verilog Hardware Architect -

- Engineered a 3-stage pipelined CPU that runs on a 8-bit ISA and eight general registers. Optimized and tested by executing three different programs in ModelSim's hardware simulation.
- Reduced clock cycles per instruction to 1 by introducing data forwarding to avoid data hazards and asynchronous reading to avoid branch hazards, resulting in no stalling nor flushing.

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## WORK EXPERIENCE

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### MarketSource, Inc.

**July 2016 - Current**

- Electronics & Entertainment Lead -

San Francisco, CA

- Manage team responsibilities, schedules, and tasks. Train associates for electronics and mobility sales experience and knowledge. Acquiring guest needs from face-to-face interactions and promoting sales regarding mobile technologies, smart home devices, and digital services.

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## TECHNICAL SKILLS

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**Languages:** Java, SQL, Javascript, HTML/CSS, C++, Scala, jQuery, JSON, XML, (System) Verilog

**SW Engineering:** Agile, Object-oriented design, TDD, BDD, MVC, RESTful, open-closed principle

**Technologies:** JSP, Apache Tomcat, PostgreSQL, Bitbucket/Git, Unix, npm, gulp