NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2013 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design
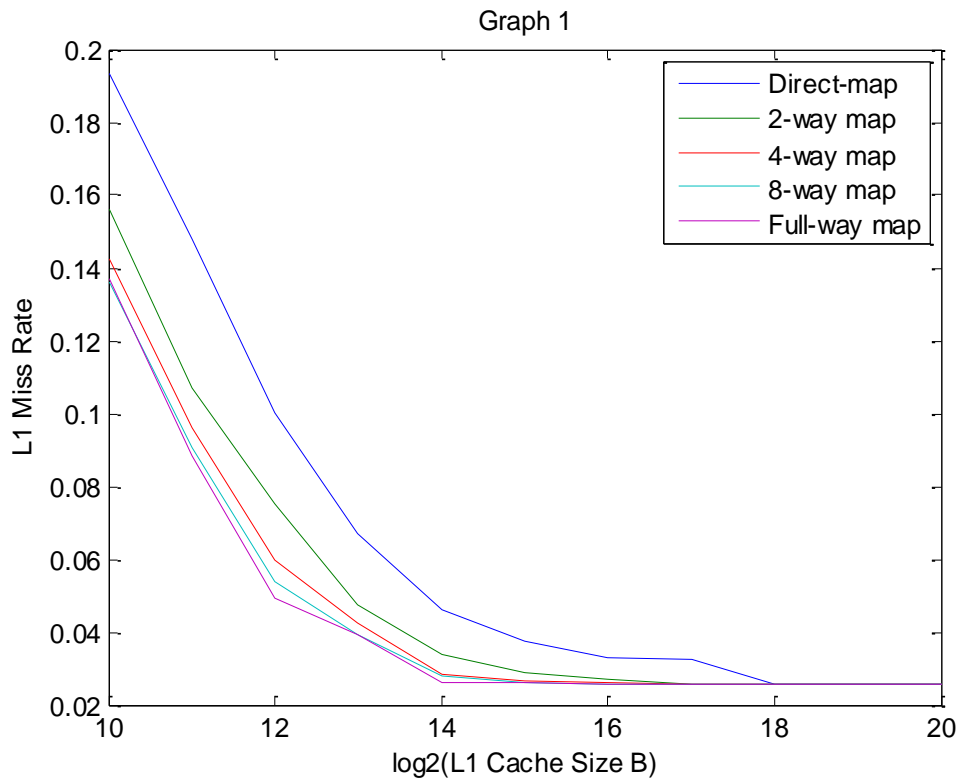
by

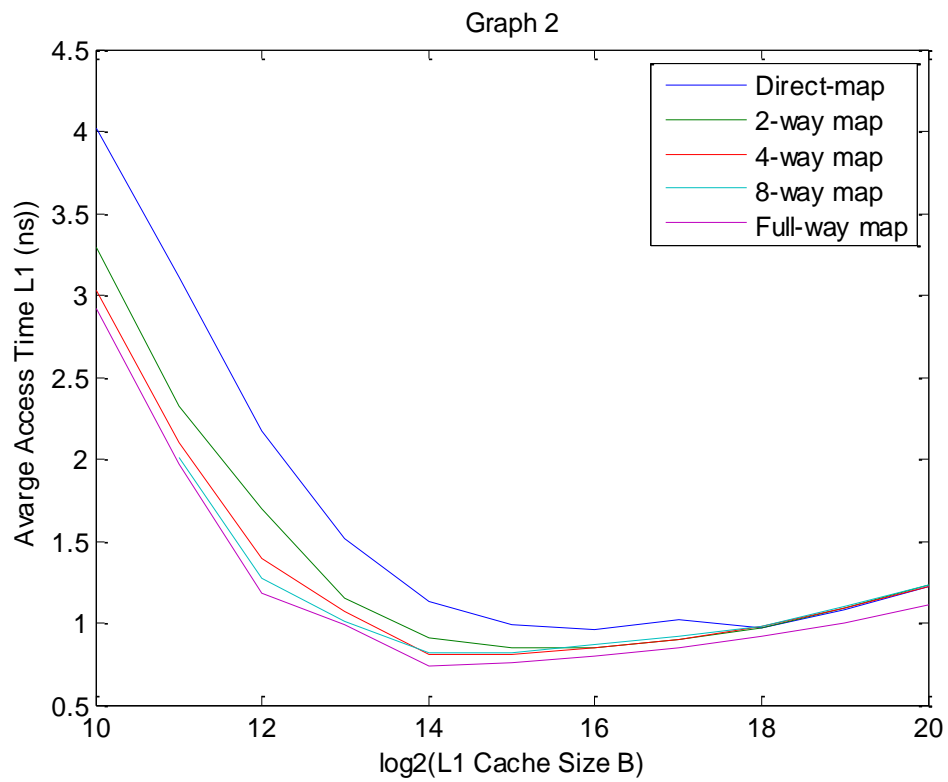**Joshua Stevens**

Graph one:

Graph 1

Discussion:
1. The miss rate goes down as the cache size increase. For the associative, the increasing associative cause the miss rate to go down for a given cache.
2. The compulsory miss rate is going to be near the value of 0.022
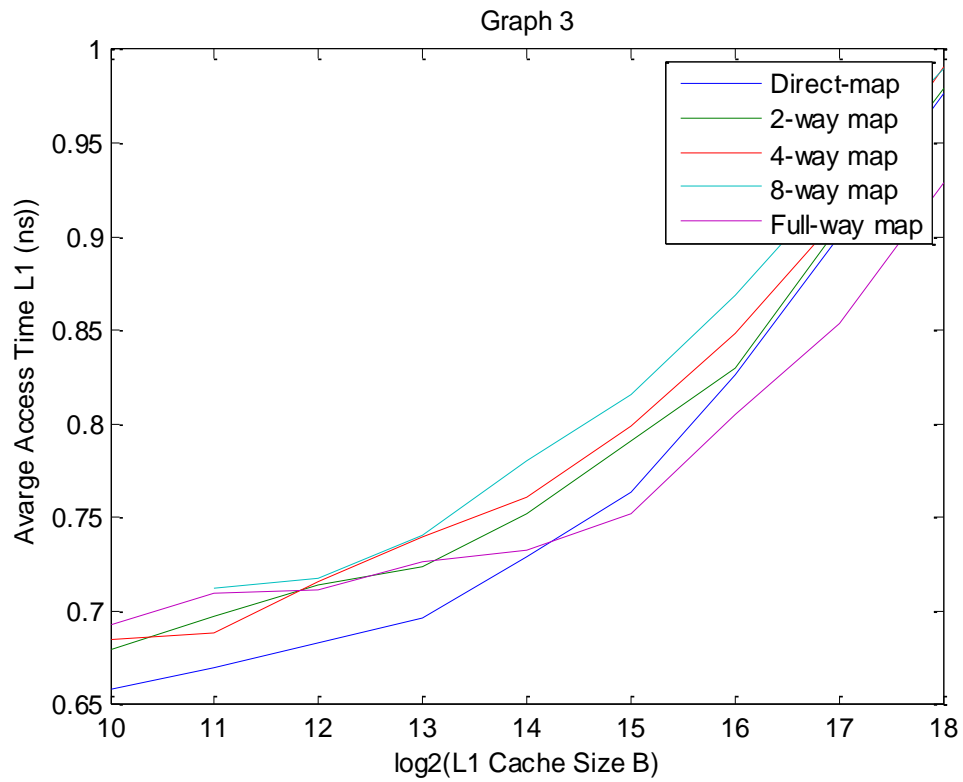3. conflict = miss rate − compulsory

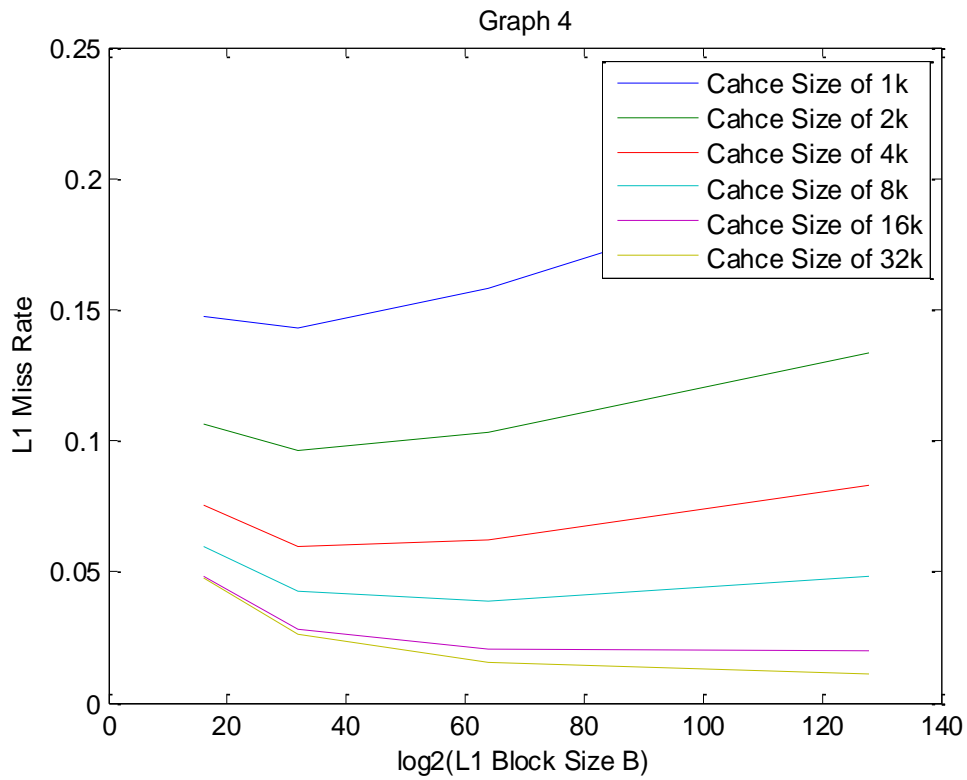| Map type	Conflict
1-way	.168
2-way	.133
4-way	.119
8-way	.116
Full-way	.115

Graph two:

Graph 2

1. The best configuration is a cache size of 16384B and Full-way associativity
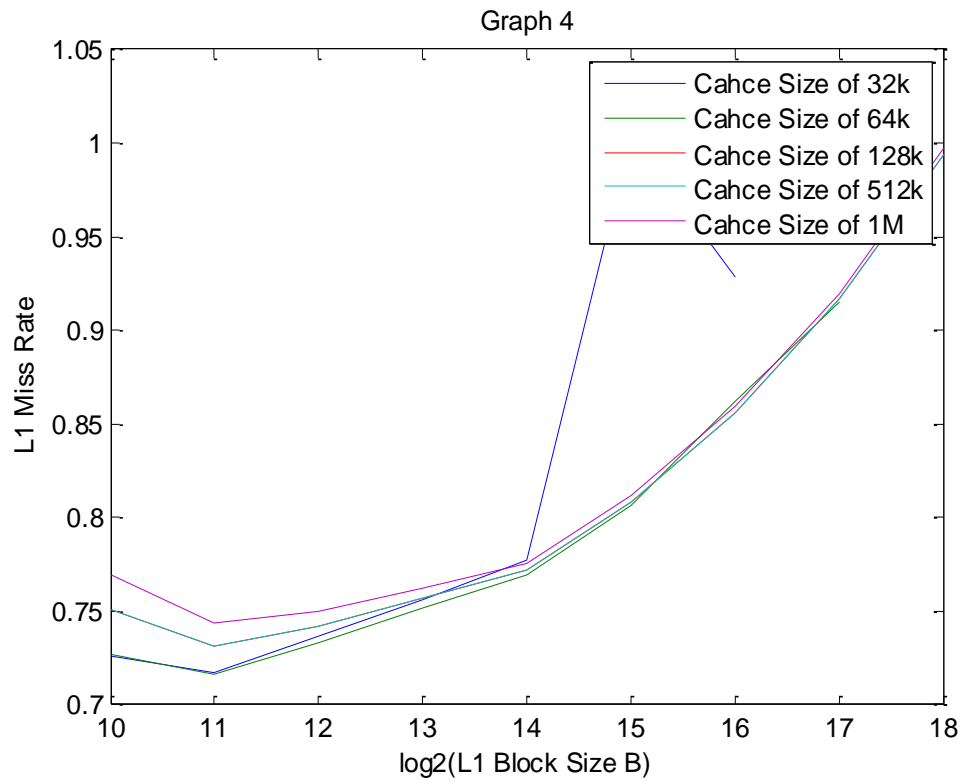
Graph Three:

Graph 3

1. 2-way map has the second best average access time
2. Direct map has the lowers average access time, it is about .1 low than the optimal AAT.

Graph Four

Graph 4

1. Small cache size prefer small block sizes.
   Large cache size prefer large block sizes.
   If there is a dirty bit on a given set and it need to be replaced it cause many of
   other bytes that are not dirty to be replaced.

Graph 5:

Graph 4

9.4

1.