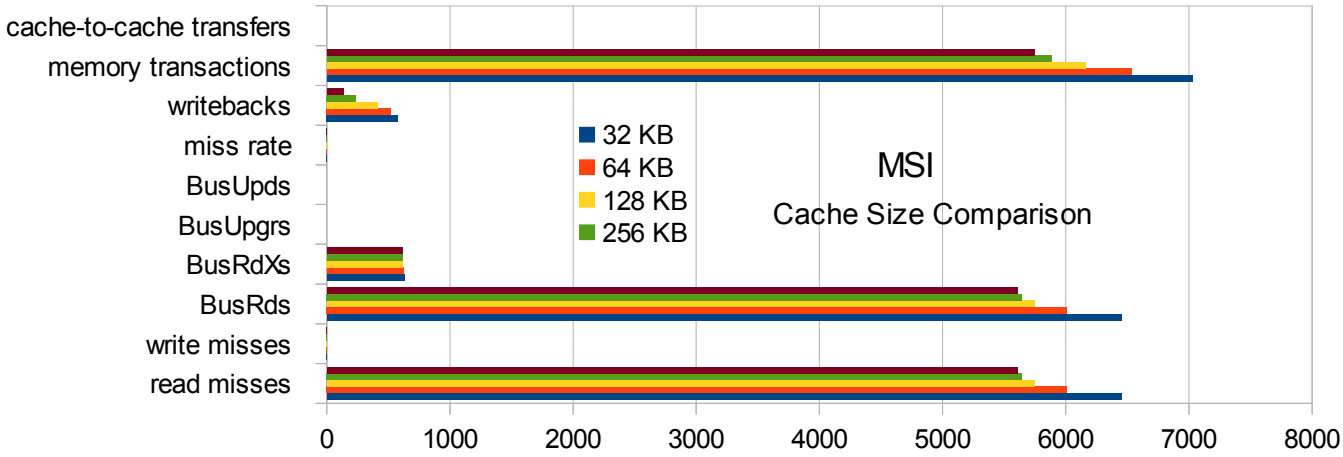
Joshua Stevens and Ryan Clarke
ECE 506

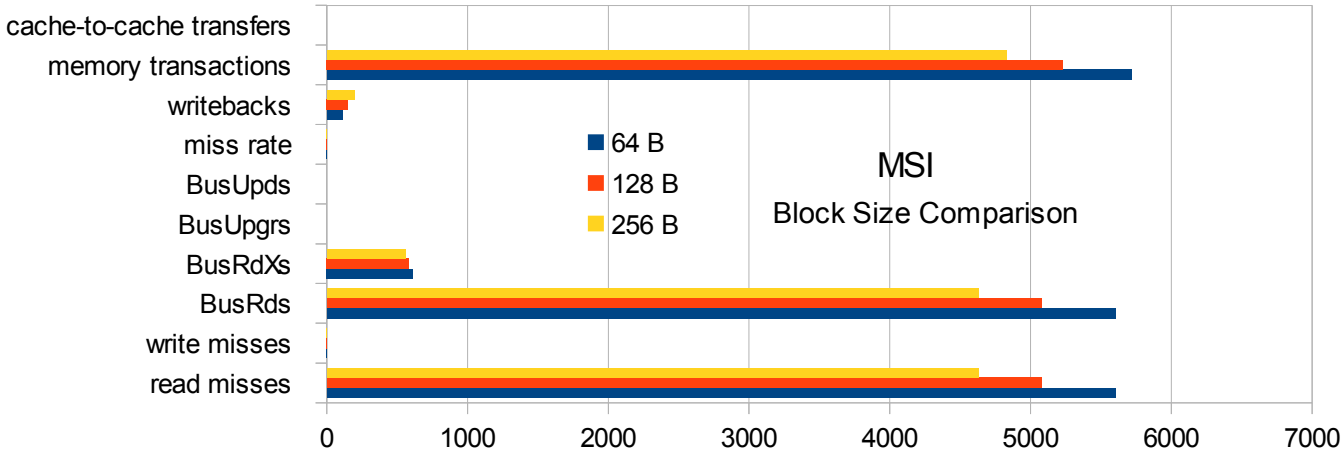
Program 2 Report

Protocol:	MSI				
	Cache Size Comparison				
	32 KB	**64 KB**	**128 KB**	**256 KB**	**512 KB**
read misses	6449.75	6011.50	5749.25	5644.25	5609.50
write misses	2.00	1.75	1.75	1.75	1.75
BusRds	6449.75	6011.50	5749.25	5644.25	5609.50
BusRdXs	630.00	622.75	617.50	614.25	612.50
BusUpgrs	0	0	0	0	0
BusUpds	0	0	0	0	0
miss rate	0.05162	0.04812	0.04602	0.04518	0.04490
writebacks	577.25	519.00	411.50	236.25	134.75
memory transactions	7029.00	6532.25	6162.50	5882.25	5746.00
cache-to-cache transfers	0	0	0	0	0



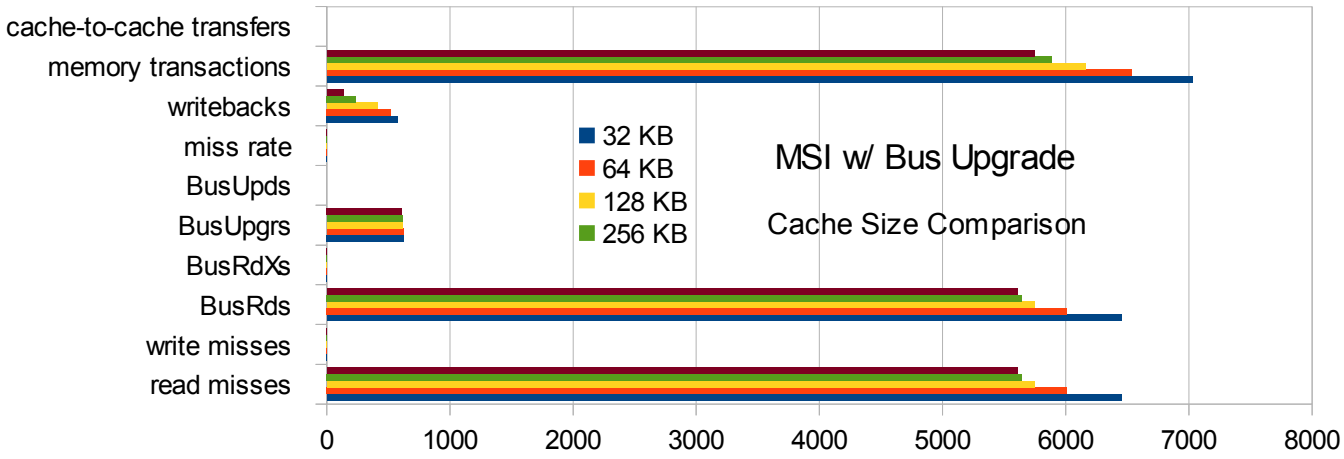
As the cache size increases the memory transactions, writebacks, BusReads and read misses all go down. There is little effect on the number of BusRdXs. There are deminishing returns each time the cache size is increased. The bus traffic is very high for this protocol, and the number of memory transactions is high. This protocol is not very complex.

Protocol:	MSI		
	Block Size Comparison		
	64 B	**128 B**	**256 B**
read misses	5603.50	5078.75	4632.75
write misses	1.75	1.50	1.50
BusRds	5603.50	5078.75	4632.75
BusRdXs	612.50	584.75	560.50
BusUpgrs	0	0	0
BusUpds	0	0	0
miss rate	0.04485	0.04065	0.03708
writebacks	113.25	152.00	197.50
memory transactions	5718.50	5232.25	4831.75
cache-to-cache transfers	0	0	0



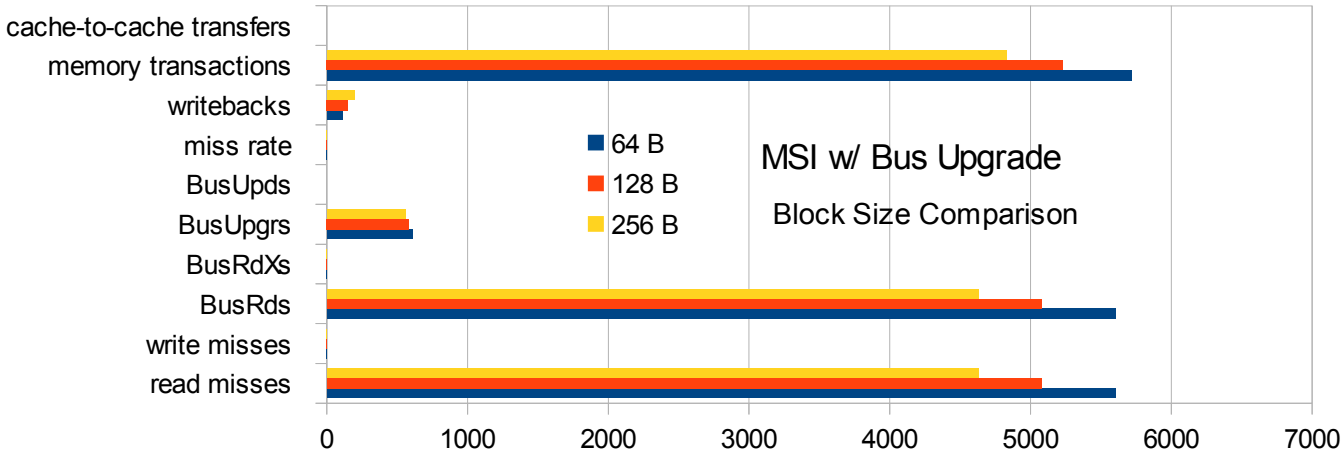
As the block size increases the memory transactions, BusReads and read misses all go down. There is also a small decrease in the number of BusRdXs as the block size is increased. The number of write backs increases as the block size increases. The benefit to increasing the block size is linear, with no diminishing returns evident in testing. The bus traffic is very high for this protocol, as is the number of memory transactions. This protocol is not very complex.

Protocol:	MSI with Bus Upgrade *Cache Size Comparison*				
	32 KB	**64 KB**	**128 KB**	**256 KB**	**512 KB**
read misses	6449.75	6011.50	5749.25	5644.25	5609.50
write misses	2.00	1.75	1.75	1.75	1.75
BusRds	6449.75	6011.50	5749.25	5644.25	5609.50
BusRdXs	2.00	1.75	1.75	1.75	1.75
BusUpgrs	628.00	621.00	615.75	612.50	610.75
BusUpds	0	0	0	0	0
miss rate	0.05162	0.04812	0.04602	0.04518	0.04490
writebacks	577.25	519.00	411.50	236.25	134.75
memory transactions	7029.00	6532.25	6162.50	5882.25	5746.00
cache-to-cache transfers	0	0	0	0	0



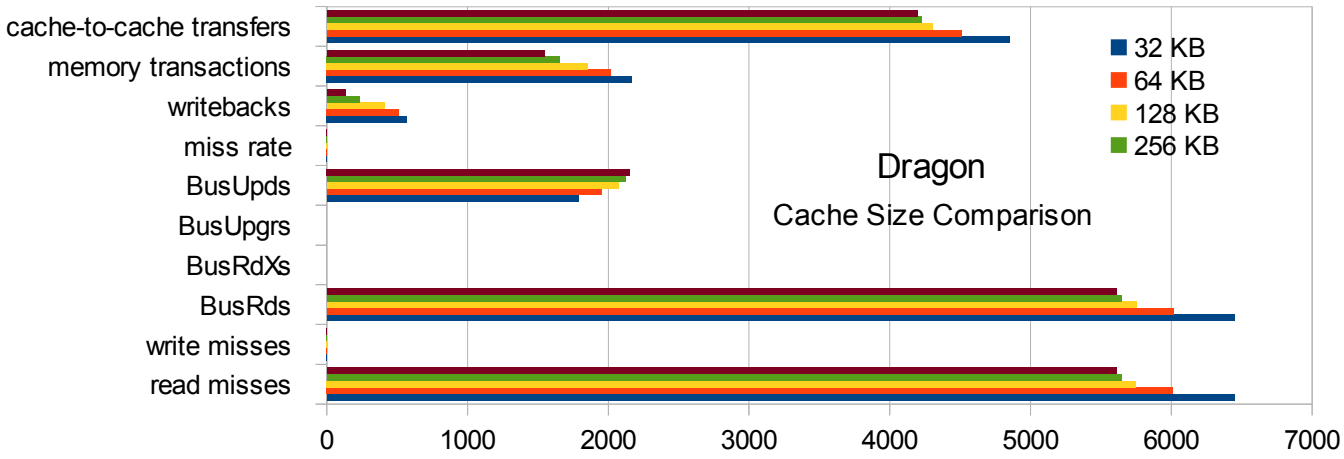
As the cache size increases the memory transactions, write backs BusRds and read misses all go down. There is no effect on the number of BusUpgrs. The number of write backs is very small. As the block size increases there are deminishing returns. The bus traffic is very high for this protocol, and the number of memory transactions is high. This protocol is not very complex.

Protocol:	MSI with Bus Upgrade *Block Size Comparison*		
	64 B	**128 B**	**256 B**
read misses	5603.50	5078.75	4632.75
write misses	1.75	1.50	1.50
BusRds	5603.50	5078.75	4632.75
BusRdXs	1.75	1.50	1.50
BusUpgrs	610.75	583.25	559.00
BusUpds	0	0	0
miss rate	0.04485	0.04065	0.03708
writebacks	113.25	152.00	197.50
memory transactions	5718.50	5232.25	4831.75
cache-to-cache transfers	0	0	0



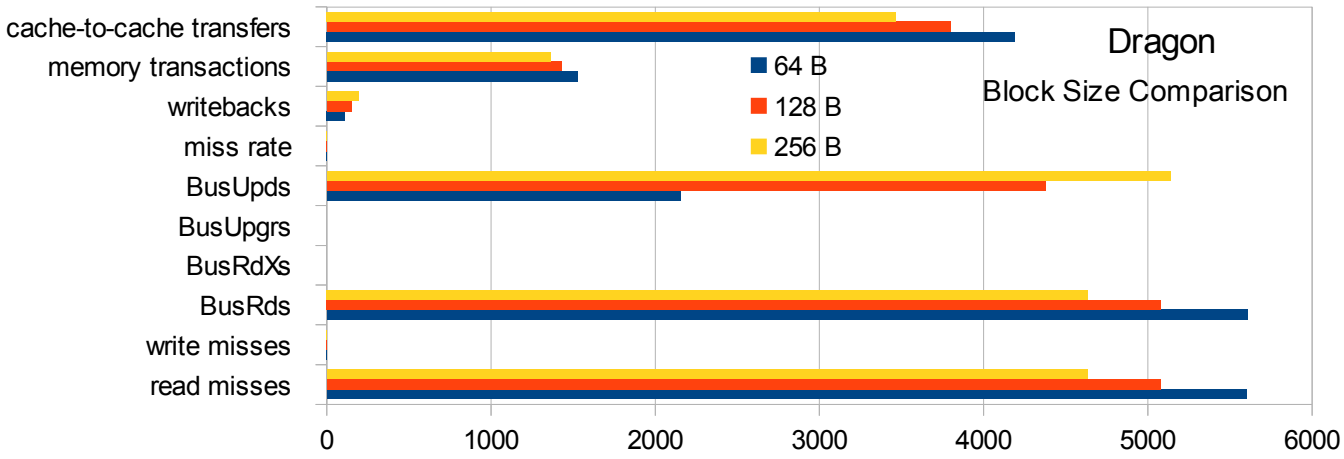
As the block size increases the memory transactions, BusUpgrs, BusReads and read misses go down. The number of write backs is very small, but as the block size gets bigger the number of write backs increase. As the block sizes get bigger there is a linear benefit with no evident deminishing returns. The bus traffic is very high for this protocol, and the number of memory transactions is high. This protocol is not very complex.

Protocol:	**Dragon**				
	Cache Size Comparison				
	32 KB	**64 KB**	**128 KB**	**256 KB**	**512 KB**
read misses	6449.75	6011.50	5749.25	5644.25	5609.50
write misses	2.00	1.75	1.75	1.75	1.75
BusRds	6451.50	6013.25	5751.00	5646.00	5611.25
BusRdXs	0	0	0	0	0
BusUpgrs	0	0	0	0	0
BusUpds	1791.25	1949.50	2072.75	2120.00	2154.25
miss rate	0.05162	0.04812	0.04602	0.04518	0.04490
writebacks	569.50	514.00	409.00	233.75	132.75
memory transactions	2168.50	2020.25	1857.50	1657.00	1547.50
cache-to-cache transfers	4852.75	4507.00	4302.50	4222.75	4196.50



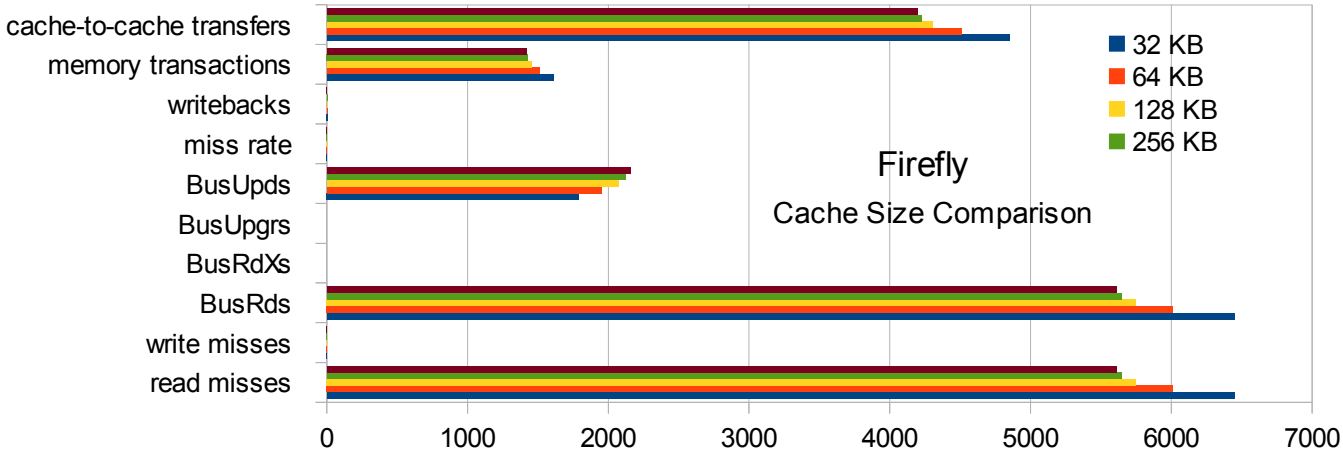
As the cache size increasea the cache-to-cache transfers, memory transactions, write backs, BusRds and read misses go down. As the the cache size increases the number of BusUpgrs goes up. As the cache sizes get bigger there is a non-linear benefit, with deminishing returns. The bus traffic is very low for this protocol, and the number of memory transactions is low. This protocol is more complex.

Protocol:	Dragon		
	Block Size Comparison		
	64 B	**128 B**	**256 B**
read misses	5603.50	5078.75	4632.75
write misses	1.75	1.50	1.50
BusRds	5605.25	5080.25	4634.25
BusRdXs	0	0	0
BusUpgrs	0	0	0
BusUpds	2154.25	4374.75	5138.25
miss rate	0.04485	0.04065	0.03708
writebacks	111.25	149.75	194.75
memory transactions	1524.50	1430.50	1361.75
cache-to-cache transfers	4192.00	3799.50	3467.25



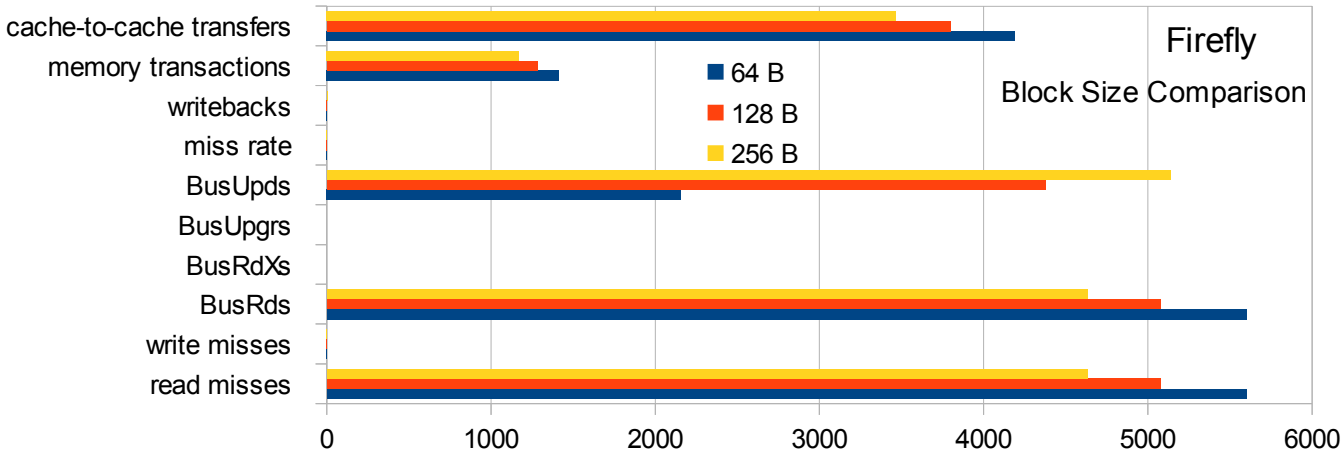
As the block size increases the cache-to-cache transfers, memory transactions,read misses ane BusRds go down. The write backs and the BusUpgrs go up as the block size is increased. As the block sizes get bigger there is a linear benefit. The bus traffic is very low for this protocol. The number of memory transactions is low. This protocol is more complex.

Protocol:	Firefly				
	Cache Size Comparison				
	32 KB	**64 KB**	**128 KB**	**256 KB**	**512 KB**
read misses	6449.75	6011.50	5749.25	5644.25	5609.50
write misses	2.00	1.75	1.75	1.75	1.75
BusRds	6449.75	6011.50	5749.25	5644.25	5609.50
BusRdXs	0	0	0	0	0
BusUpgrs	0	0	0	0	0
BusUpds	1793.00	1951.25	2074.50	2121.75	2156.00
miss rate	0.05162	0.04812	0.04602	0.04518	0.04490
writebacks	8.75	6.25	6.00	5.00	2.25
memory transactions	1607.75	1512.50	1454.50	1428.25	1417.00
cache-to-cache transfers	4852.75	4507.00	4302.50	4222.75	4196.50



As the cache size increases the cache-to-cache transfers, memory transactions, read misses and BusRds go down. As the the cache size increases the number of BusUpgrs goes up. As the cache sizes get bigger there is a non-linear benefit with deminishing returns. The bus traffic is very low for this protocol. The number of memory transactions is low. This protocol is complex.

Protocol:	Firefly		
	Block Size Comparison		
	64 B	**128 B**	**256 B**
read misses	5603.50	5078.75	4632.75
write misses	1.75	1.50	1.50
BusRds	5603.50	5078.75	4632.75
BusRdXs	0	0	0
BusUpgrs	0	0	0
BusUpds	2156.00	4376.25	5139.75
miss rate	0.04485	0.04065	0.03708
writebacks	1.50	2.00	2.50
memory transactions	1414.75	1282.75	1169.50
cache-to-cache transfers	4192.00	3799.50	3467.25



As the block size increases the cache-to-cache transfers, memory transactions, read misses and BusRds go down. As the the cache size increases the number of BusUpgrs goes up. As the block sizes get bigger there is a linear benefit. The bus traffic is very low for this protocol. The number of memory transactions is low. This protocol is complex.