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ECE 506

Program Report 3

**Results**

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| --- | --- | --- | --- | --- | --- |
| Simulation results (Cache 0) | | | | | |
| **Size** | **32kB** | **64kB** | **128kB** | **256kB** | **512kB** |
| **number of reads** | 112661 | 112661 | 112661 | 112661 | 112661 |
| **number of read misses** | 6359 | 6032 | 5817 | 5746 | 5721 |
| **number of writes** | 11942 | 11942 | 11942 | 11942 | 11942 |
| **write misses** | 36 | 24 | 13 | 13 | 10 |
| **total miss rate** | 0.051323 | 0.048602 | 0.046789 | 0.046219 | 0.045994 |
| **number of writebacks** | 2168 | 2007 | 1801 | 1616 | 1543 |
| **number of Invalidations** | 1990 | 1940 | 1889 | 1873 | 1852 |
| **number of cache-to-cache transfers** | 4748 | 4538 | 4373 | 4316 | 4295 |

For Cache 0,

As the Cache Size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations abd cache-to-cache transactions.

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| Simulation results (Cache 1) | | | | | |
| **Size** | **32kB** | **64kB** | **128kB** | **256kB** | **512kB** |
| **number of reads** | 110830 | 110830 | 110830 | 110830 | 110830 |
| **number of read misses** | 6391 | 6057 | 5845 | 5780 | 5762 |
| **number of writes** | 11710 | 11710 | 11710 | 11710 | 11710 |
| **write misses** | 38 | 26 | 14 | 12 | 9 |
| **total miss rate** | 0.052465 | 0.049641 | 0.047813 | 0.047266 | 0.047095 |
| **number of writebacks** | 2131 | 1985 | 1800 | 1584 | 1509 |
| **number of Invalidations** | 2012 | 1958 | 1902 | 1884 | 1862 |
| **number of cache-to-cache transfers** | 1618 | 1538 | 1481 | 1468 | 1463 |

For Cache 1,

As the Cache Size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations and cache-to-cache transactions.

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| Simulation results (Cache 2) | | | | | |
| **Size** | **32kB** | **64kB** | **128kB** | **256kB** | **512kB** |
| **number of reads** | 114938 | 114938 | 114938 | 114938 | 114938 |
| **number of read misses** | 6385 | 6033 | 5817 | 5748 | 5728 |
| **number of writes** | 12383 | 12383 | 12383 | 12383 | 12383 |
| **write misses** | 37 | 25 | 14 | 12 | 9 |
| **total miss rate** | 0.050439 | 0.047581 | 0.045798 | 0.04524 | 0.045059 |
| **number of writebacks** | 2174 | 2016 | 1812 | 1629 | 1544 |
| **number of Invalidations** | 1982 | 1927 | 1885 | 1869 | 1853 |
| **number of cache-to-cache transfers** | 43 | 29 | 21 | 22 | 19 |

For Cache 2,

As the Cache Size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations and cache-to-cache transactions.

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| Simulation results (Cache 3) | | | | | |
| **Size** | **32kB** | **64kB** | **128kB** | **256kB** | **512kB** |
| **number of reads** | 113428 | 113428 | 113428 | 113428 | 113428 |
| **number of read misses** | 6405 | 6060 | 5850 | 5783 | 5761 |
| **number of writes** | 12108 | 12108 | 12108 | 12108 | 12108 |
| **write misses** | 34 | 23 | 12 | 10 | 7 |
| **total miss rate** | 0.051292 | 0.048456 | 0.046696 | 0.046146 | 0.045947 |
| **number of writebacks** | 2211 | 2056 | 1824 | 1617 | 1542 |
| **number of Invalidations** | 1994 | 1938 | 1884 | 1865 | 1846 |
| **number of cache-to-cache transfers** | 50 | 39 | 26 | 30 | 28 |

For Cache 3,

As the cache size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations and cache-to-cache transactions.

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| --- | --- | --- | --- |
| Simulation results (Cache 0) | | | |
| **Block Size** | **64B** | **128B** | **256B** |
| **number of reads** | 112661 | 112661 | 112661 |
| **number of read misses** | 5716 | 5293 | 4903 |
| **number of writes** | 11942 | 11942 | 11942 |
| **write misses** | 9 | 10 | 8 |
| **total miss rate** | 0.045946 | 0.042559 | 0.039413 |
| **number of writebacks** | 1520 | 1476 | 1401 |
| **number of Invalidations** | 1845 | 1801 | 1764 |
| **number of cache-to-cache transfers** | 4291 | 3999 | 3717 |

For Cache 0,

As the block size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations and cache-to-cache transactions.

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| --- | --- | --- | --- |
| Simulation results (Cache 1) | | | |
| **Block Size** | **64B** | **128B** | **256B** |
| **number of reads** | 110830 | 110830 | 110830 |
| **number of read misses** | 5752 | 5346 | 4941 |
| **number of writes** | 11710 | 11710 | 11710 |
| **write misses** | 8 | 8 | 6 |
| **total miss rate** | 0.047005 | 0.043692 | 0.04037 |
| **number of writebacks** | 1490 | 1456 | 1428 |
| **number of Invalidations** | 1853 | 1801 | 1762 |
| **number of cache-to-cache transfers** | 1462 | 1365 | 1252 |

For Cache 1,

As the block size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks, invalidations and cache-to-cache transactions.

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| --- | --- | --- | --- |
| Simulation results (Cache 2) | | | |
| **Block Size** | **64B** | **128B** | **256B** |
| **number of reads** | 114938 | 114938 | 114938 |
| **number of read misses** | 5723 | 5303 | 4905 |
| **number of writes** | 12383 | 12383 | 12383 |
| **write misses** | 8 | 9 | 7 |
| **total miss rate** | 0.045012 | 0.041721 | 0.03858 |
| **number of writebacks** | 1523 | 1480 | 1420 |
| **number of Invalidations** | 1844 | 1790 | 1763 |
| **number of cache-to-cache transfers** | 18 | 25 | 31 |

For Cache 2,

As the block size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks and invalidations. There is an increase in the number of cache-to-cache transactions.

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| --- | --- | --- | --- |
| Simulation results (Cache 3) | | | |
| **Block Size** | **64B** | **128B** | **256B** |
| **number of reads** | 113428 | 113428 | 113428 |
| **number of read misses** | 5754 | 5337 | 4945 |
| **number of writes** | 12108 | 12108 | 12108 |
| **write misses** | 6 | 7 | 5 |
| **total miss rate** | 0.045883 | 0.042569 | 0.039431 |
| **number of writebacks** | 1525 | 1503 | 1445 |
| **number of Invalidations** | 1837 | 1784 | 1744 |
| **number of cache-to-cache transfers** | 27 | 32 | 40 |

For Cache 3,

As the block size increase, there is a reduction in number of read misses, number of write misses. Because there is a reduction in the number of read and write misses, there will be a reduction in the total miss rate. There is a reduction in the number of writebacks and invalidations. There is an increase in the number of cache-to-cache transactions.

Conclusion

As the block size and cache sizes increase, there is a reduction in the number of read and write misses. If the block size is set at 64B and the cache size is increased, the total miss rate will approach asymptote where there is no benefit by increasing the cache size. The same goes for the block size. Also, the number of total number of messages being sent goes done as the cache size and bloc size increase.