DLD LAB WIN 2021

Experiment 6

Aim: To simulate logic gates 1. 1bit comparator

2. 2bit comparator
3. 4bit comparator
4. 6bit comparator

Tools used: vivado software

Truth tables:

1bit comparator:

a	b	a<b	a>b	a=b
0	0	0	0	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

2bit comparator:

A		B				
a1	a0	b1	b0	A<B	A>B	A=B
0	0	0	0	0	0	1
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	0	1
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	0	1	1	1	0	0
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	0	0	1

4 bit comparator:

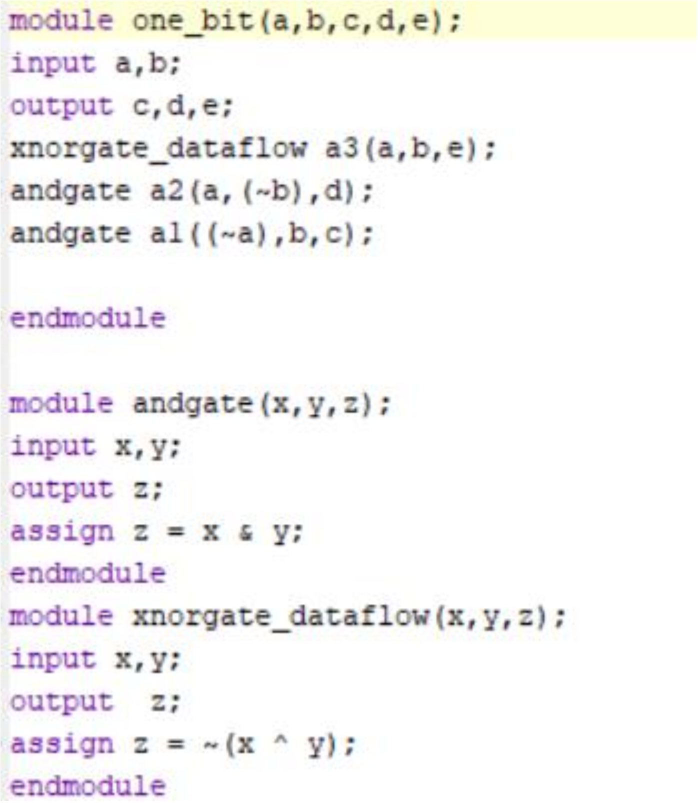
a3b3	a2b2	a1b1	a0b0	A<B	A>B	A=B
a3>b3	x	x	x	0	1	0
a3<b3	x	x	x	1	0	0
a3=b3	a2>b2	x	x	0	1	0
a3=b3	a2<b2	x	x	1	0	0
a3=b3	a2=b2	a1>b1	x	0	1	0
a3=b3	a2=b2	a1<b1	x	1	0	0
a3=b3	a2=b2	a1=b1	a0>b0	0	1	0
a3=b3	a2=b2	a1=b1	a0<b0	1	0	0
a3=b3	a2=b2	a1=b1	a0=b0	0	0	1

6bit comparator:

a5b5	a4b4	a3b3	a2b2	a1b1	a0b0	A<B	A>B	A=B
a5>b5	x	x	x	x	x	0	1	0
a5<b5	x	x	x	x	x	0	0	1
a5=b5	a4>b4	x	x	x	x	0	1	0
a5=b5	a4<b4	x	x	x	x	0	0	1
a5=b5	a4=b4	a3>b3	x	x	x	0	1	0
a5=b5	a4=b4	a3b3	a2b2	x	x	0	0	1
a5=b5	a4=b4	a3b3	a2b2	x	x	0	1	0
a5=b5	a4=b4	A3b3	a2b2	a1b1	x	0	0	1
a5=b5	a4=b4	a3b3	a2b2	a1b1	a0>b0	0	1	0
a5=b5	a4=b4	a3b3	a2b2	a1b1	a0<b0	0	0	1
a5=b5	a4=b4	a3b3	a2b2	a1b1	a0=b0	1	0	0

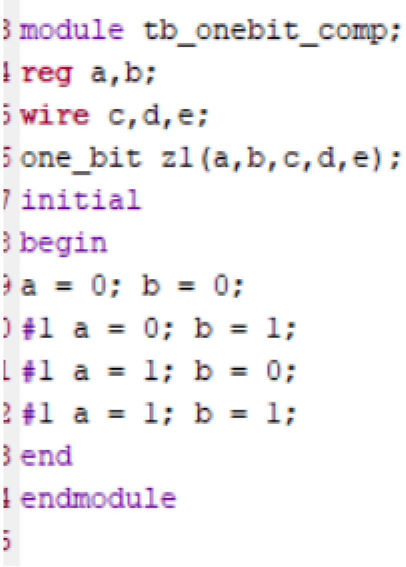
Codes:

1bit comparator:



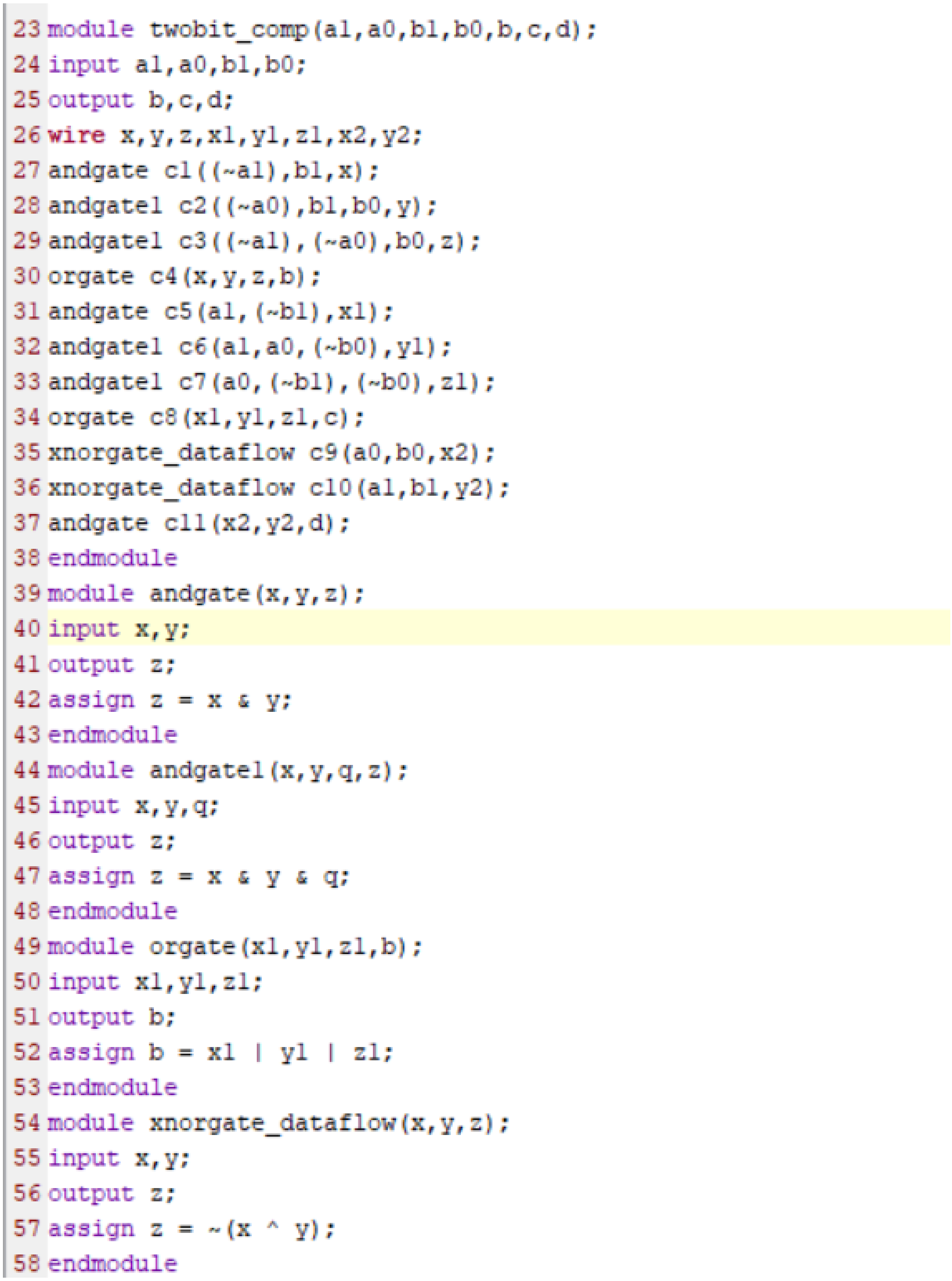
```
module one_bit(a,b,c,d,e);
input a,b;
output c,d,e;
xnorgate_dataflow a3(a,b,e);
andgate a2(a,(~b),d);
andgate a1((~a),b,c);

endmodule

module andgate(x,y,z);
input x,y;
output z;
assign z = x & y;
endmodule
module xnorgate_dataflow(x,y,z);
input x,y;
output  z;
assign z = ~(x ^ y);
endmodule
```

Test bench code



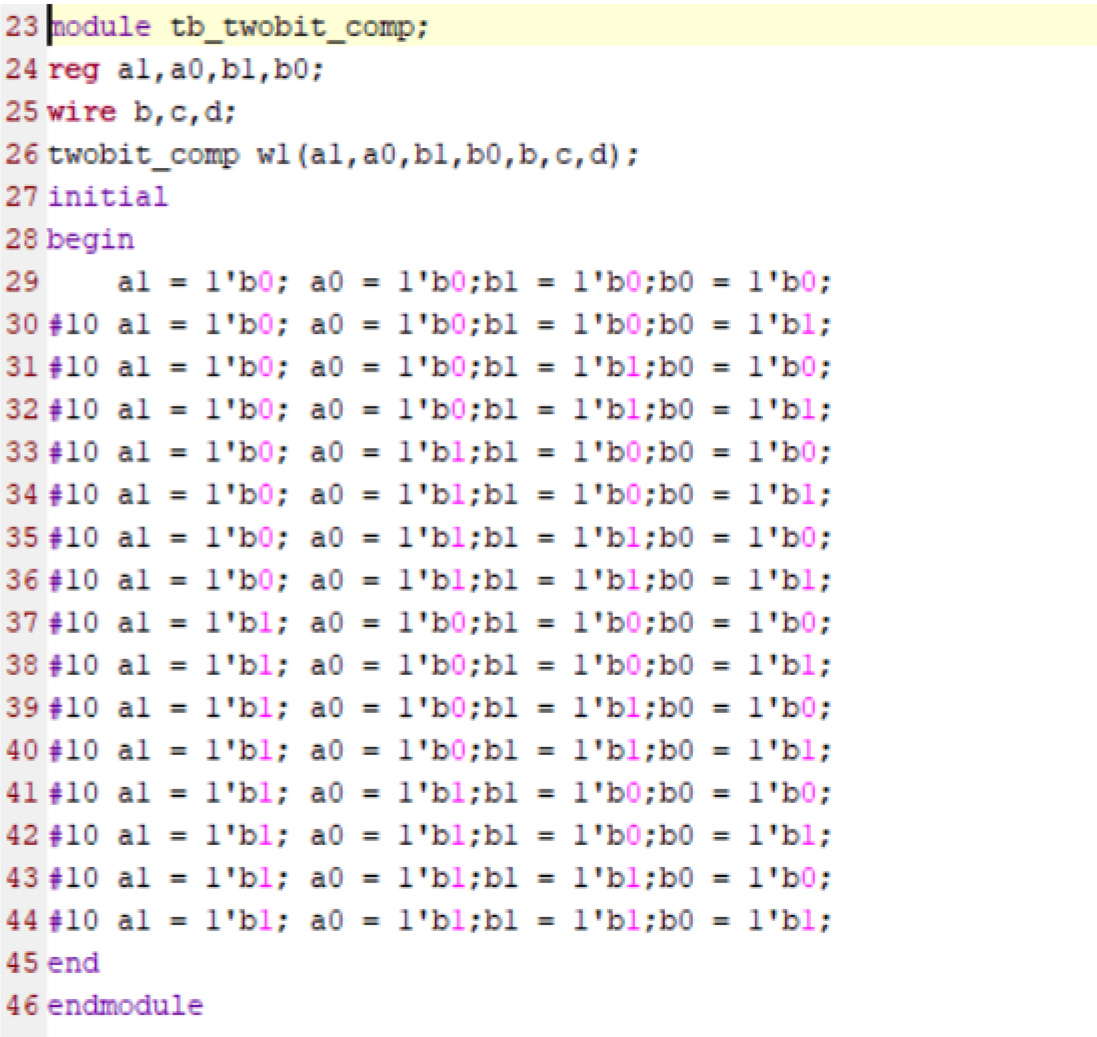
```
module tb_onebit_comp;
reg a,b;
wire c,d,e;
one_bit z1(a,b,c,d,e);
initial
begin
a = 0; b = 0;
#1 a = 0; b = 1;
#1 a = 1; b = 0;
#1 a = 1; b = 1;
end
endmodule
```

2 bit comparator:



```
module twobit_comp(a1,a0,b1,b0,b,c,d);
input a1,a0,b1,b0;
output b,c,d;
wire x,y,z,x1,y1,z1,x2,y2;
andgate c1((~a1),b1,x);
andgate1 c2((~a0),b1,b0,y);
andgate1 c3((~a1),(~a0),b0,z);
orgate c4(x,y,z,b);
andgate c5(a1,(~b1),x1);
andgate1 c6(a1,a0,(~b0),y1);
andgate1 c7(a0,(~b1),(~b0),z1);
orgate c8(x1,y1,z1,c);
xnorgate_dataflow c9(a0,b0,x2);
xnorgate_dataflow c10(a1,b1,y2);
andgate c11(x2,y2,d);
endmodule
module andgate(x,y,z);
input x,y;
output z;
assign z = x & y;
endmodule
module andgate1(x,y,q,z);
input x,y,q;
output z;
assign z = x & y & q;
endmodule
module orgate(x1,y1,z1,b);
input x1,y1,z1;
output b;
assign b = x1 | y1 | z1;
endmodule
module xnorgate_dataflow(x,y,z);
input x,y;
output z;
assign z = ~(x ^ y);
endmodule
```

Test bench code:



```
module tb_twobit_comp;
reg a1,a0,b1,b0;
wire b,c,d;
twobit_comp w1(a1,a0,b1,b0,b,c,d);
initial
begin
    a1 = 1'b0; a0 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a1 = 1'b0; a0 = 1'b0;b1 = 1'b0;b0 = 1'b1;
#10 a1 = 1'b0; a0 = 1'b0;b1 = 1'b1;b0 = 1'b0;
#10 a1 = 1'b0; a0 = 1'b0;b1 = 1'b1;b0 = 1'b1;
#10 a1 = 1'b0; a0 = 1'b1;b1 = 1'b0;b0 = 1'b0;
#10 a1 = 1'b0; a0 = 1'b1;b1 = 1'b0;b0 = 1'b1;
#10 a1 = 1'b0; a0 = 1'b1;b1 = 1'b1;b0 = 1'b0;
#10 a1 = 1'b0; a0 = 1'b1;b1 = 1'b1;b0 = 1'b1;
#10 a1 = 1'b1; a0 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a1 = 1'b1; a0 = 1'b0;b1 = 1'b0;b0 = 1'b1;
#10 a1 = 1'b1; a0 = 1'b0;b1 = 1'b1;b0 = 1'b0;
#10 a1 = 1'b1; a0 = 1'b0;b1 = 1'b1;b0 = 1'b1;
#10 a1 = 1'b1; a0 = 1'b1;b1 = 1'b0;b0 = 1'b0;
#10 a1 = 1'b1; a0 = 1'b1;b1 = 1'b0;b0 = 1'b1;
#10 a1 = 1'b1; a0 = 1'b1;b1 = 1'b1;b0 = 1'b0;
#10 a1 = 1'b1; a0 = 1'b1;b1 = 1'b1;b0 = 1'b1;
end
endmodule
```

4bit comparator:

Code:

```
module fourbit_comp(a0,a1,a2,a3,b0,b1,b2,b3,A_LT_B,A_GT_B,A_EQU_B);
input  a0,a1,a2,a3,b0,b1,b2,b3;
output A_EQU_B,A_GT_B,A_LT_B;
wire x1,x2,x3,x4,y1,y2,y3,y4;
xnorgate r1(a3,b3,x1);
xnorgate r2(a2,b2,x2);
xnorgate r3(a1,b1,x3);
xnorgate r4(a0,b0,x4);
andgate i1(x1,x2,x5);
andgate i2(x3,x4,x6);
andgate i3(x5,x6,A_EQU_B);
andgate p1(a3,(~b3),y1);
andgate p2(a2,(~b2),y2);
andgate p3(a1,(~b1),y3);
andgate p4(a0,(~b0),y4);
andgate p5(x1,y2,y5);
andgate p6(x2,y3,y6);
andgate p7(x3,y4,y7);
orgate p8(y1,y5,y8);
orgate p9(y6,y7,y9);
orgate p10(y8,y9,A_GT_B);
andgate k1((~a3),b3,z1);
andgate k2((~a2),b2,z2);
andgate k3((~a1),b1,z3);
andgate k4((~a0),b0,z4);
andgate k5(x1,z2,z5);
andgate k6(x2,z3,z6);
andgate k7(x3,z4,z7);
orgate k9(z1,z5,z8);
orgate k10(z6,z7,z9);
orgate k12(z8,z9,A_LT_B);
endmodule
module orgate(x1,y1,b);
input x1,y1;
output b;
assign b = x1 | y1 ;
endmodule
module andgate(x,y,z);
input x,y;
output z;
assign z = x & y;
```

endmodule

module xnorgate(x,y,z);

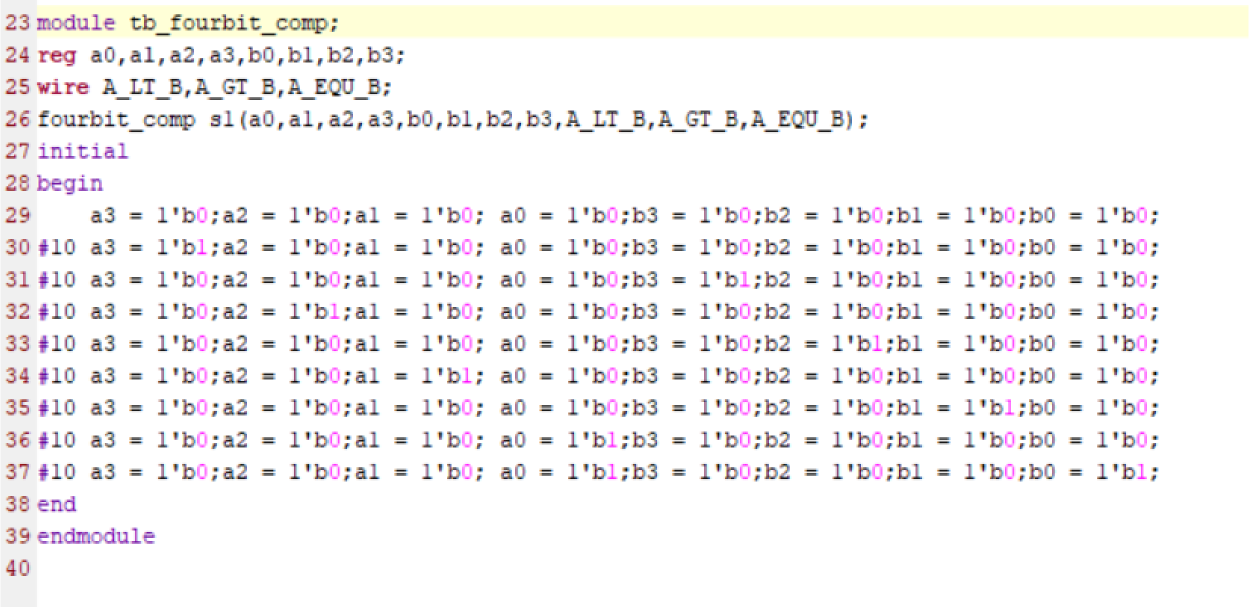
input x,y;

output z;

assign z = ~(x ^ y);

endmodule

Test bench code:



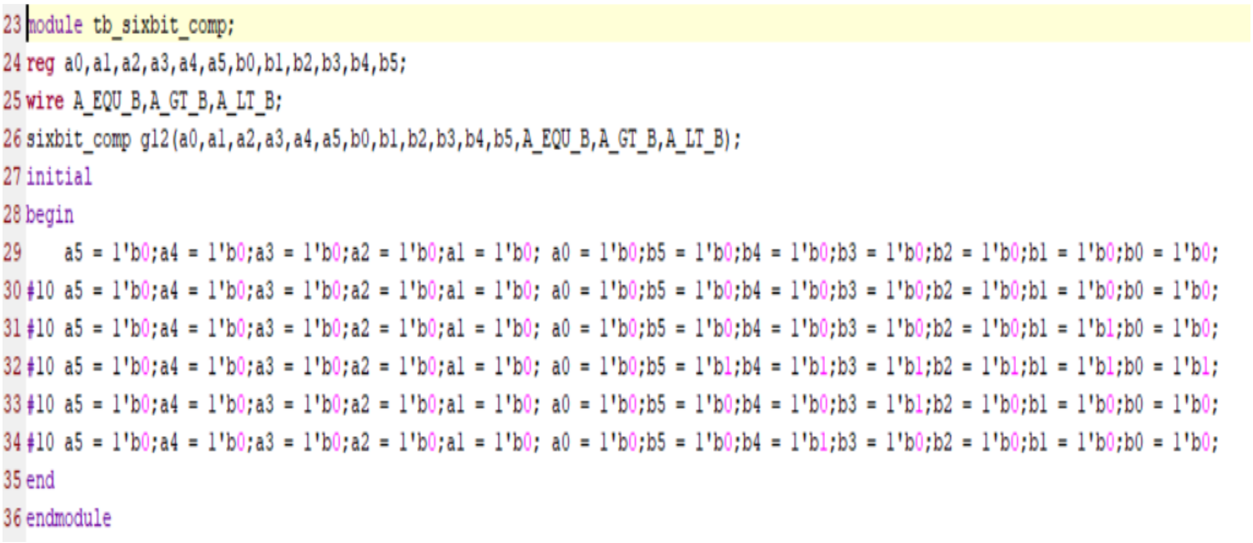
```
module tb_fourbit_comp;
reg a0,a1,a2,a3,b0,b1,b2,b3;
wire A_LT_B,A_GT_B,A_EQU_B;
fourbit_comp s1(a0,a1,a2,a3,b0,b1,b2,b3,A_LT_B,A_GT_B,A_EQU_B);
initial
begin
    a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b1;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b3 = 1'b1;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b1;a1 = 1'b0; a0 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b3 = 1'b0;b2 = 1'b1;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b1; a0 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b1;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b1;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b1;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b1;
end
endmodule
```

6bit comparator:

```
module sixbit_comp(a0,a1,a2,a3,a4,a5,b0,b1,b2,b3,b4,b5,A_EQU_B,A_GT_B,A_LT_B);

input a0,a1,a2,a3,a4,a5,b0,b1,b2,b3,b4,b5;

output A_EQU_B,A_GT_B,A_LT_B;

wire x1,x2,x3,x4,x5,x6,x7,x8,x9,y1,y2,y3,y4,y5,y6,y7,y8,y9,y10,y11,y12,y13,y14,z1,z2,z3,z4,z5,z6,z7,z8,z9,z10;

xnorgate t1(a5,b5,x1);

xnorgate t2(a4,b4,x2);

xnorgate t3(a3,b3,x3);

xnorgate t4(a2,b2,x4);

xnorgate t5(a1,b1,x5);

xnorgate t6(a0,b0,x6);

andgate t7(x1,x2,x7);

andgate t8(x3,x4,x8);

andgate t9(x5,x6,x9);

andgate1 t10(x7,x8,x9,A_EQU_B);

andgate t11(a5,(~b5),y1);

andgate t12(a4,(~b4),y2);

andgate t13(a3,(~b3),y3);
andgate t14(a2,(~b2),y4);
andgate t15(a1,(~b1),y5);
andgate t16(a0,(~b0),y6);
andgate t17(x1,y2,y7);
andgate t18(x2,y3,y8);
andgate t19(x3,y4,y9);
andgate t20(x4,y5,y10);
andgate t21(x5,y6,y11);
orgate t22(y1,y7,y12);
orgate t23(y8,y9,y13);
orgate t24(y10,y11,y14);
orgate1 t25(y12,y13,y14,A_GT_B);
andgate t26((~a5),b5,z1);
andgate t27((~a4),b4,z2);
andgate t28((~a3),b3,z3);
andgate t29((~a2),b2,z4);
andgate t30((~a1),b1,z5);
andgate t31((~a0),b0,z6);
andgate t32(x1,z2,z7);
andgate t33(x2,z3,z8);
andgate t34(x3,z4,z9);
andgate t35(x4,z5,z10);
andgate t36(x5,z6,z11);
orgate t37(z1,z7,z12);
orgate t38(z8,z9,z13);
orgate t39(z10,z11,z14);
orgate1 t40(z12,z13,z14,A_LT_B);
endmodule
module xnorgate(x,y,z);
input x,y;
output z;
assign z = ~(x ^ y);
endmodule
module andgate(x,y,z);
input x,y;
output z;
assign z = x & y;
endmodule
module andgate1(x,y,z,m);
input x,y,z;
output m;
assign m = x & y & z;
endmodule
module orgate(x1,y1,b);
```

```
input x1,y1;
output b;
assign b = x1 | y1 ;
endmodule
module orgate1(x1,y1,z1,b);
input x1,y1,z1;
output b;
assign b = x1 | y1 | z1;
Endmodule
```

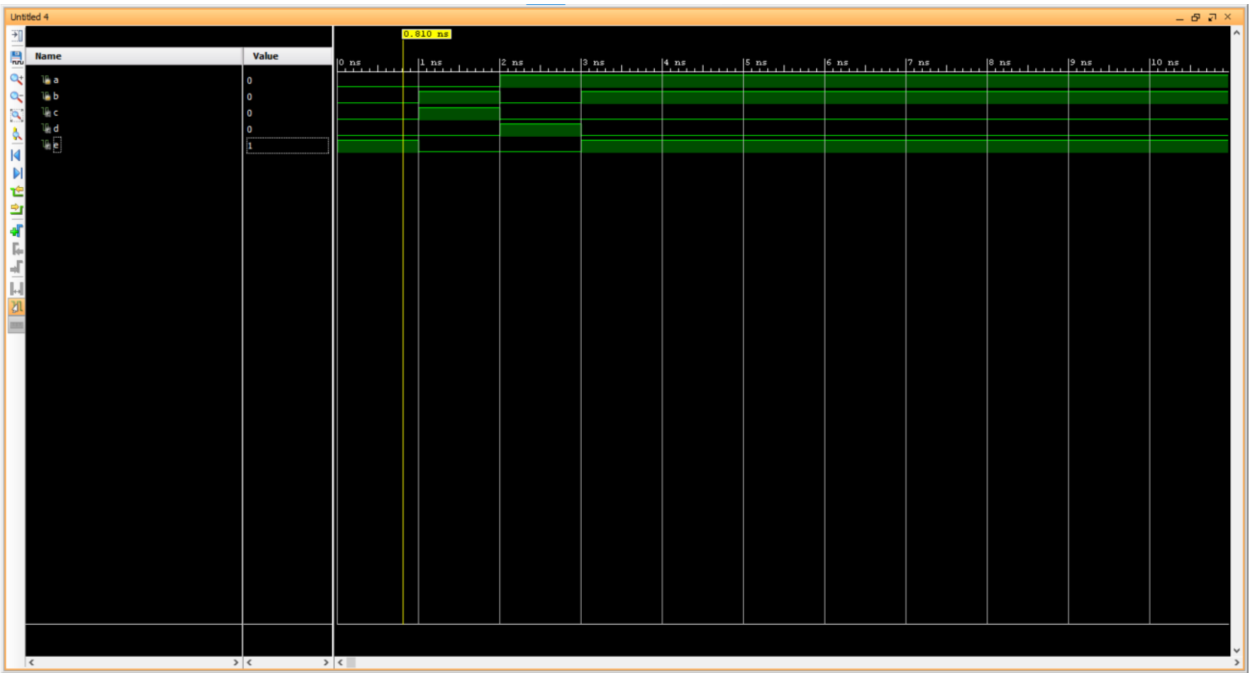
Test bench code:



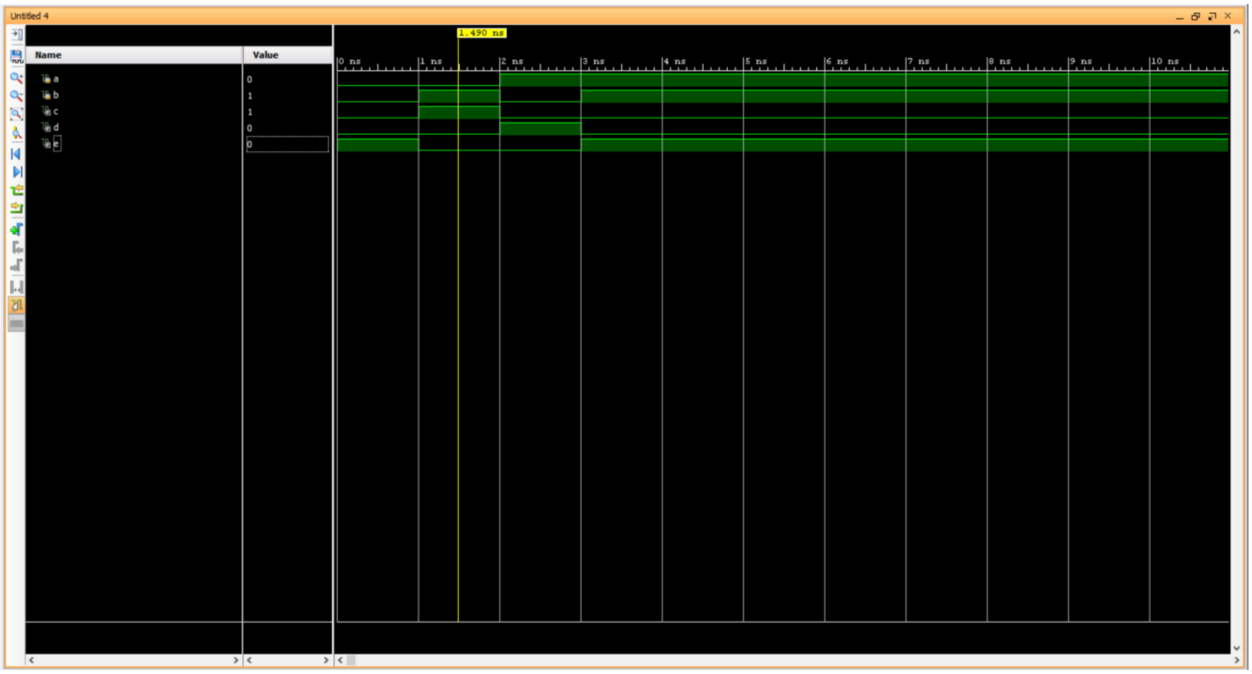
```
module tb_sixbit_comp;
reg a0,a1,a2,a3,a4,a5,b0,b1,b2,b3,b4,b5;
wire A_EQU_B,A_GT_B,A_LT_B;
sixbit_comp g12(a0,a1,a2,a3,a4,a5,b0,b1,b2,b3,b4,b5,A_EQU_B,A_GT_B,A_LT_B);
initial
begin
    a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b0;b4 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b0;b4 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b0;b4 = 1'b0;b3 = 1'b0;b2 = 1'b0;b1 = 1'b1;b0 = 1'b0;
#10 a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b1;b4 = 1'b1;b3 = 1'b1;b2 = 1'b1;b1 = 1'b1;b0 = 1'b1;
#10 a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b0;b4 = 1'b0;b3 = 1'b1;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
#10 a5 = 1'b0;a4 = 1'b0;a3 = 1'b0;a2 = 1'b0;a1 = 1'b0; a0 = 1'b0;b5 = 1'b0;b4 = 1'b1;b3 = 1'b0;b2 = 1'b0;b1 = 1'b0;b0 = 1'b0;
end
endmodule
```

Results:

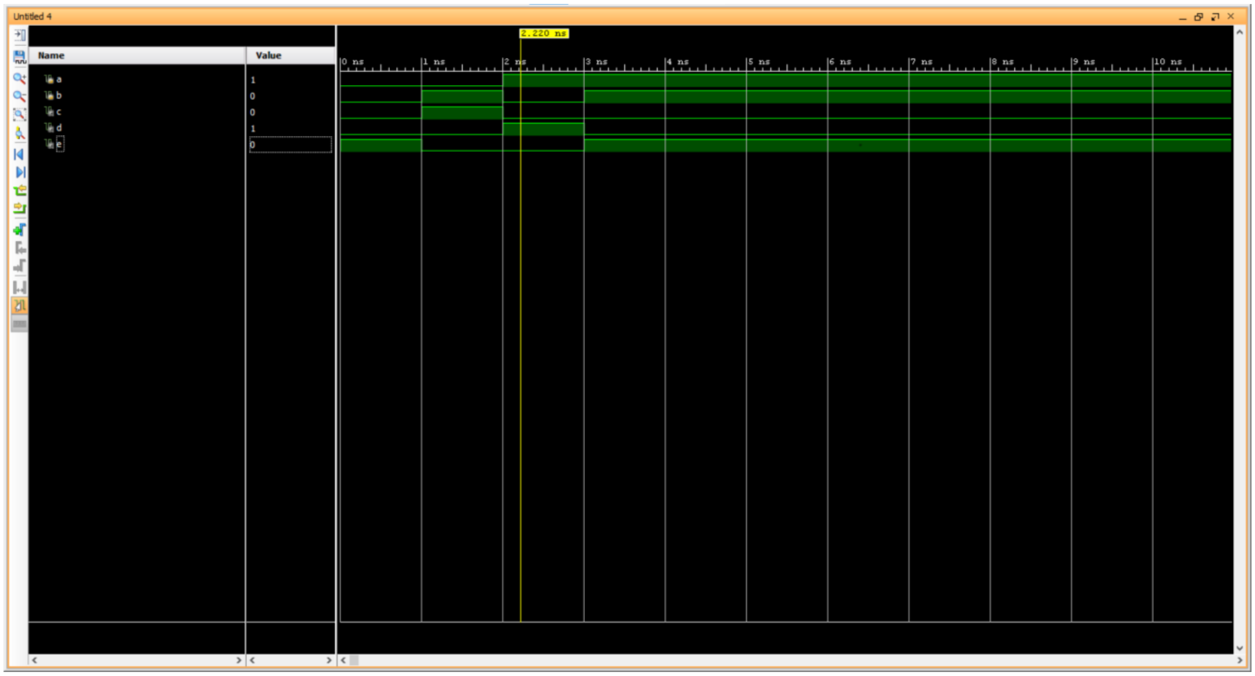
1bit comparator:



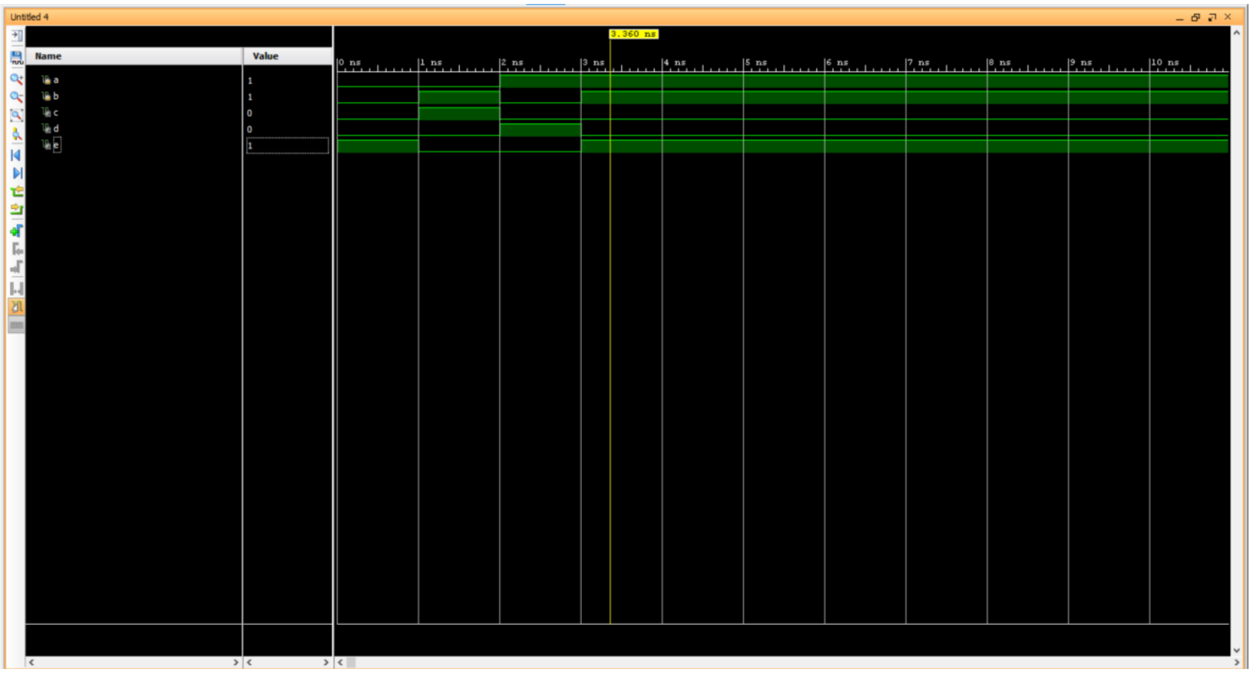
Name	Value
a	0
b	0
c	0
d	0
e	1



Name	Value
a	0
b	1
c	1
d	0
e	0

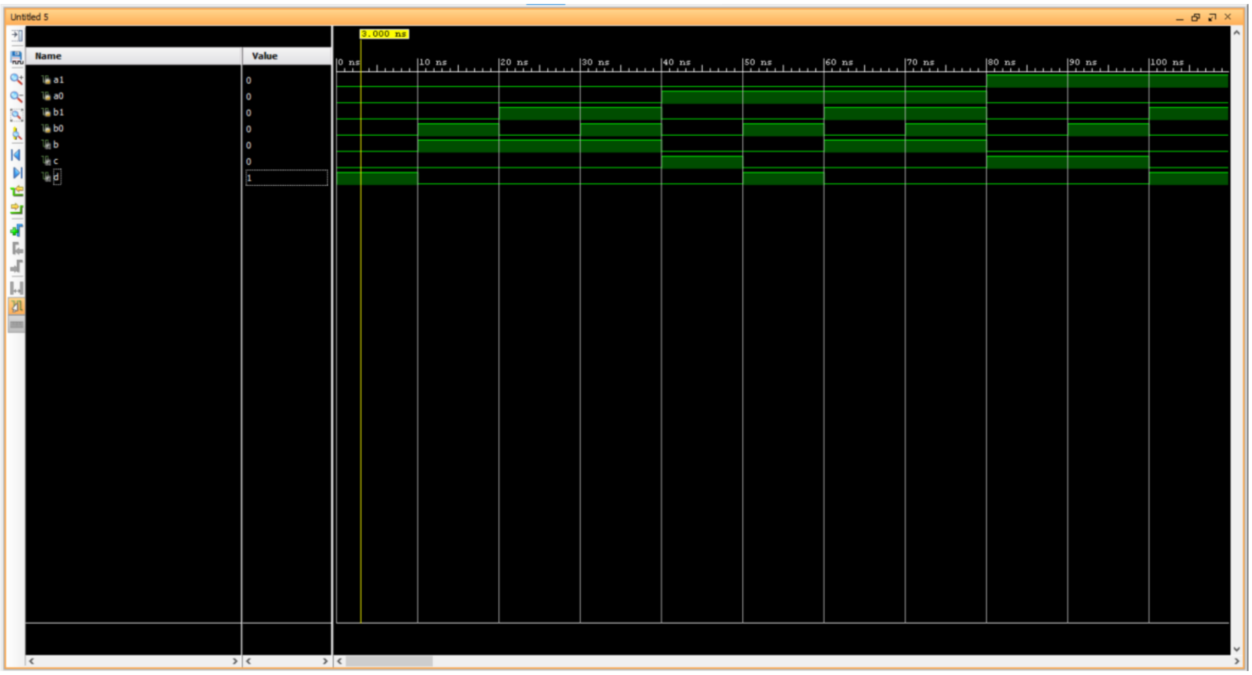


Name	Value
a	1
b	0
c	0
d	1
e	0



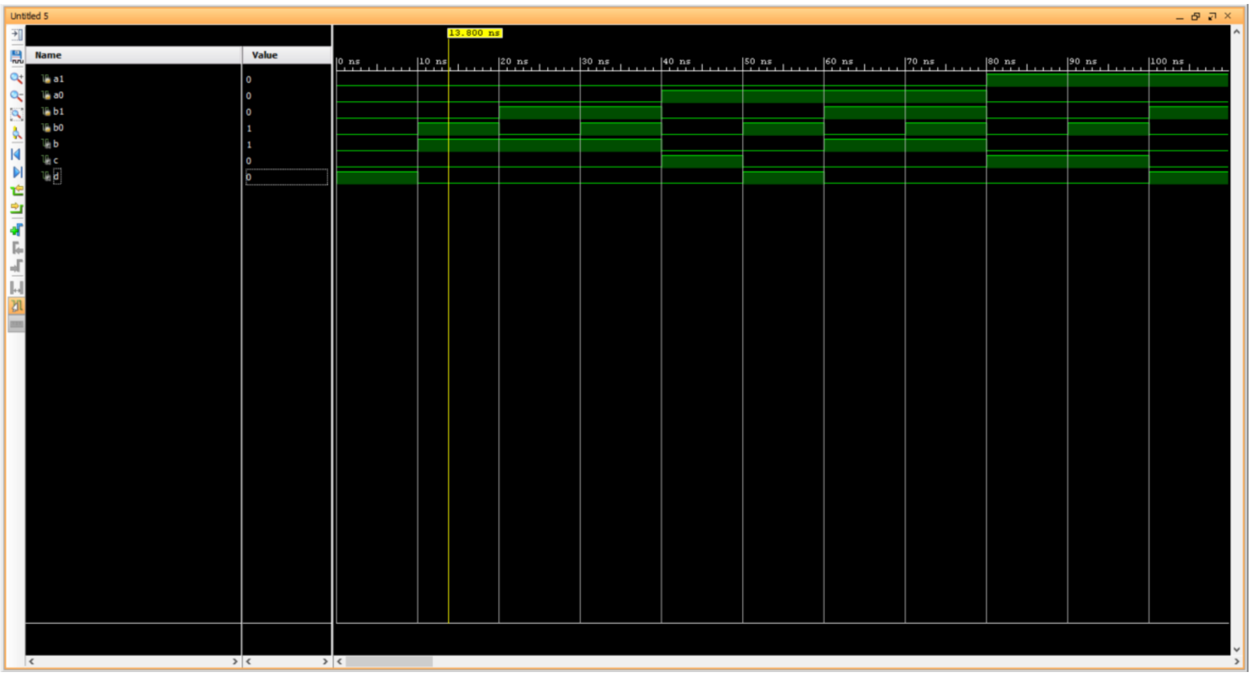
Name	Value
a	1
b	1
c	0
d	0
e	1

2bit comparator:



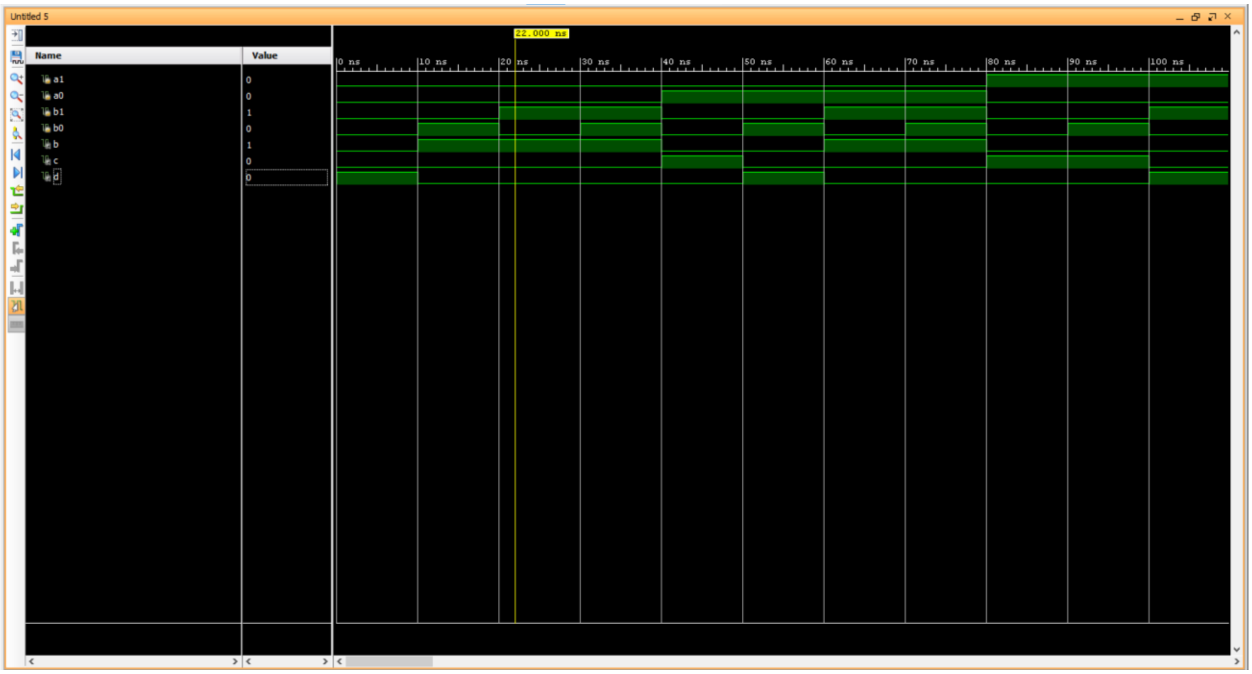
Untitled 5

Name	Value
a1	0
a0	0
b1	0
b0	0
b	0
c	0
d	1

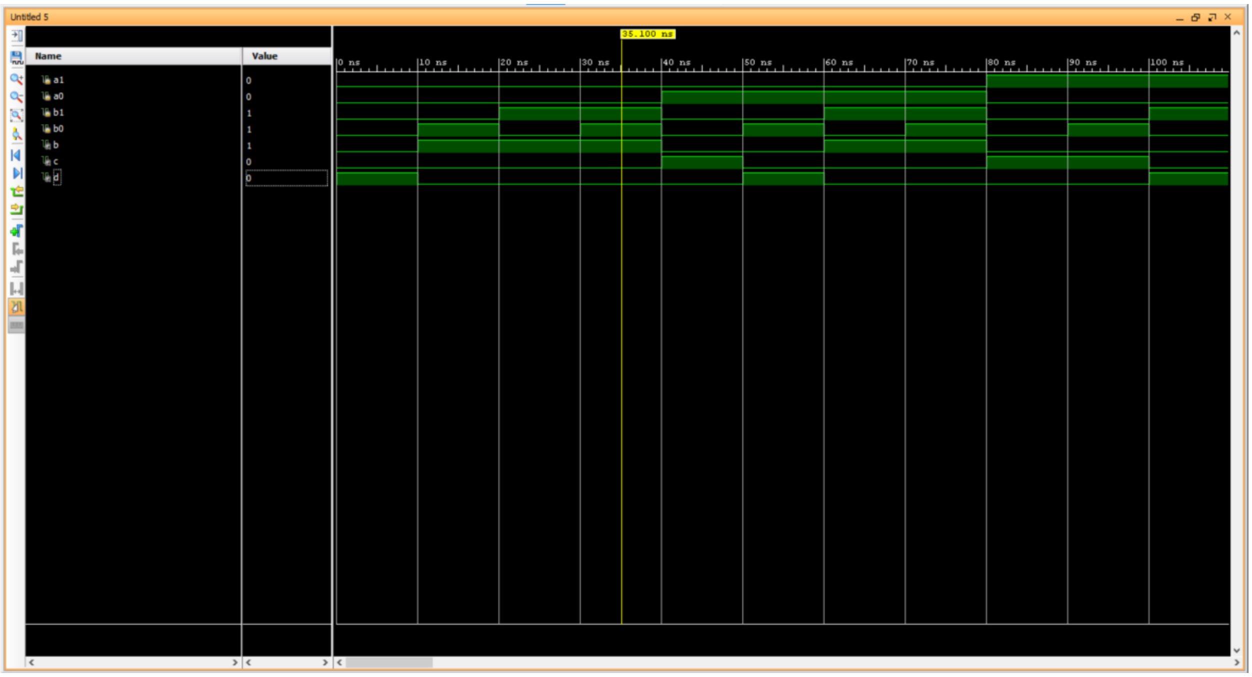


Untitled 5

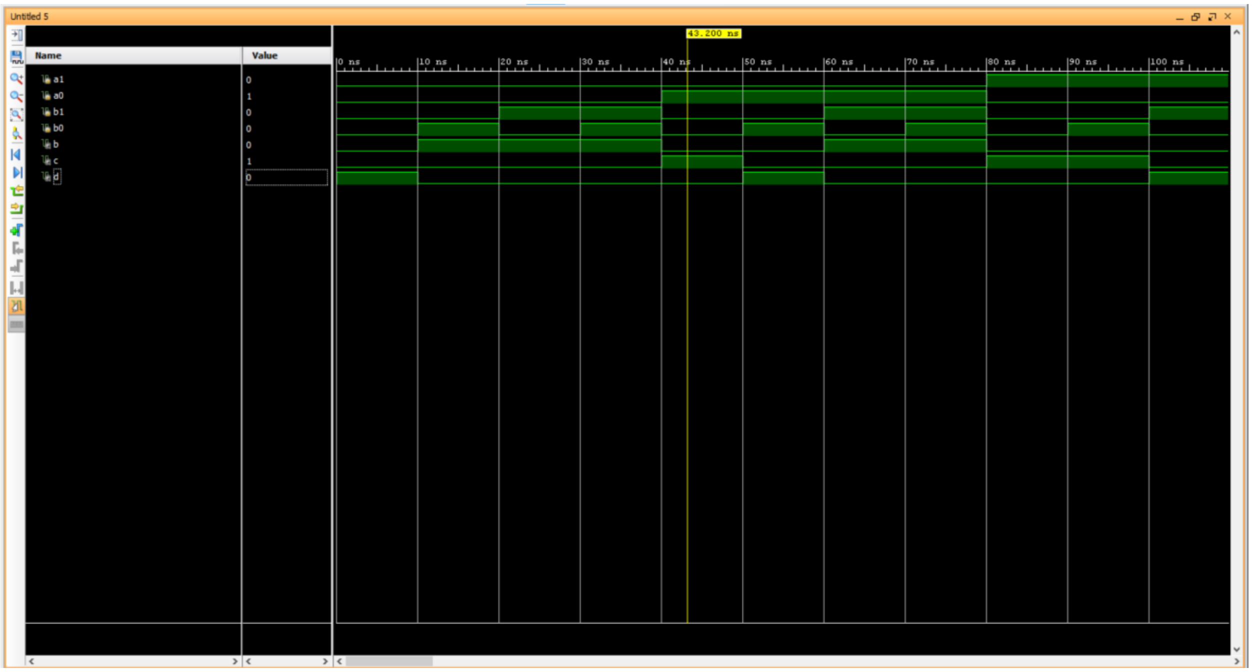
Name	Value
a1	0
a0	0
b1	0
b0	1
b	1
c	0
d	0



Name	Value
a1	0
a0	0
b1	1
b0	0
b	1
c	0
d	0

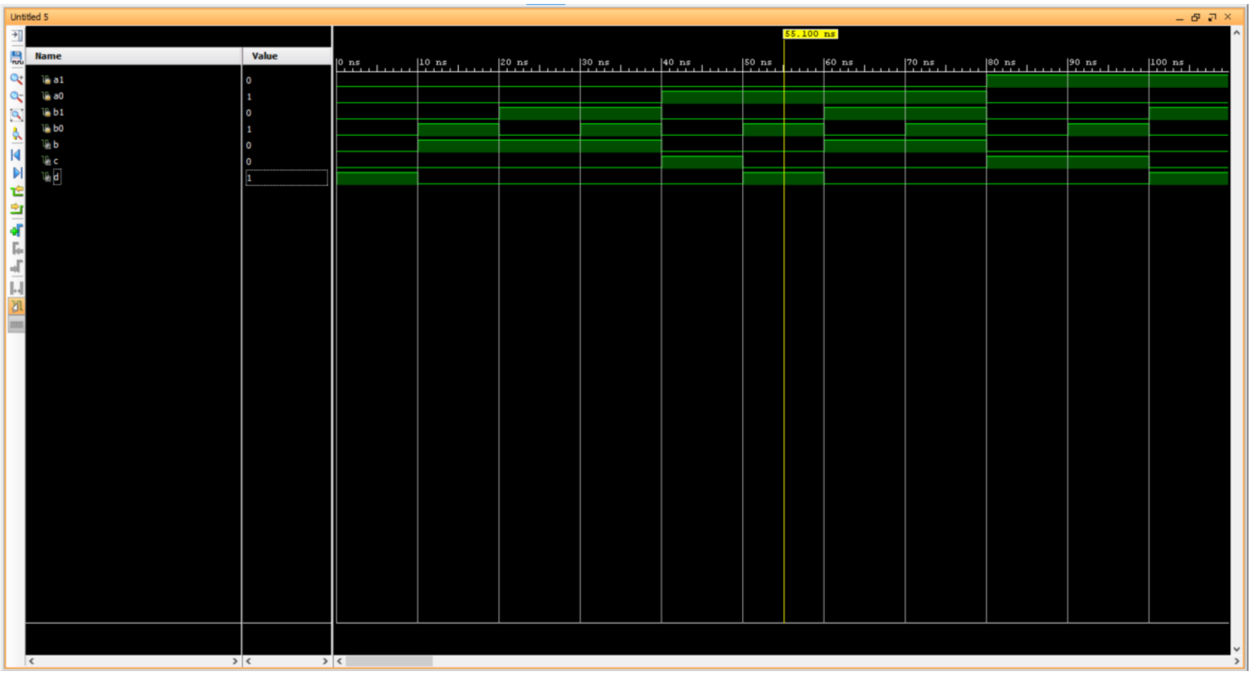


Name	Value
a1	0
a0	0
b1	1
b0	1
b	1
c	0
d	0



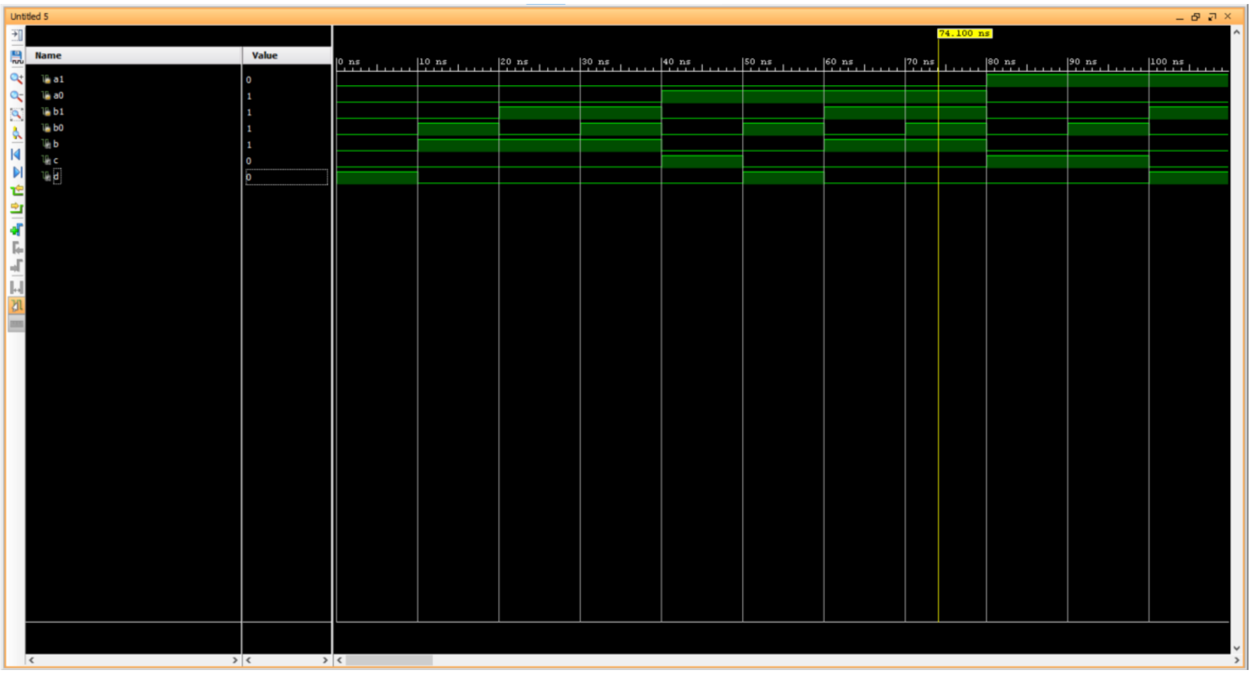
Untitled 5

Name	Value
a1	0
a0	1
b1	0
b0	0
b	0
c	1
d	0



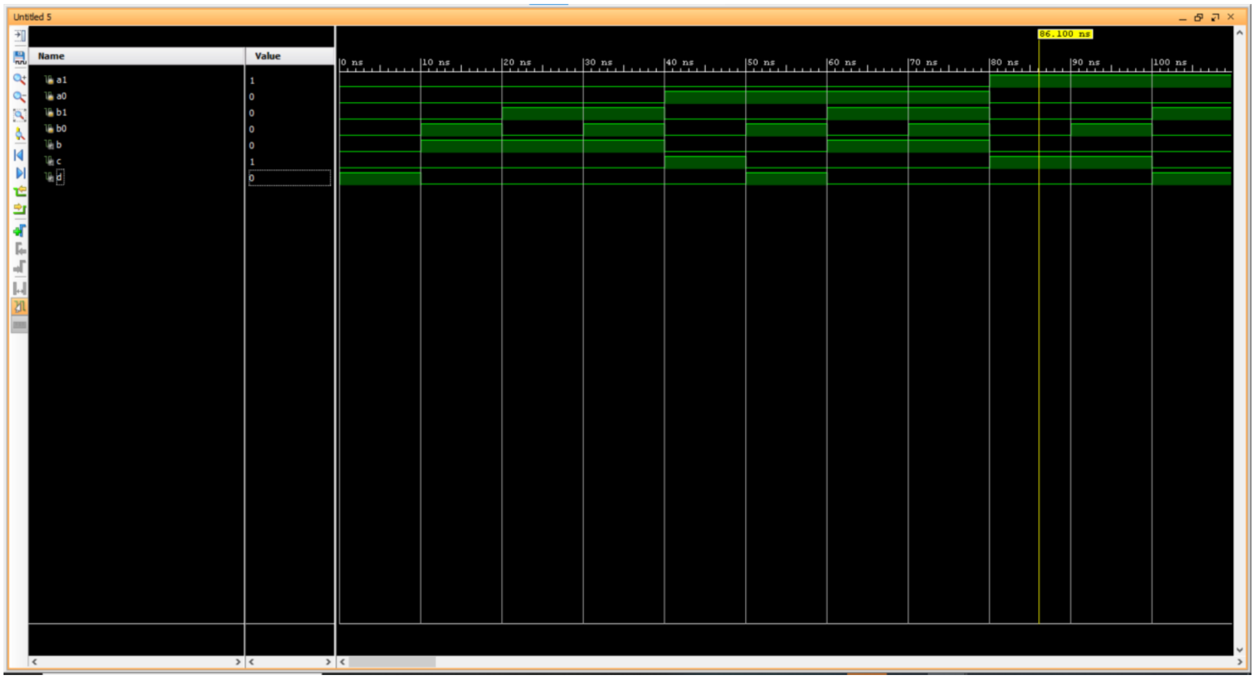
Untitled 5

Name	Value
a1	0
a0	1
b1	0
b0	1
b	0
c	0
d	1



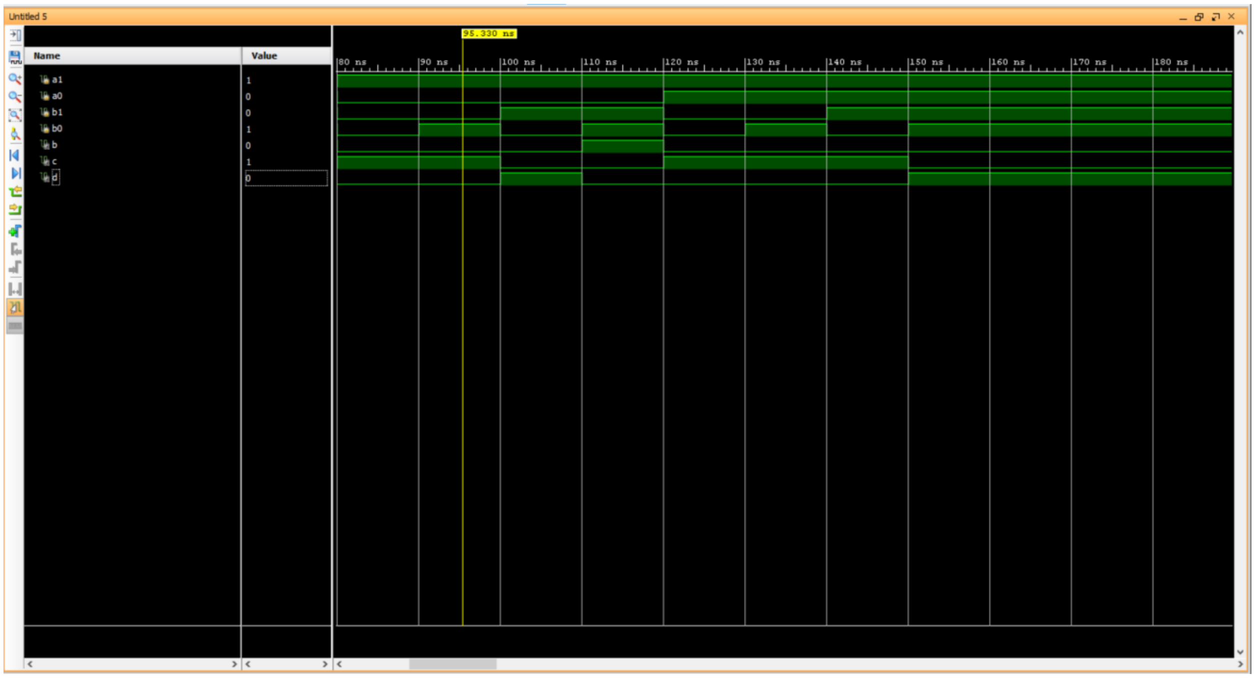
Untitled 5

Name	Value
a1	0
a0	1
b1	1
b0	1
b	1
c	0
d	0

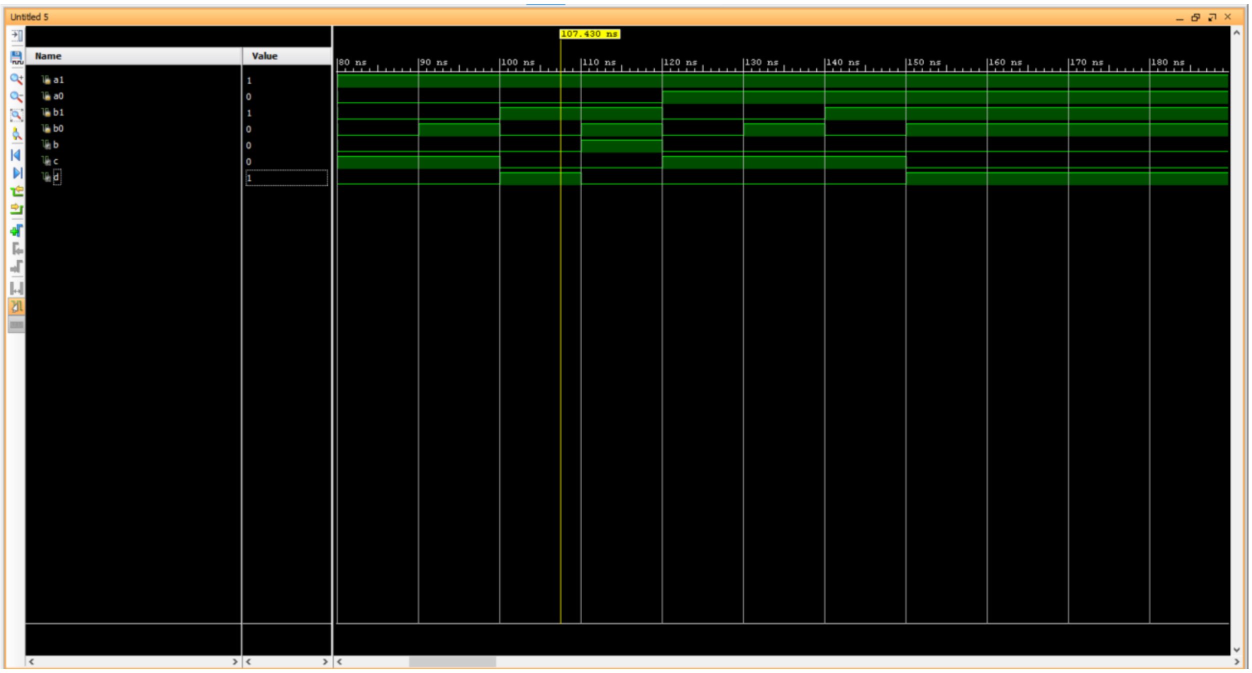


Untitled 5

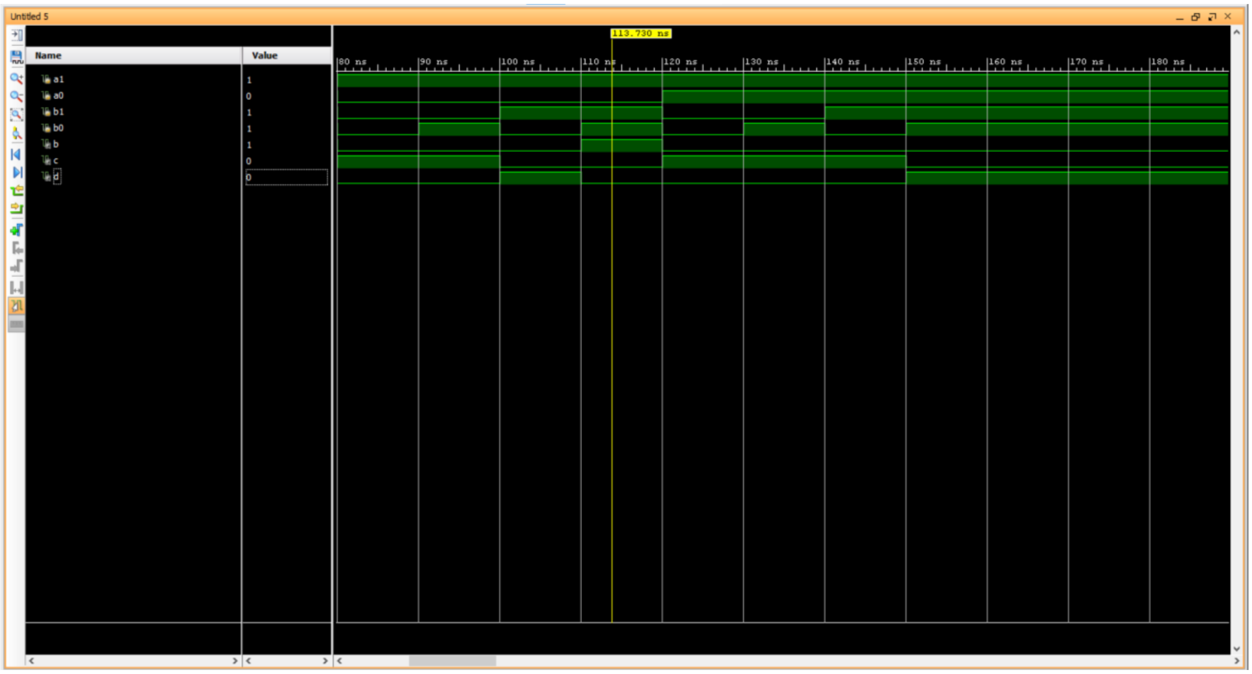
Name	Value
a1	1
a0	0
b1	0
b0	0
b	0
c	1
d	0



Name	Value
a1	1
a0	0
b1	0
b0	1
b	0
c	1
d	0

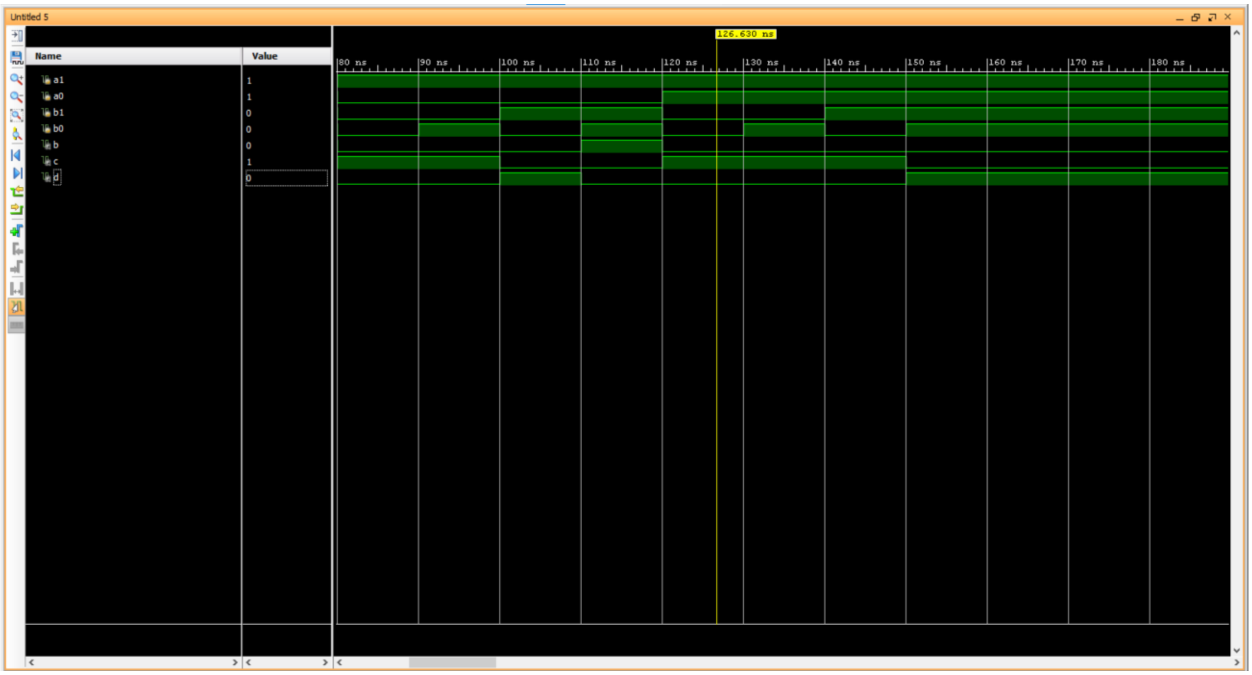


Name	Value
a1	1
a0	0
b1	1
b0	0
b	0
c	0
d	1



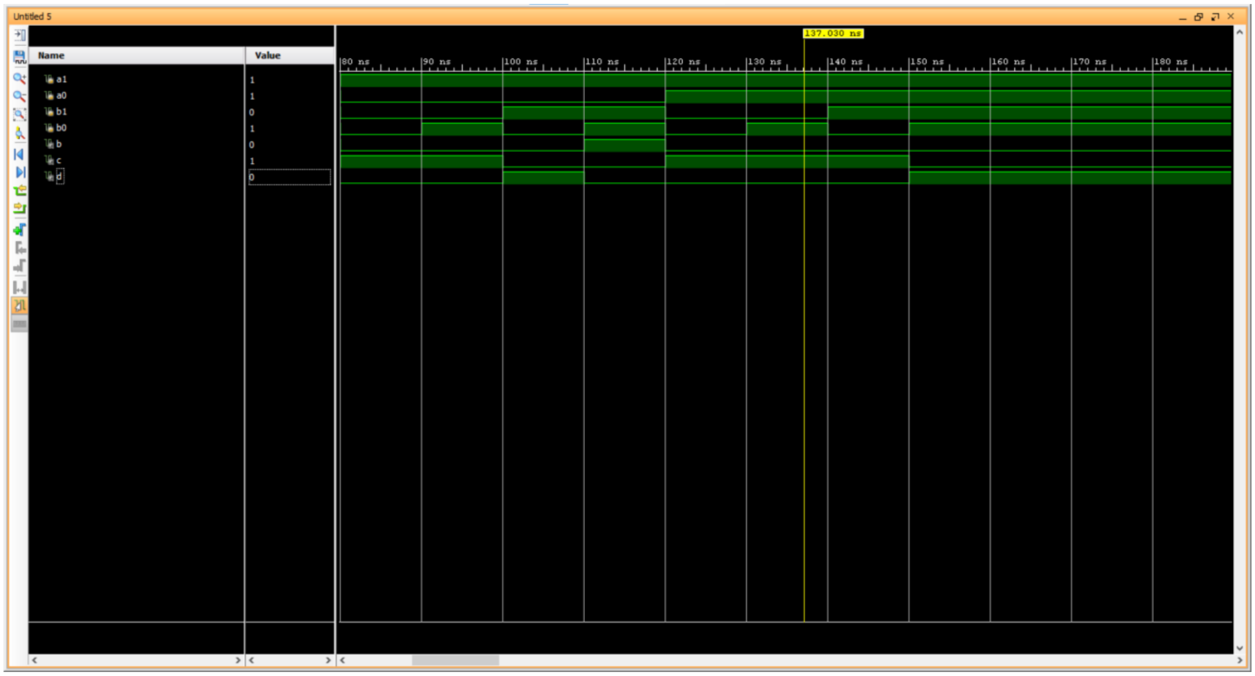
Untitled 5

Name	Value
a1	1
a0	0
b1	1
b0	1
b	1
c	0
d	0



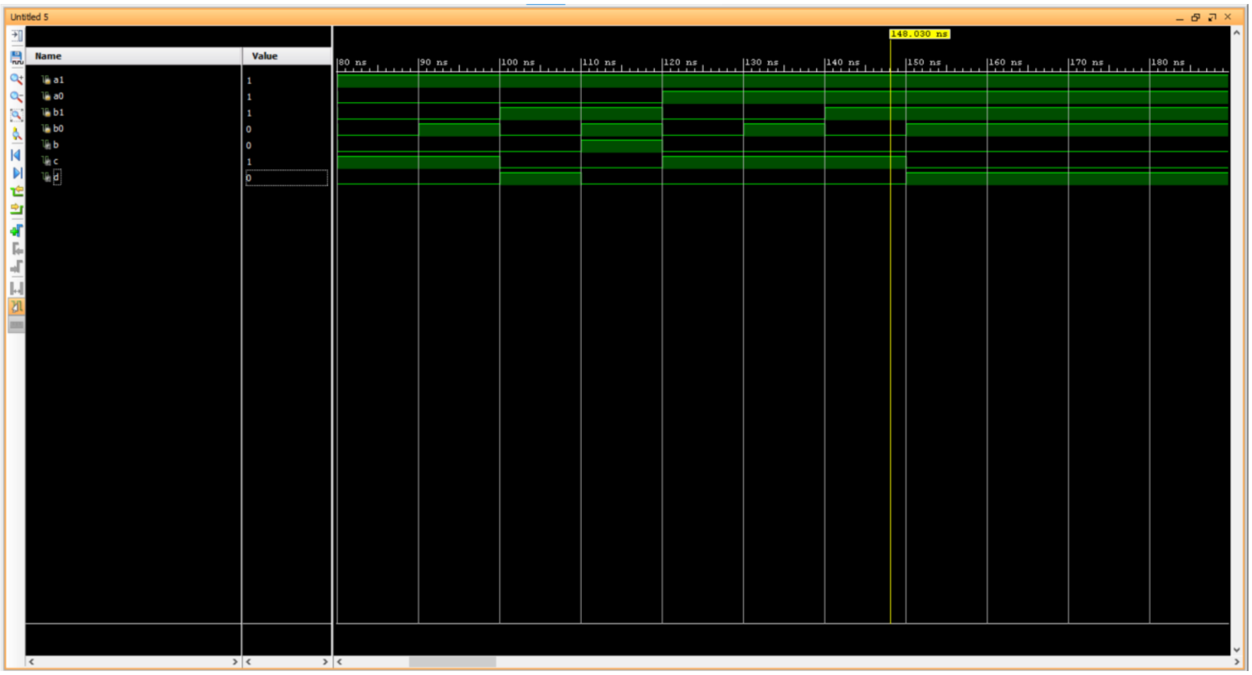
Untitled 5

Name	Value
a1	1
a0	1
b1	0
b0	0
b	0
c	1
d	0



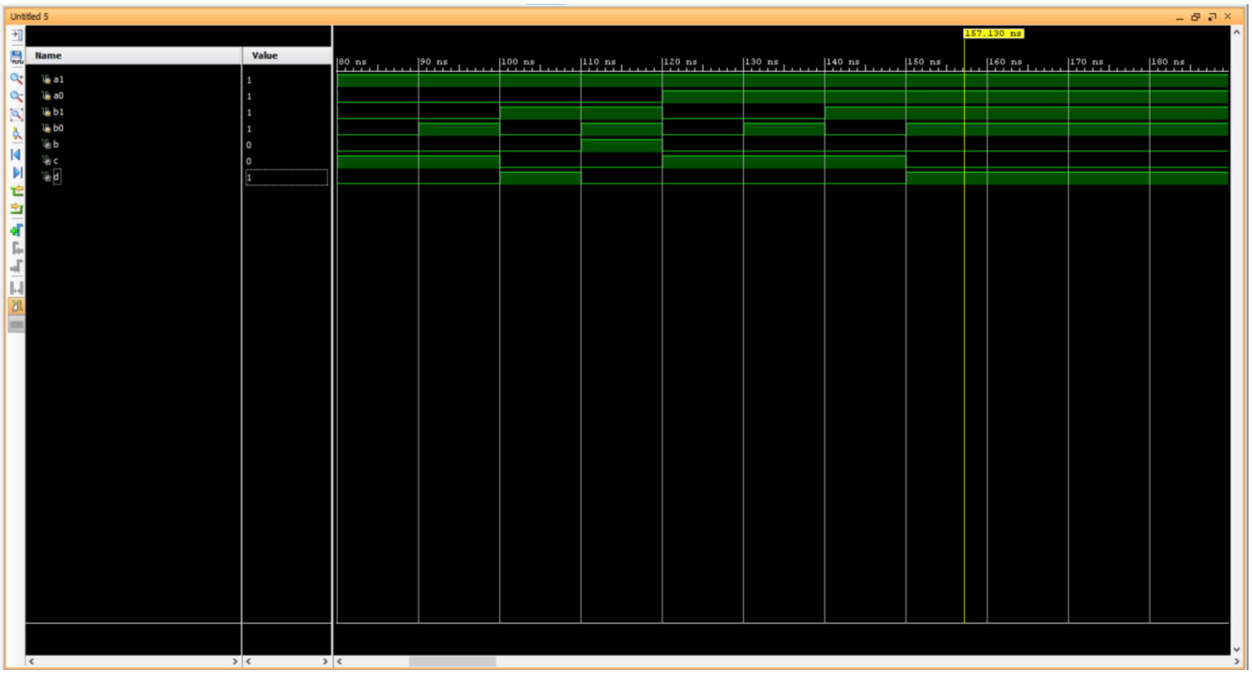
Untitled 5

Name	Value
a1	1
a0	1
b1	0
b0	1
b	0
c	1
d	0



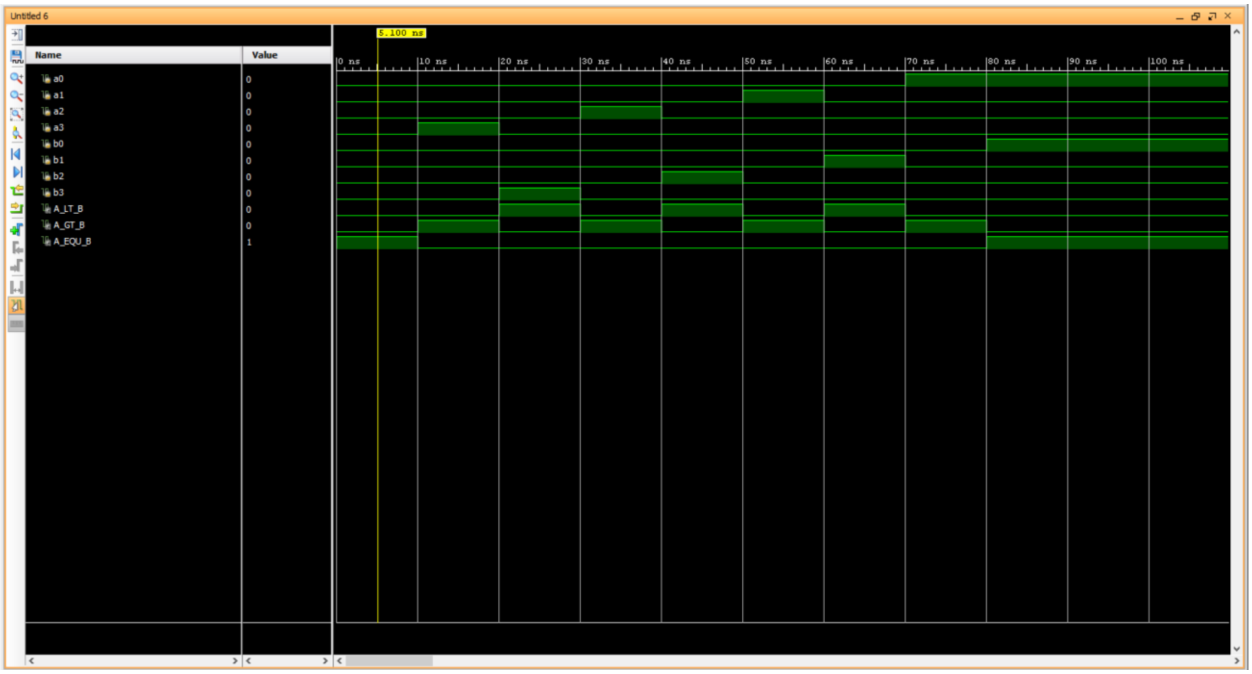
Untitled 5

Name	Value
a1	1
a0	1
b1	1
b0	0
b	0
c	1
d	0

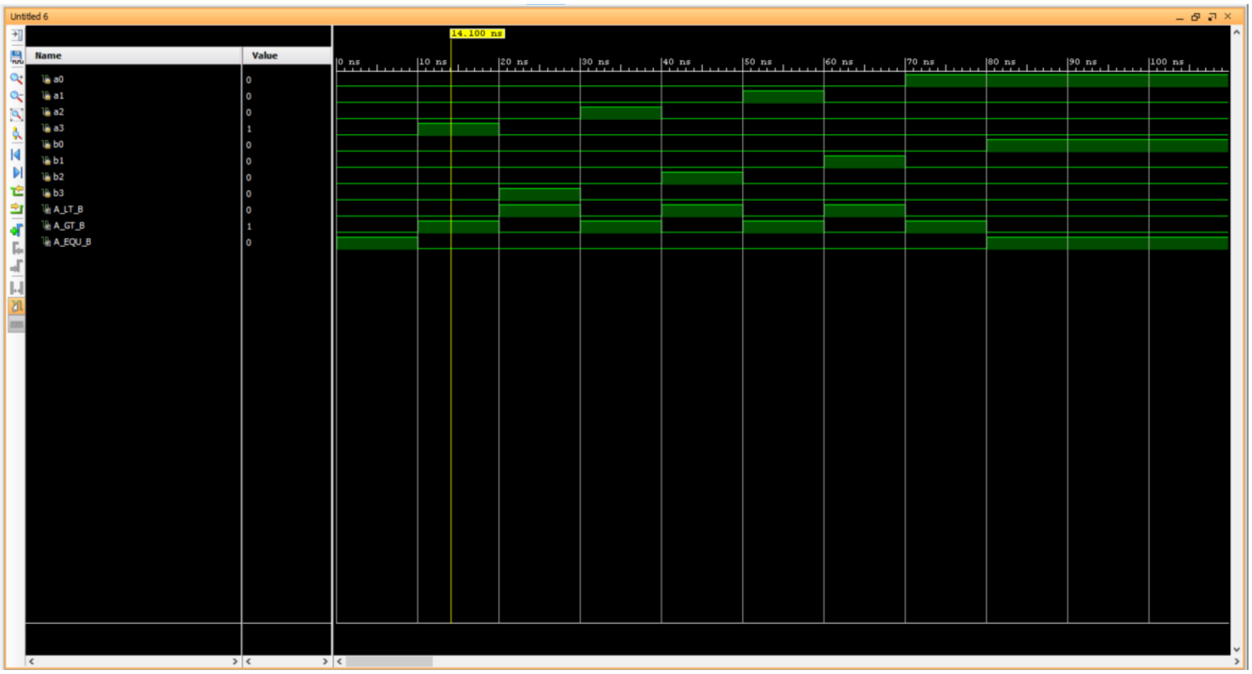


Name	Value
a1	1
a0	1
b1	1
b0	1
b	0
c	0
d	1

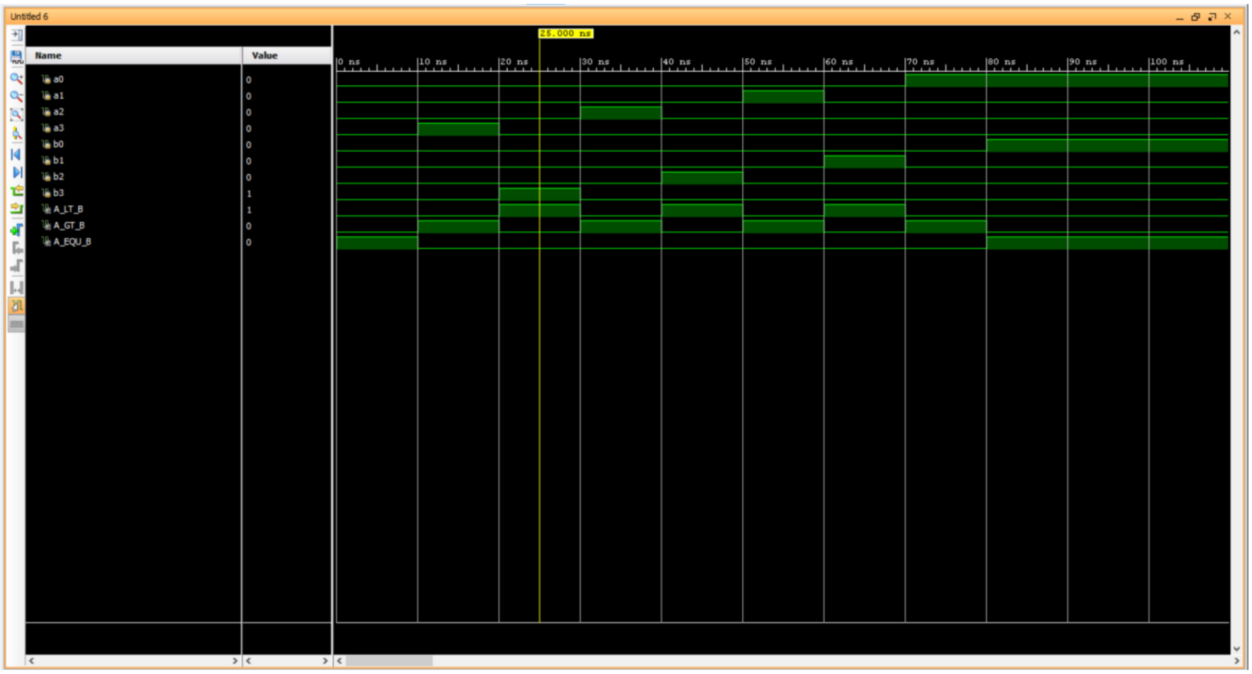
4bit comparator:



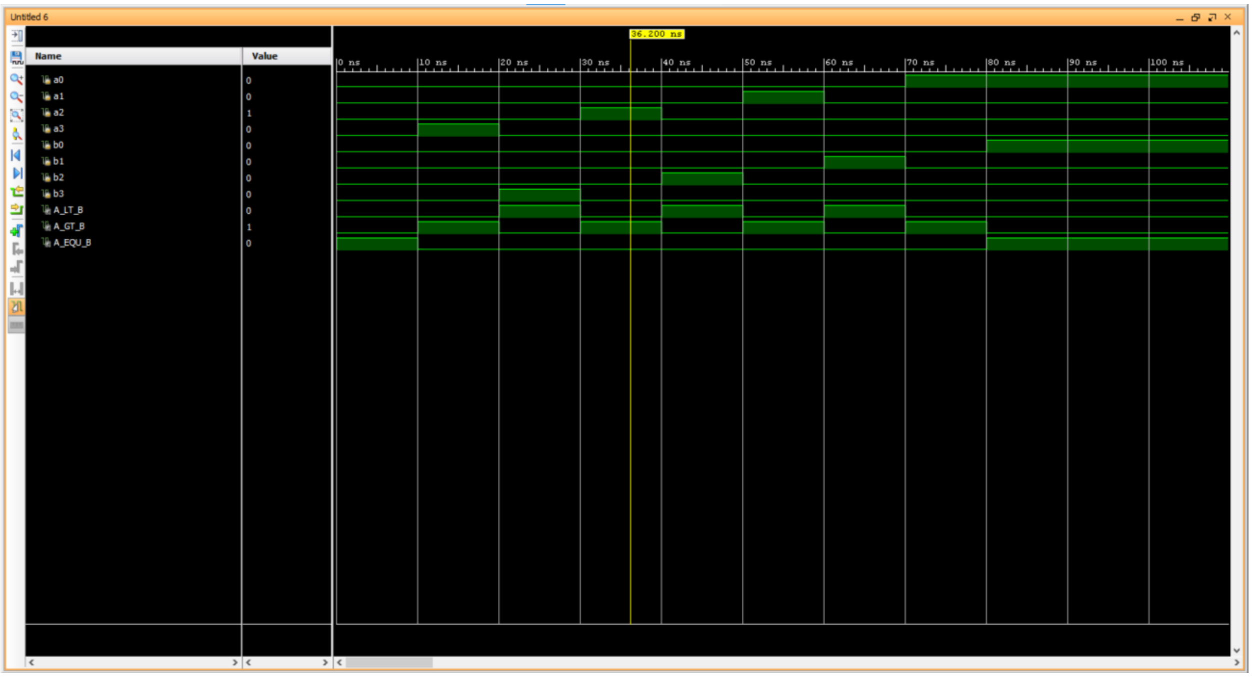
Name	Value
a0	0
a1	0
a2	0
a3	0
b0	0
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	0
A_EQU_B	1



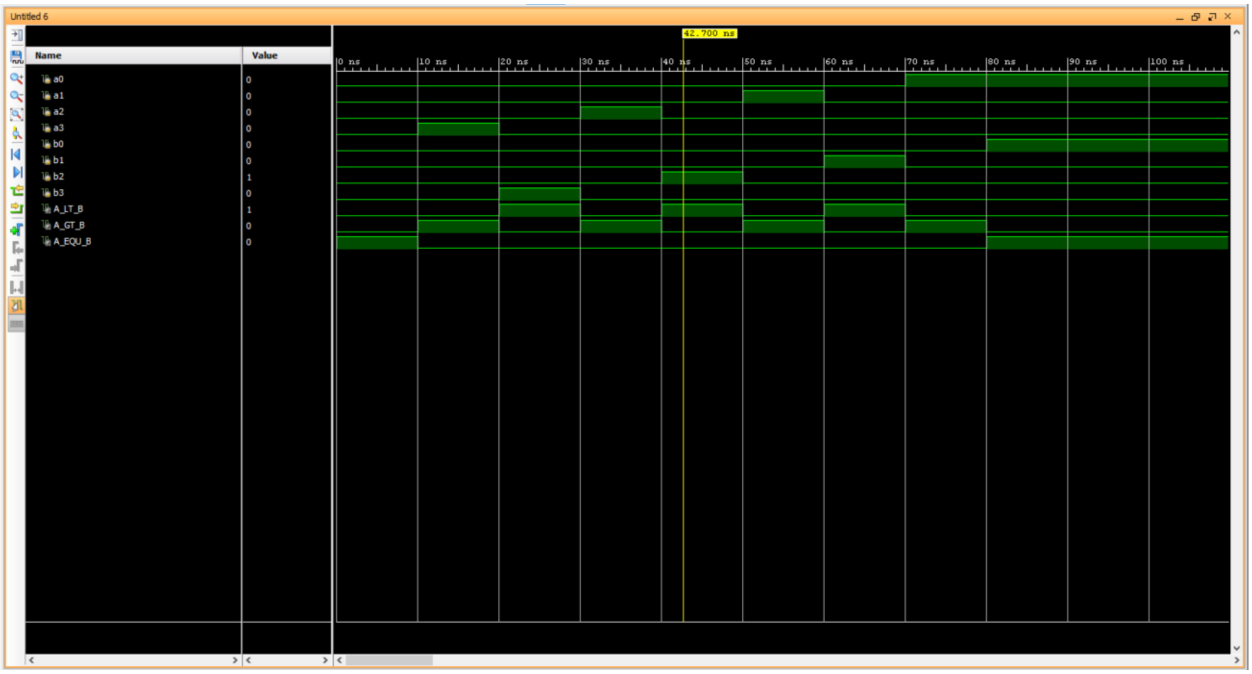
Name	Value
a0	0
a1	0
a2	0
a3	1
b0	0
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	1
A_EQU_B	0



Name	Value
a0	0
a1	0
a2	0
a3	0
b0	0
b1	0
b2	0
b3	1
A_LT_B	1
A_GT_B	0
A_EQU_B	0

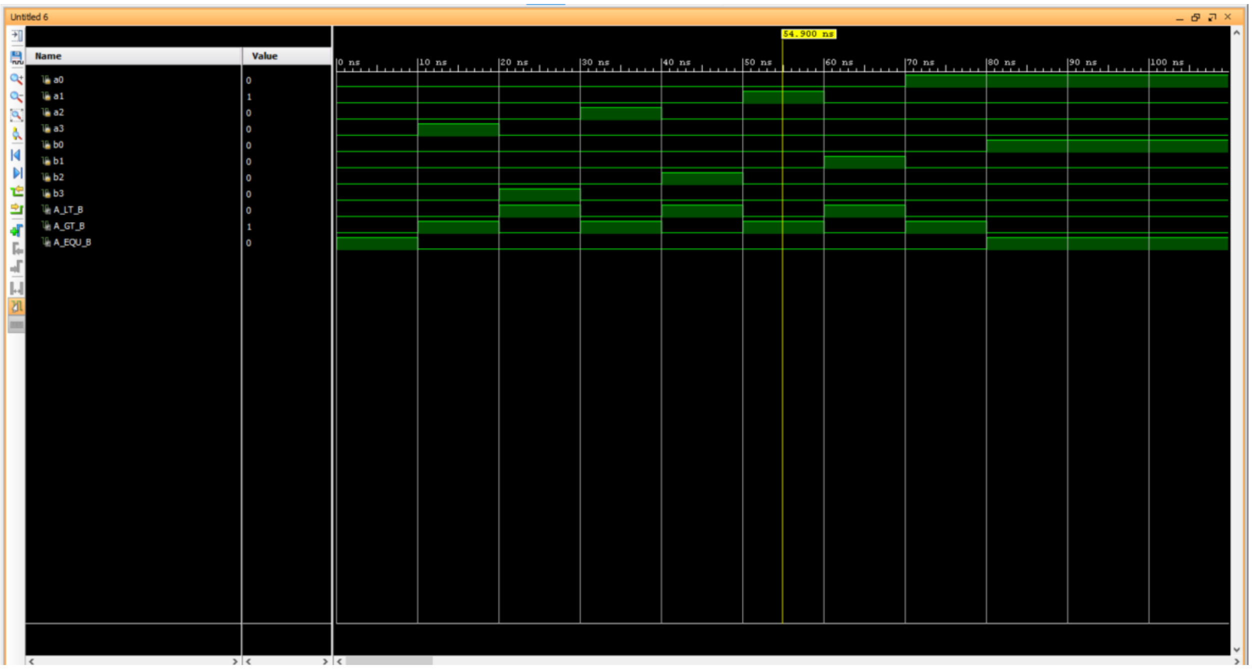


Name	Value
a0	0
a1	0
a2	1
a3	0
b0	0
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	1
A_EQU_B	0



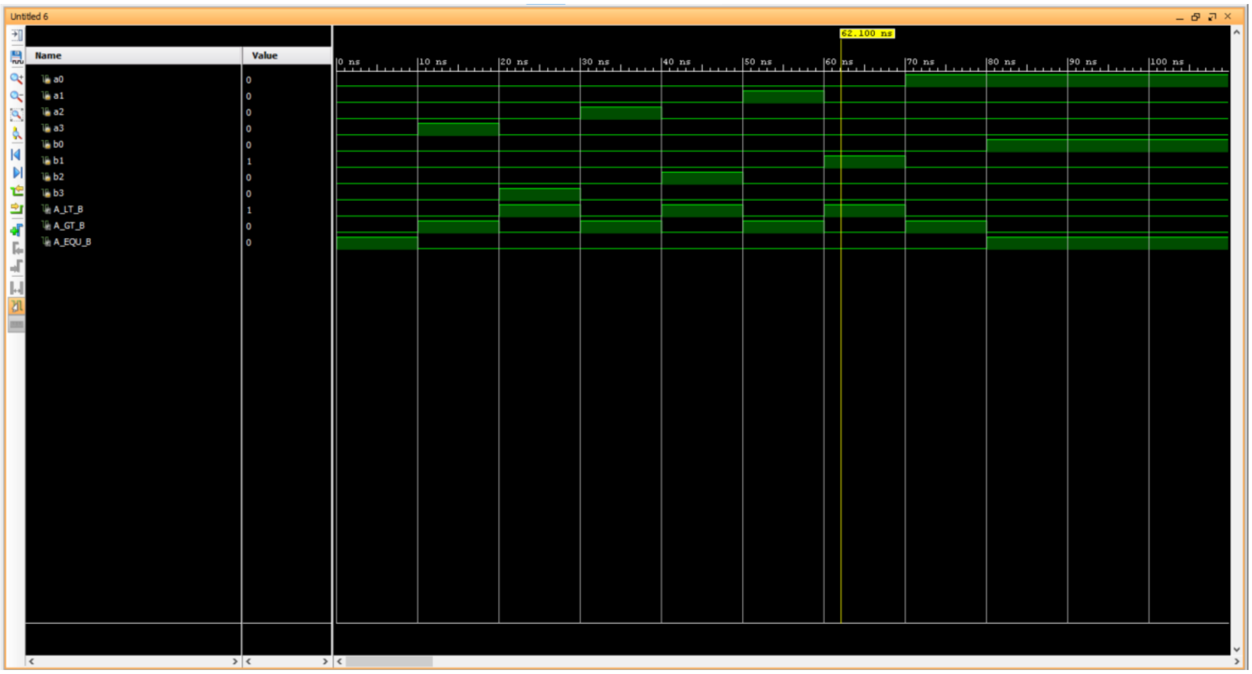
Untitled 6

Name	Value
a0	0
a1	0
a2	0
a3	0
b0	0
b1	0
b2	1
b3	0
A_LT_B	1
A_GT_B	0
A_EQU_B	0

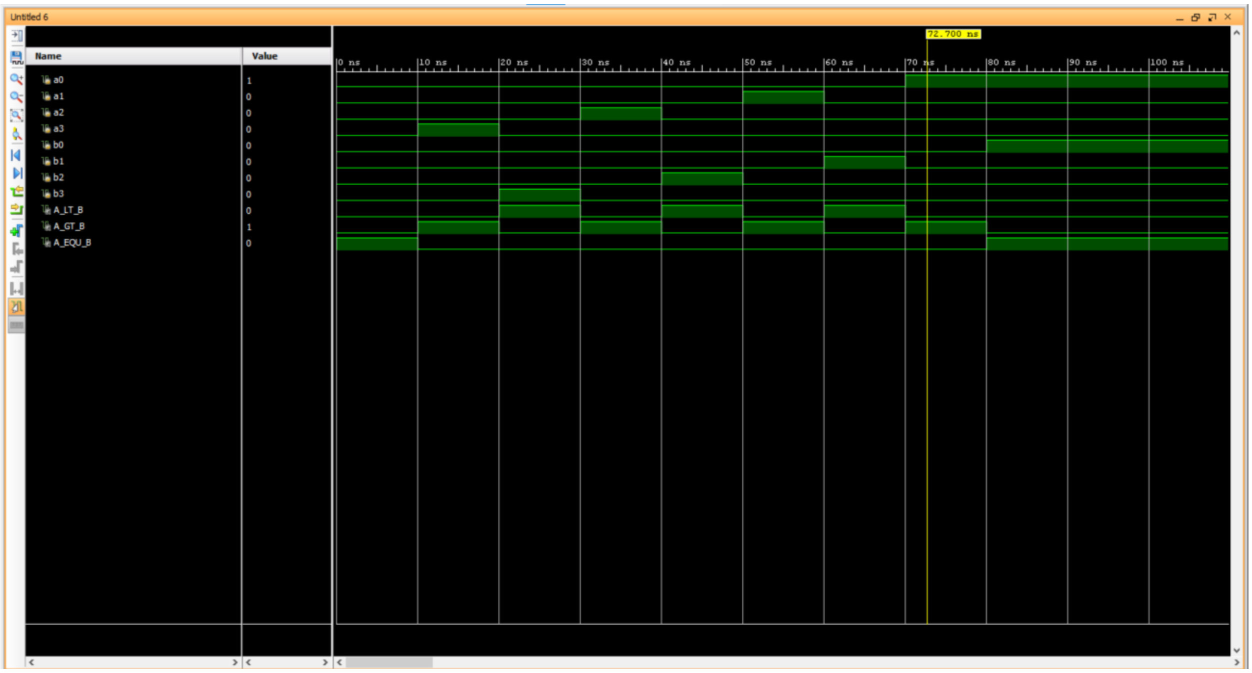


Untitled 6

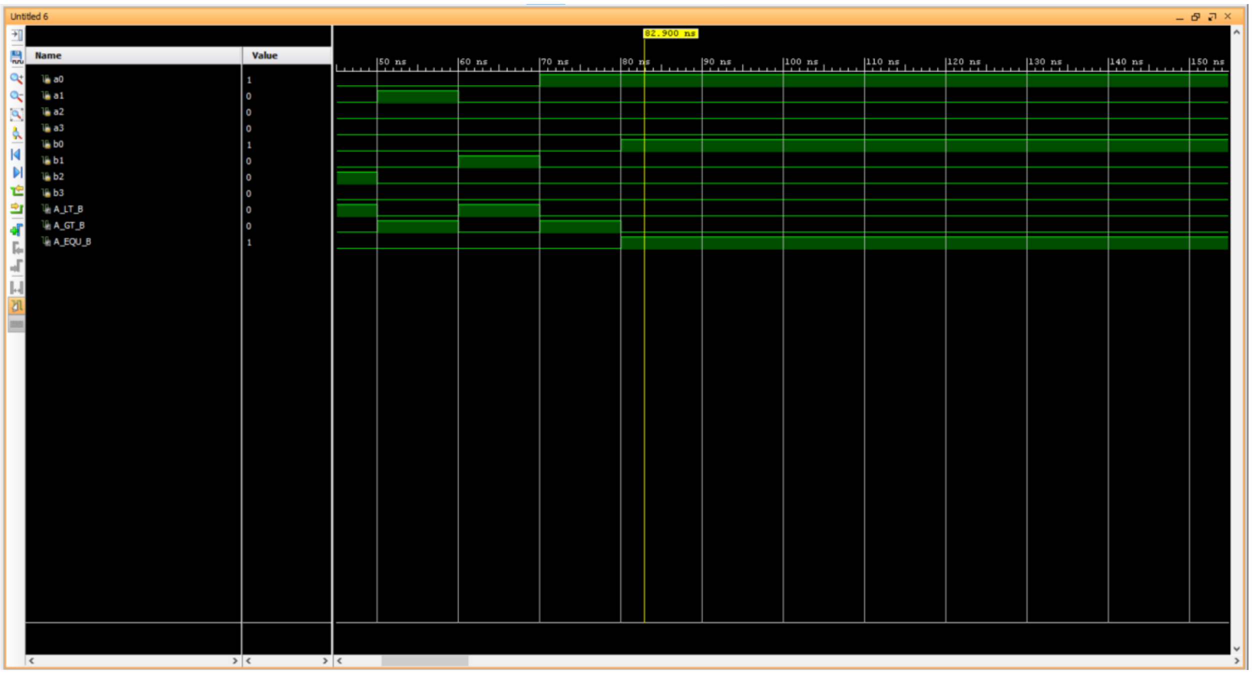
Name	Value
a0	0
a1	1
a2	0
a3	0
b0	0
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	1
A_EQU_B	0



Name	Value
a0	0
a1	0
a2	0
a3	0
b0	0
b1	1
b2	0
b3	0
A_LT_B	1
A_GT_B	0
A_EQU_B	0

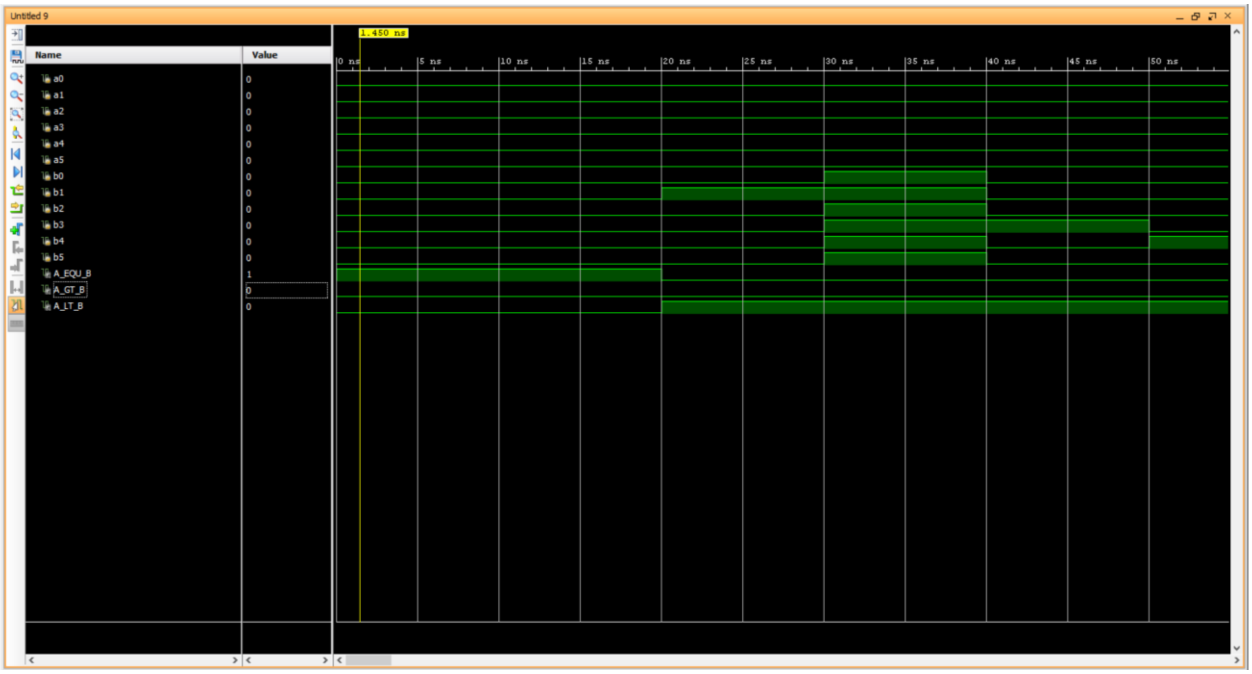


Name	Value
a0	1
a1	0
a2	0
a3	0
b0	0
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	1
A_EQU_B	0

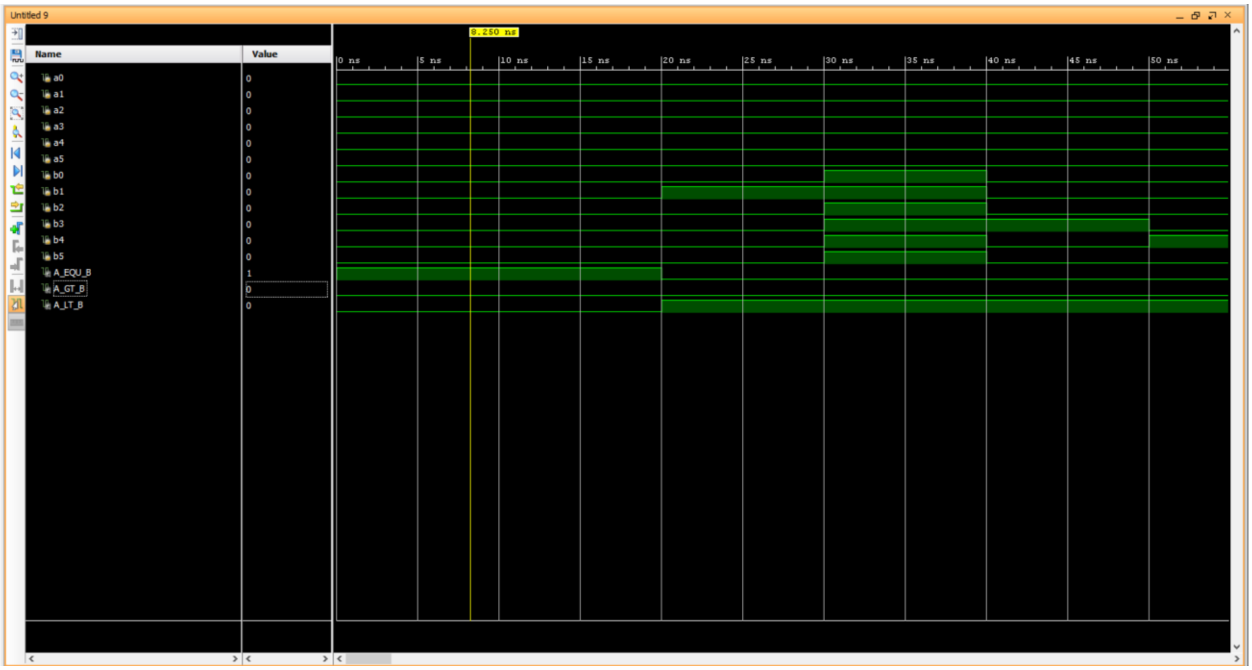


Name	Value
a0	1
a1	0
a2	0
a3	0
b0	1
b1	0
b2	0
b3	0
A_LT_B	0
A_GT_B	0
A_EQU_B	1

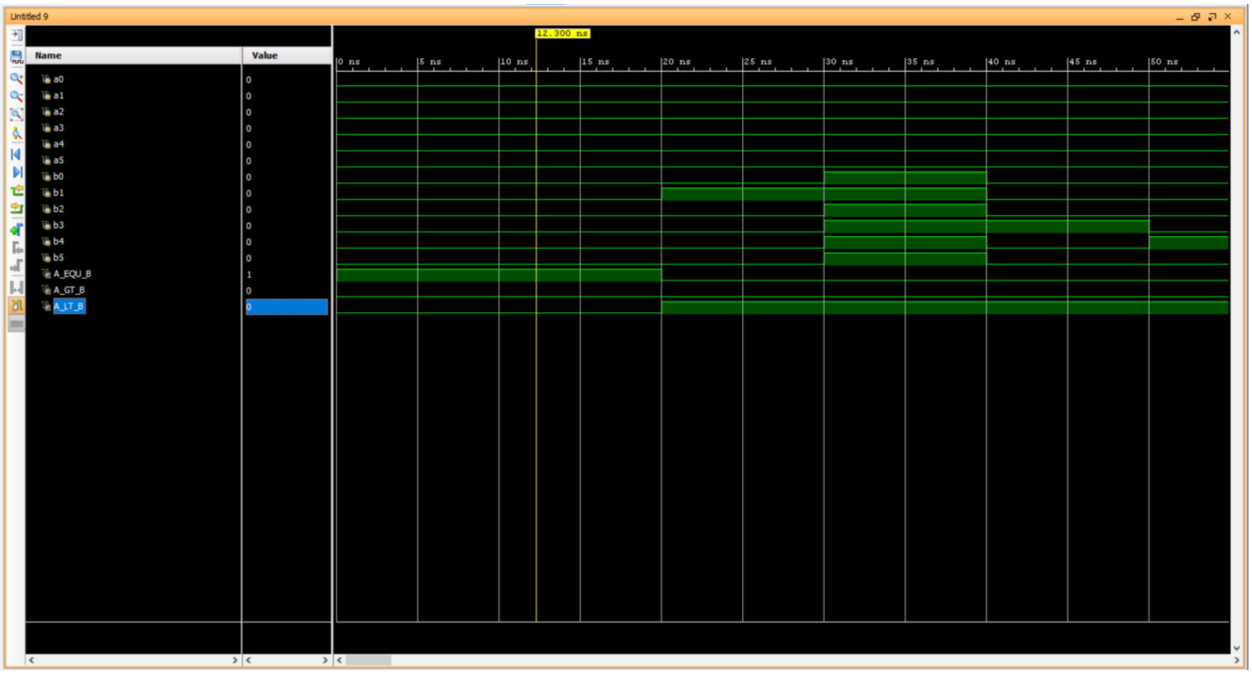
6bit comparator:



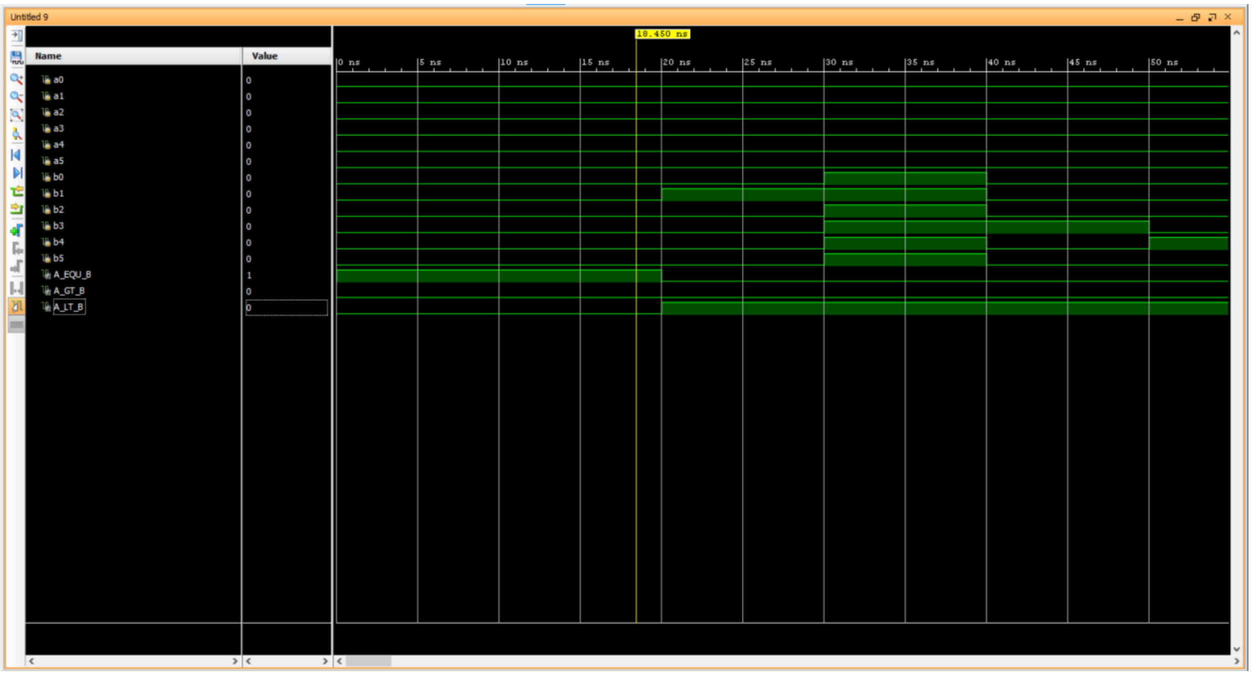
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	0
b4	0
b5	0
A_EQU_B	1
A_GT_B	0
A_LT_B	0



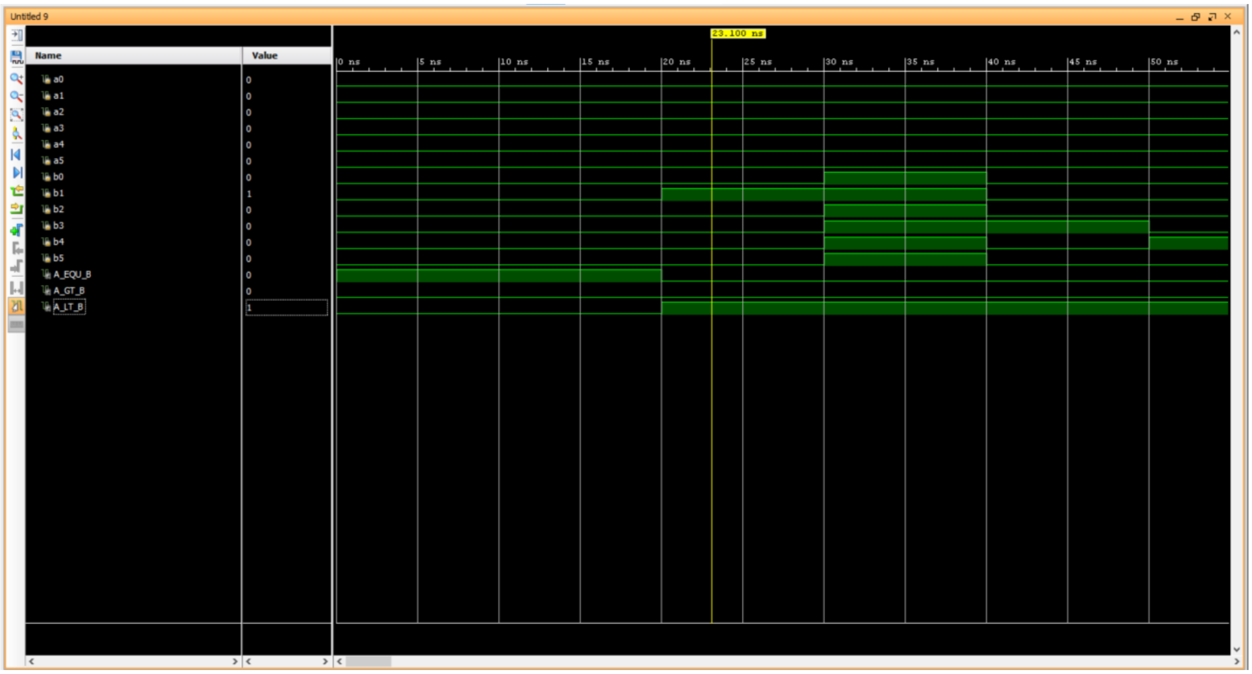
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	0
b4	0
b5	0
A_EQU_B	1
A_GT_B	0
A_LT_B	0



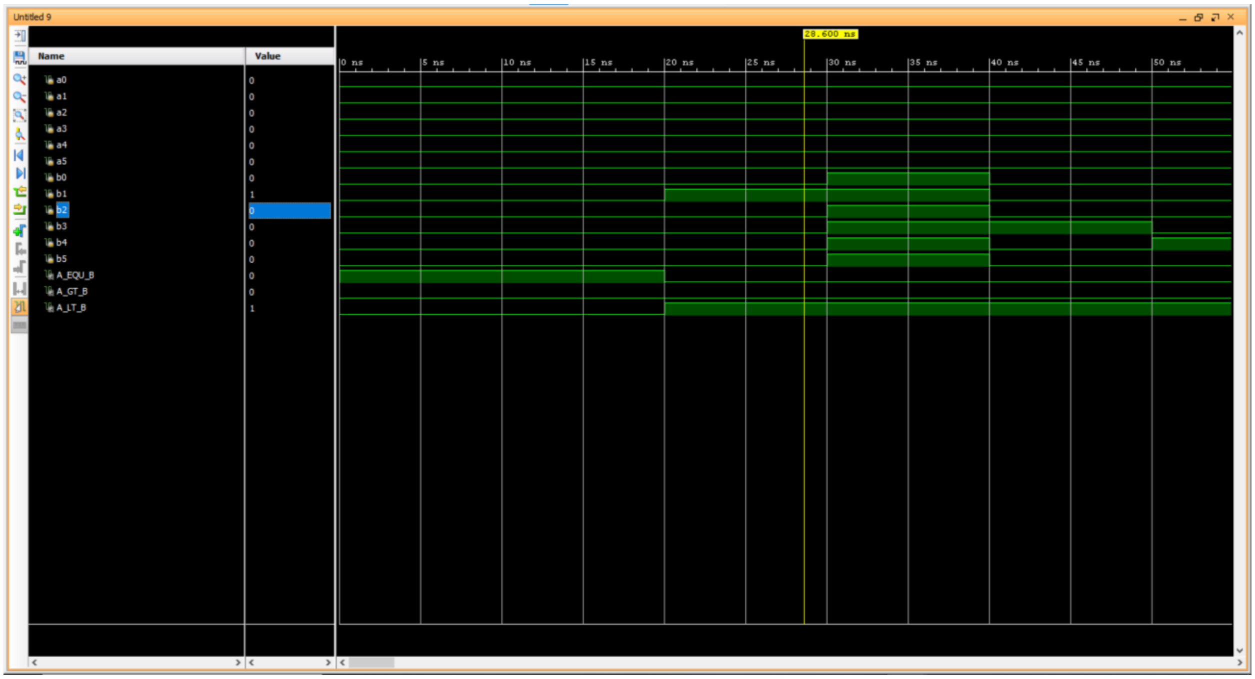
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	0
b4	0
b5	0
A_EQU_B	1
A_GT_B	0
A_LT_B	0



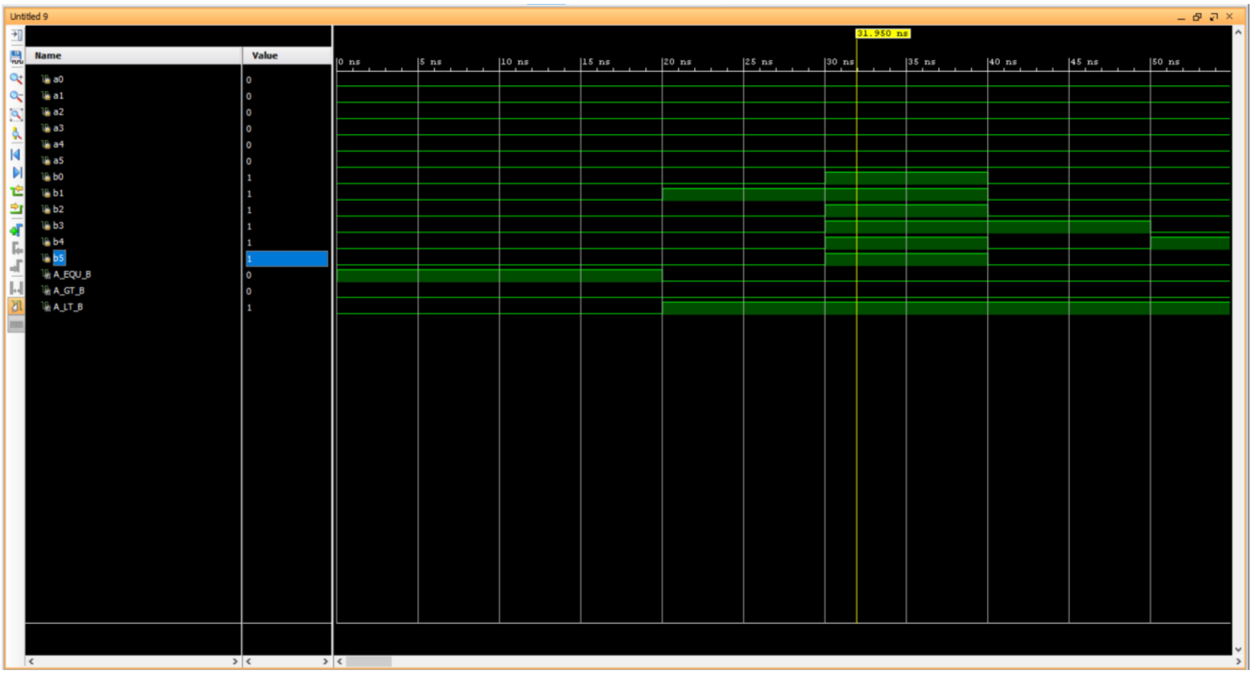
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	0
b4	0
b5	0
A_EQU_B	1
A_GT_B	0
A_LT_B	0



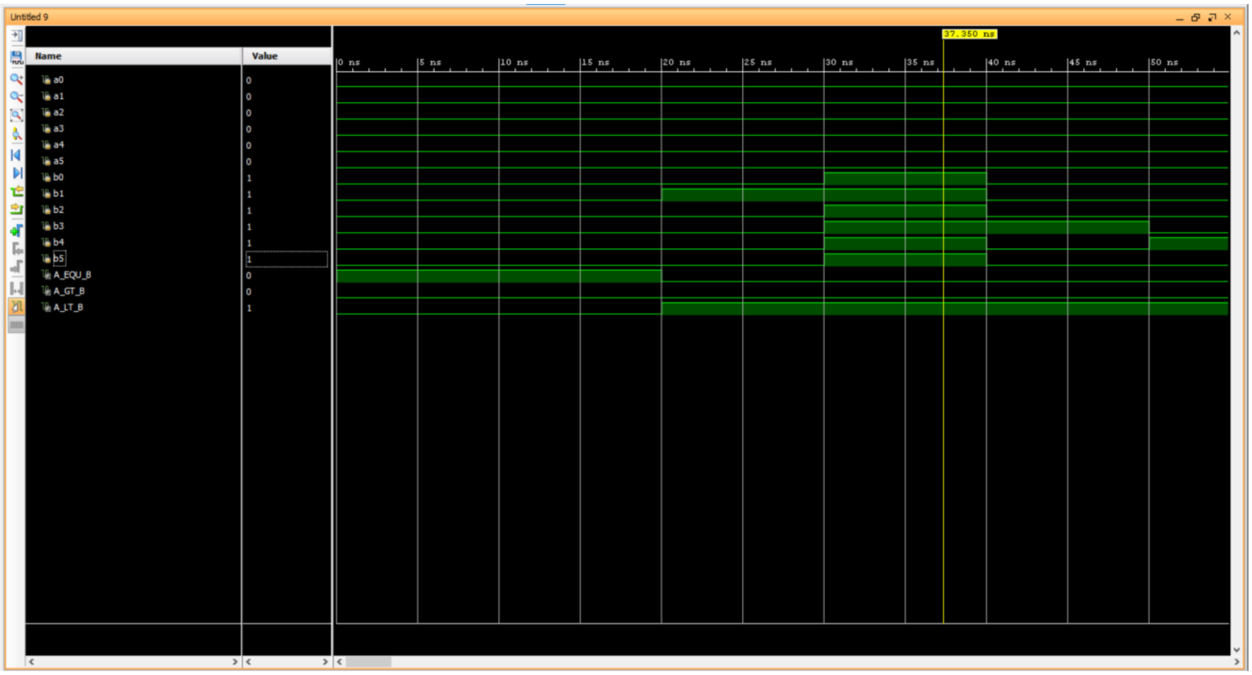
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	1
b2	0
b3	0
b4	0
b5	0
A_EQU_B	0
A_GT_B	0
A_LT_B	1



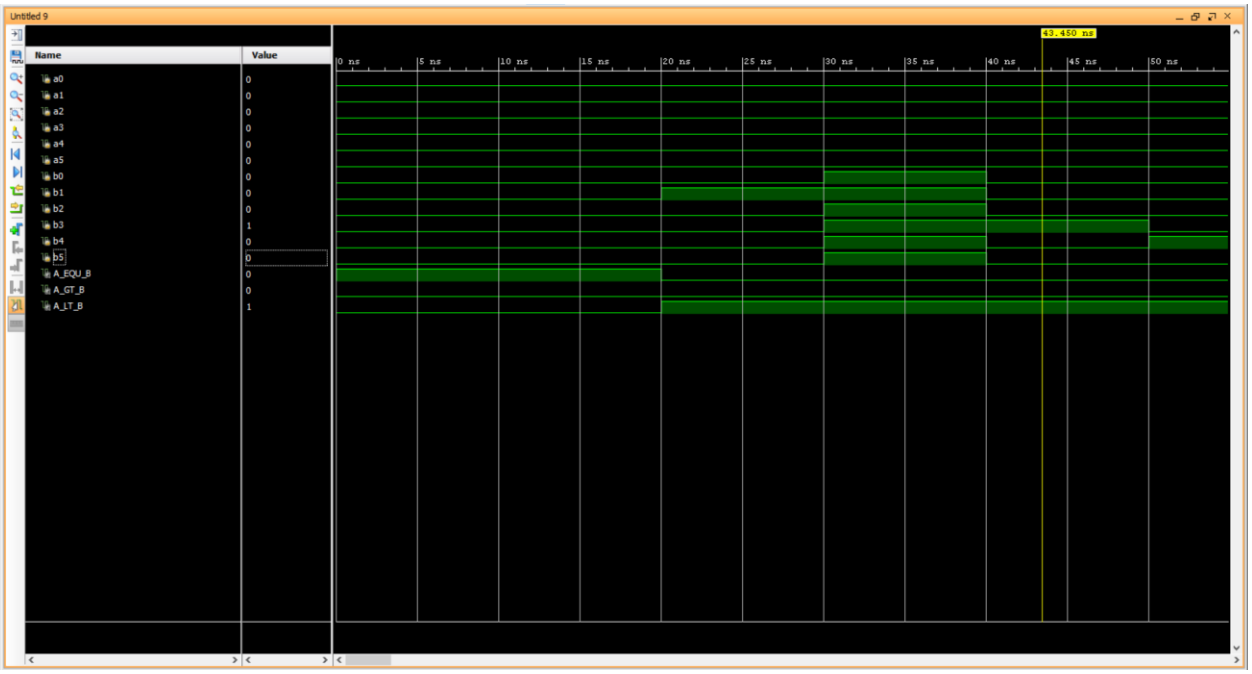
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	1
b2	0
b3	0
b4	0
b5	0
A_EQU_B	0
A_GT_B	0
A_LT_B	1



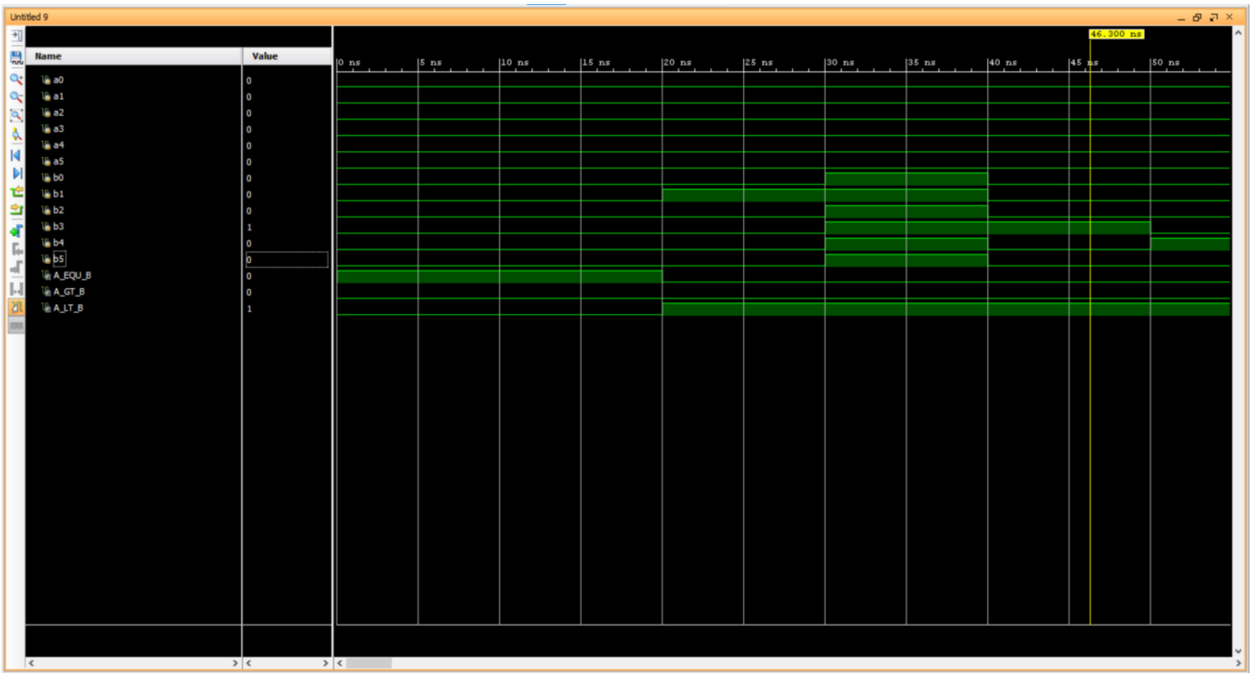
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	1
b1	1
b2	1
b3	1
b4	1
b5	1
A_EQU_B	0
A_GT_B	0
A_LT_B	1



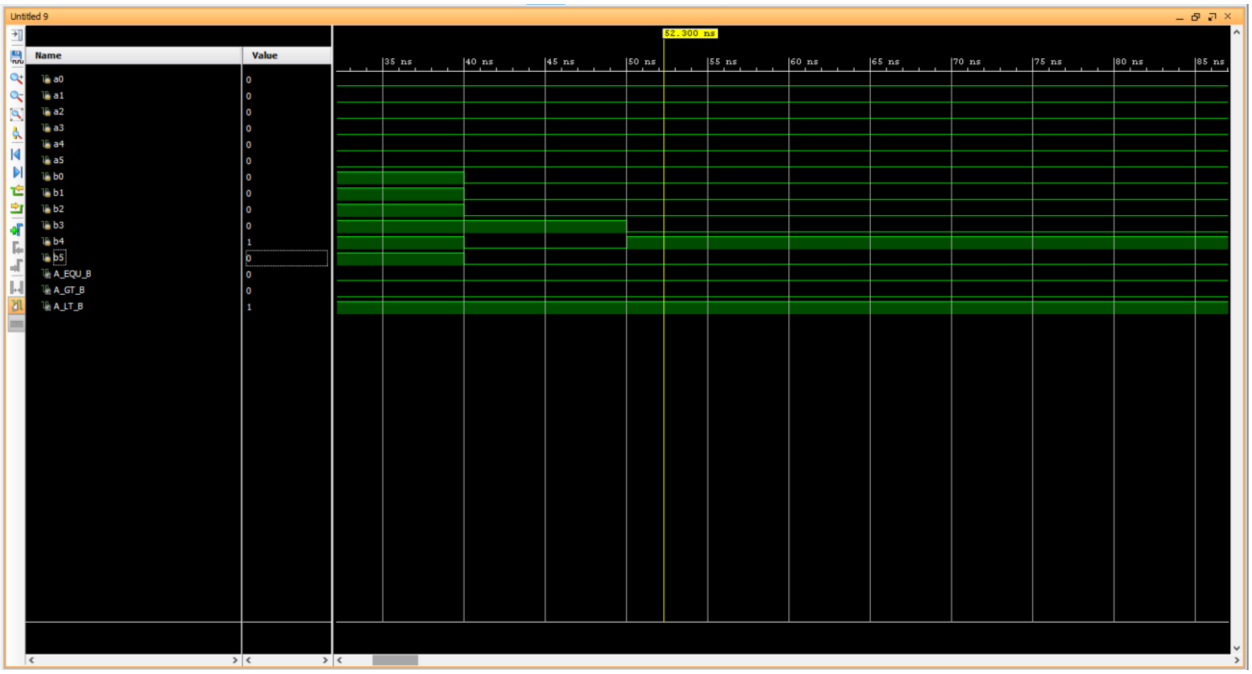
Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	1
b1	1
b2	1
b3	1
b4	1
b5	1
A_EQU_B	0
A_GT_B	0
A_LT_B	1



Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	1
b4	0
b5	0
A_EQU_B	0
A_GT_B	0
A_LT_B	1



Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	1
b4	0
b5	0
A_EQU_B	0
A_GT_B	0
A_LT_B	1



Untitled 9

Name	Value
a0	0
a1	0
a2	0
a3	0
a4	0
a5	0
b0	0
b1	0
b2	0
b3	0
b4	1
b5	0
A_EQU_B	0
A_GT_B	0
A_LT_B	1

Conclusion :

I have got full knowledge about comparators and how to draw it

Now I can draw any type of comparator