DLD LAB WIN 2021

LAB4

Aim: To simulate different types of logic gates DeMUX-1to4 and

MUX-6to1

Tools used: vivado software

Truth tables:

DeMux-1to4:

Data Input	Select	Inputs		Out	puts	
D	Sı	S ₀	Υ ₃	Y ₂	Υ ₁	Y ₀
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

MUX-16to1:

TRUTH TABLE

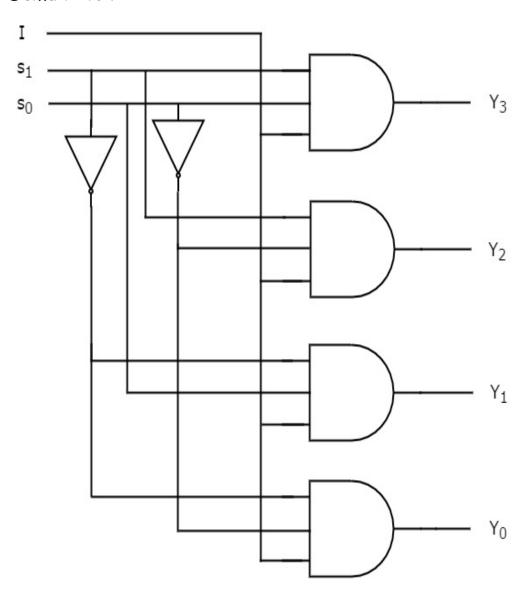
S0	S1	\$2	\$3	Ē	SELECTED CHANNEL
X	Х	Х	Х	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level L= Low Level

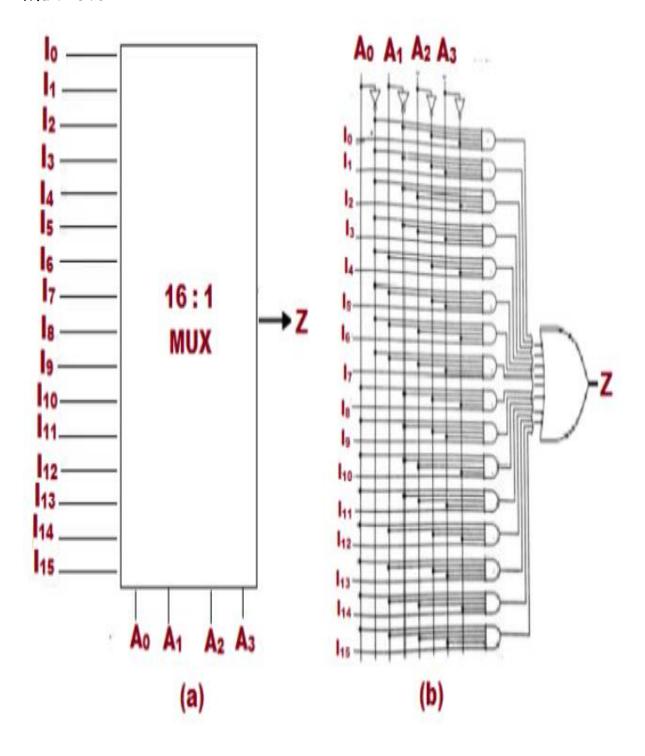
X= Don't Care

Circuit diagrams

Demux-1to4:



Mux 16 to 1:



Codes:

Demux-1to4:

```
19
20
      21
22
      module dem_1_4(i0,i1,i2,i3,s0,s1,z);
      input s0, s1, z;
23
24
      output i0, i1, i2, i3;
25
      and3 f4((~s0),(~s1),z,i0);
26
      and3 f2((~s0),s1,z,i1);
27
      and3 f3(s0,(~s1),z,i2);
28
      and3 fl(s0,s1,z,i3);
29
      endmodule
30
      module and3(a,b,c,z);
      input a,b,c;
31
32
      output z;
      assign z = a & b & c;
33
      endmodule
34
35
36
```

Test bench code demux 4:1:

```
1
2
     module tb_dem_1_4;
3
4
     reg s0, s1, z;
5
     wire i0,i1,i2,i3;
6
7
     dem_1_4 a2(i0,i1,i2,i3,s0,s1,z);
8
     initial
9
     begin
0 0
         z = 1'b1;
1 0
       s0 = 1'b0; s1 = 1'b0;
2  #10 s0 = 1'b0;s1 = 1'b1;
3 () #10 s0 = 1'b1;s1 = 1'b0;
4 O #10 s0 = 1'b1;s1 = 1'b1;
5
     end
16
     endmodule
7
```

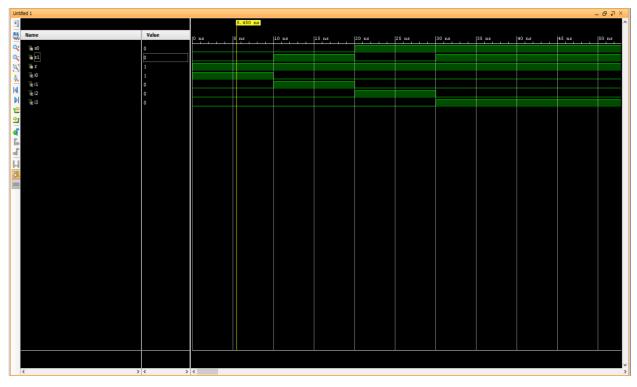
Mux 16:1

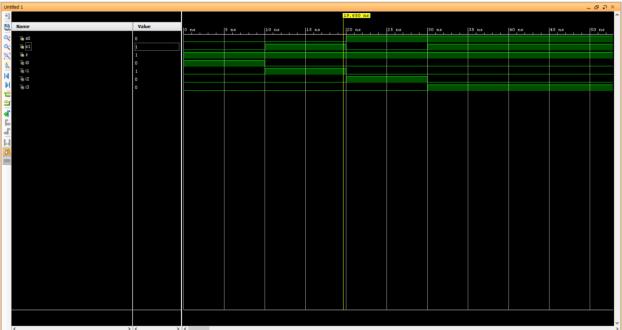
```
22
23
      module mux16 1(i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15,s0,s1,s2,s3,z);
24
     input i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15,s0,s1,s2,s3;
25
      output reg z;
26 O always@(i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15,s0,s1,s2,s3)
      begin
28 O if (s0 == 1'b0 && s1 == 1'b0 && s2 == 1'b0 && s3 == 1'b0)
29 🔾
        z = i0;
30 O else if(s0 == 1'b0 && s1 == 1'b0 && s2 == 1'b0 && s3 == 1'b1)
31 0
         z = i1:
32 O else if(s0 == 1'b0 && s1 == 1'b0 && s2 == 1'b1 && s3 == 1'b0)
33 0
       z = i2;
34 O else if(s0 == 1'b0 && s1 == 1'b0 && s2 == 1'b1 && s3 == 1'b1)
35 0
       z = i3;
36 O else if(s0 == 1'b0 && s1 == 1'b1 && s2 == 1'b0 && s3 == 1'b0)
37 🔾
        z = i4;
38 O else if(s0 == 1'b0 && s1 == 1'b1 && s2 == 1'b0 && s3 == 1'b1)
        z = 15;
39 0
40 O else if(s0 == 1'b0 && s1 == 1'b1 && s2 == 1'b1 && s3 == 1'b0)
11 O
         z = 16;
42 O else if (s0 == 1'b0 && s1 == 1'b1 && s2 == 1'b1 && s3 == 1'b1)
43 O
        z = i7;
44 O else if(s0 == 1'bl && s1 == 1'b0 && s2 == 1'b0 && s3 == 1'b0)
45 O
        z = 18;
46 ○ else if(s0 == 1'bl && s1 == 1'b0 && s2 == 1'b0 && s3 == 1'b1)
17 O
       z = 19;
48 O else if(s0 == 1'bl && s1 == 1'b0 && s2 == 1'bl && s3 == 1'b0)
49 O
       z = i0;
50 O else if(s0 == 1'bl && s1 == 1'b0 && s2 == 1'bl && s3 == 1'bl)
51 0
        z = i11;
52 O else if(s0 == 1'bl && s1 == 1'bl && s2 == 1'b0 && s3 == 1'b0)
53 0
       z = i12;
54 O else if(s0 == 1'bl && s1 == 1'bl && s2 == 1'b0 && s3 == 1'bl)
         z = i13;
56 O else if(s0 == 1'bl && s1 == 1'bl && s2 == 1'bl && s3 == 1'b0)
57 O
         z = i14;
58
      else
59 🔾
       z = i15;
50
      end
51
      endmodule
52
```

Testbench code mux 16:1

```
module tb mux16 1;
reg i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15,s0,s1,s2,s3;
wire z;
mux16 1 x3(i0,i1,i2,i3,i4,i5,i6,i7,i8,i9,i10,i11,i12,i13,i14,i15,s0,s1,s2,s3,z);
initial
begin
    i0 = 1'b0; i1 = 1'b1; i2 = 1'b0; i3 = 1'b1;
    i4 = 1'b0; i5 = 1'b1; i6 = 1'b0; i7 = 1'b1;
    i8 = 1'b0; i9 = 1'b1; i10 = 1'b0; i11 = 1'b1;
    il2 = 1'b0;il3 = 1'b1;il4 = 1'b0;il5 = 1'b1;
    s0 = 1'b0; s1 = 1'b0; s2 = 1'b0; s3 = 1'b0;
#10 s0 = 1'b0;s1 = 1'b0;s2 = 1'b0;s3 = 1'b1;
#10 s0 = 1'b0;s1 = 1'b0;s2 = 1'b1;s3 = 1'b0;
#10 s0 = 1'b0;s1 = 1'b0;s2 = 1'b1;s3 = 1'b1;
#10 s0 = 1'b0;s1 = 1'b1;s2 = 1'b0;s3 = 1'b0;
#10 s0 = 1'b0;s1 = 1'b1;s2 = 1'b0;s3 = 1'b1;
#10 s0 = 1'b0;s1 = 1'b1;s2 = 1'b1;s3 = 1'b0;
#10 s0 = 1'b0;s1 = 1'b1;s2 = 1'b1;s3 = 1'b1;
#10 s0 = 1'b1;s1 = 1'b0;s2 = 1'b0;s3 = 1'b0;
#10 s0 = 1'bl;s1 = 1'b0;s2 = 1'b0;s3 = 1'bl;
#10 s0 = 1'bl;s1 = 1'b0;s2 = 1'b1;s3 = 1'b0;
#10 s0 = 1'b1;s1 = 1'b0;s2 = 1'b1;s3 = 1'b1;
#10 s0 = 1'bl;s1 = 1'bl;s2 = 1'b0;s3 = 1'b0;
#10 s0 = 1'bl;s1 = 1'bl;s2 = 1'b0;s3 = 1'bl;
#10 s0 = 1'bl;s1 = 1'bl;s2 = 1'bl;s3 = 1'b0;
#10 s0 = 1'bl;s1 = 1'bl;s2 = 1'bl;s3 = 1'bl;
end
endmodule
```

Output Demux 4to1:

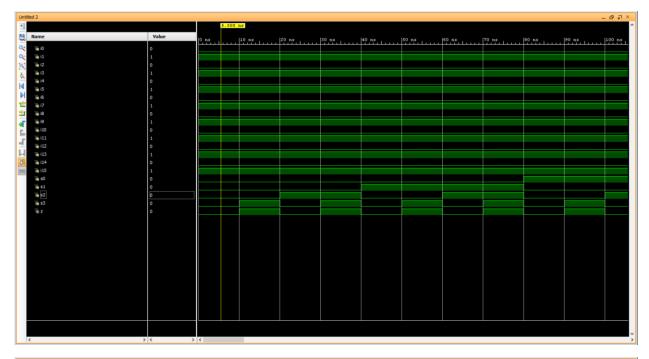


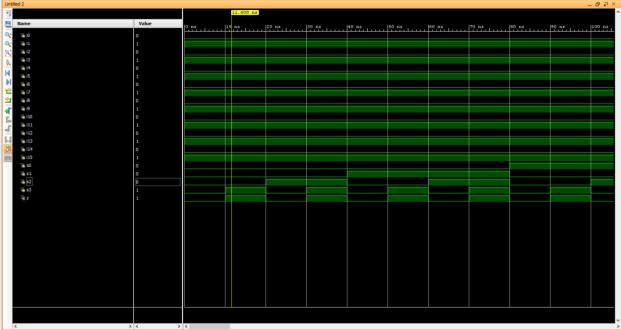


ed 1												_ 8 2
							28	.450 ns				
Name	Value	0 ns	5 ns	10 ns	15 ns	20 ns	25 ns	30 ns	35 ns	40 ns	45 ns	50 ns
₩ s0	1											
16 p1	0											_
₩ _a io	ů		_									
T& 11	0											
Th 12	1											
1 <u>€</u> i3	0											
	> < >	<										

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									34.950 ns			
Name	Value	0 ns	5 ns	10 ns	15 ns	20 ns	25 ns	30 ns	35 ns	40 ns	45 ns	50 ns
16 s0 16 51	1											
₩ Z	1											-
·	0											
14±10 14±11 14±12	0											
Ten 12 Ten 13	0											
@ I3	ľ											
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Mux 16:1 outputs:





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1						26.400	0 ns							
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2		0												ļ
\	1 <u>a</u> i1	1												
`	1 <u>6</u> i2	0												
	16 13	0												
1	1 <u>6</u> i4 1 <u>6</u> i5													
N	19 16	0												
÷	16.17	1												
ď	1 <u>a</u> i8	0												
r	16 19	1												
G.	TE 110	0												
ř	1 <u>6</u> i11	1												
	1 <u>6</u> 112	0												
H	19 i13 19 i14	0												
J &	16 (15	1												
7	16 s0	0												_
	\ <u>a_</u> s1	0												
	15 s2	1												
	1 <u>6</u> s3	0												
	Tén z	0												
		< >	<											

ed 2												_ 6 7
					32.600 ns							
Name	Value	0 ns	10 ns	20 ns	30 xs	40 ns	50 ns	60 ns	70 ns	80 ns	90 ns	100 ns
1 <u>%</u> i0 1 <u>%</u> i1												
15 i2	0											
1 <u>6</u> i3												
1 <u>6</u> 14												
1 <u>%</u> i5 1 <u>%</u> i6												
16 17												
15 i8												
1 <u>6</u> i9 1 <u>6</u> i10												
16 i11												
16. i12												
l <u>a</u> i13												
16. i14 16. i15	0											-
1 <u>h</u> s0	0											+
1 <u>6</u> s1												
16 s2 16 s3												
16 2 16 2					_							
												—
	< >	<										

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Name	Value	0 ns	10 ns .	20 ns .	30 ns .	40 ns	. 1	50 ns .	60 ns .	70 ns	80 ns	90 ns .	100 ns
l , 16 i0	0					77,775							1000
<u> 16 i1</u>	1												1
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0												
16 13	1												
16 14 16 15	0												-
18 16	1												
16 17	1												_
1 14 is	ō												
18 19	1												
™ i10	0												
r 14 111	1												
19 i12 19 i13	0												-
1 14 114	1												
15 i15	1												_
1 <u>8</u> s0	0												_
18 s1	1												
16 s2	0]											
1 <u>6</u> s3	0												
₹ Z	0												
<	> <	> <											
15	, (

d 2							5	4.800 r	ns.				_ 윤
Name	Value	10		100	100					B0	100	100	
1 <u>6</u> i0	o	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns		60 ns	70 hs	80 ns	90 ns	100 2
1 <u>6</u> 11	1												
10 12	i.												
1 13	1												
18-14	0												
16 15	1												
l <u>a</u> i6	0												_
12- 17	1												
16 is	0												
16 i9 16 i10	0												
16 i11	ľ												
W 112	ō												
1 i13	1												
Via 114	0												
16 115	1												
1 <u>6</u> s0	0												
16 S1	1	,											
16 s2 16 s3	P	J											-
₩ z	1;						_						-
	1.												

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									72.800 ns			
Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 rs	80 ns	90 ns	100 ns
14 10	0									1		1
16.11	1											
16 t2 18 t3	0											4
1 <u>a</u> 13 1 <u>a</u> 14	10											
18 15	1											+
16 16	0											
14 17	1											1
1 <u>6</u> i8	0											
14 19	1											
16 i10 16 i11	°.											
1 11 12 112	i o											
16 113	1											
16 114	0											
10-115	1											
1≜ s0	0											
₩ s1	1											
16 g2 16 s3	1								_			
¹₩ z	1											
<	> < >	<										

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)]										83.40) ns	
Name	Value	0 ns	10 ns .	20 ns .	30 ns ,	40 ns .	50 ns .	60 ns	70 ns .	80 ns .	90 ns .	100 ns
<u> 1≟ i0</u>	0											
1€ 11	1											
18 12	0											
16 13	1											
18 i3 18 i4 16 i5	0											
12 16	0											
<u>←</u> 1 <u>‰</u> i7	1											
<u>2r</u> 1 <u>6</u> i8	0											
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1											
- 110 - 20 444	0											
% i11 % i12	0											
- 18 i13	1											_
1 18 114	0											
l <u>a</u> i15	1											
<u>1</u> ≤0	1											
V6 s1	0											
16 52 16 53	0											
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Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 ns	80 ns	90 ns	100 ns
V <u>a</u> 10	0											
12.11	1											
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1 <u>6</u> 14	i i											
18 15	1											
16	0											
1 <u>6</u> i7	1											
1 <u>6</u> 18	0											
16 19	1											
1 <u>a</u> i10	0											
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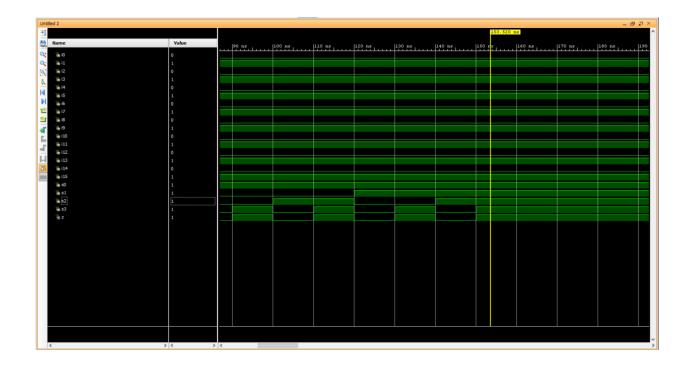
d 2												_ ១ :
				1	03.500 n							
Name	Value	 80 ns	90 ns	100 rs	1	110 ns	120 ns	130 ns	140 ns	150 ns	160 ns	170 ns
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16 14	0											
18 15	1											
14 16	0											
14 17	1											
1 <u>6</u> i8 1 <u>6</u> i9	0											-
16 i10	0											
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ÞI	16 15 16 16	0												
ė	14.17	1												
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er er	V _a i9	1												
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iii 	1 <u>a</u> i12	0												
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							124.110	ns				
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	0											
19 19 12	0											
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16.13	1											
19-14 19-15	0											
14 16	0											
18 17	1											
1 <u>6</u> i8	0											
16 19	1											
18 110	0											
16 111	1											
19 i12 19 i13	0											
15 114	0											
I i15	1											
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1 s1	1											
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15	1												
16	0												
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19	l,												
110	o												
111	1												
112	0												
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115	1												
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s2 s3	1	-											
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Conclusion:

Now I got full knowledge about the mutliplexer and demultiplexer