DLD

EXPERIMENT – 7

Aim: To simulate the logic gates of JK flipflop and D flipflop

Tools used: vivado software

Truth tables:

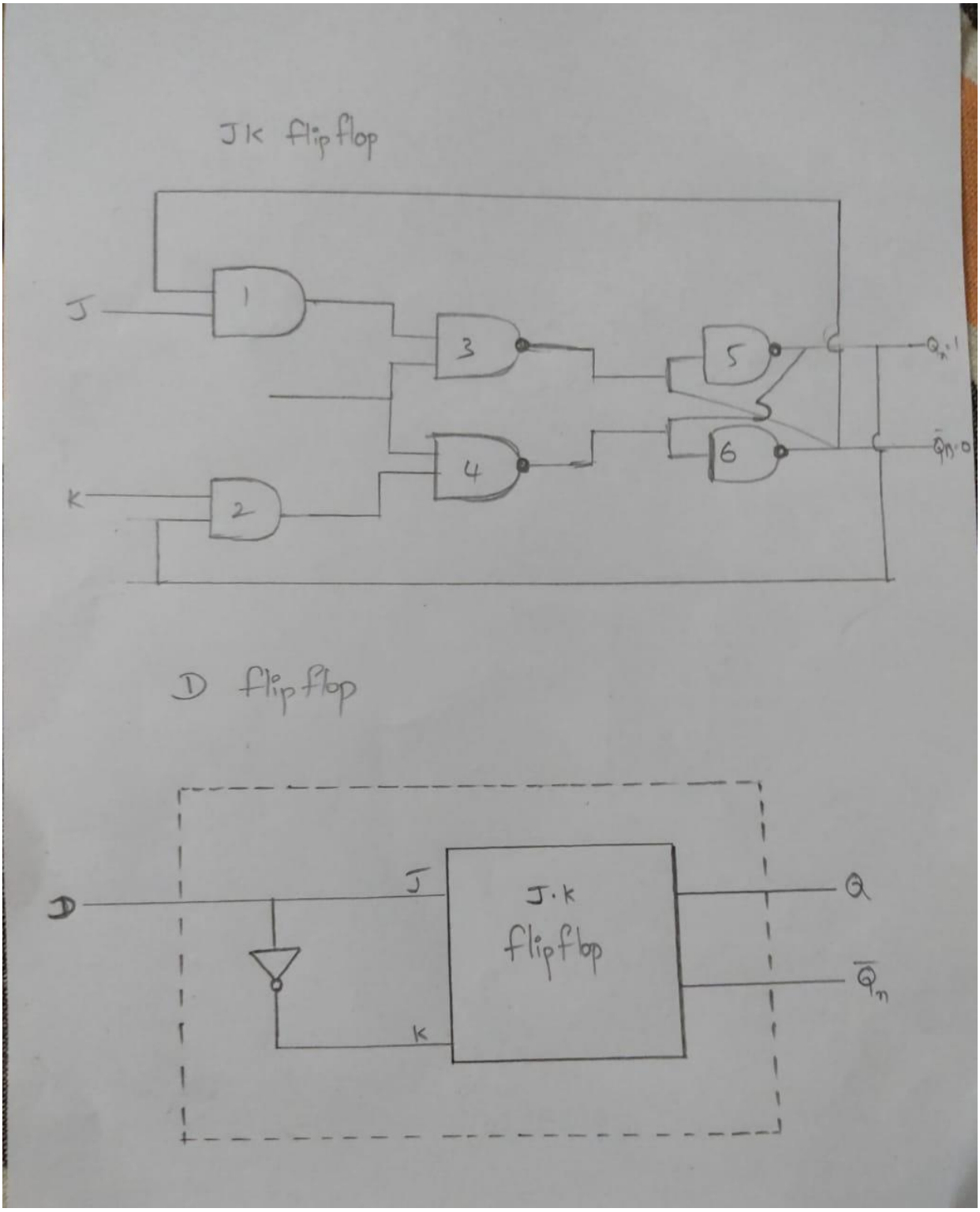
Jk flipflop:

Truth table for jk flipflop			
clk	j	k	Qn+1
0	x	x	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Qn

D flipflop:

Truth table for D flipflop			
clk	D	q	Qbar
0	0	Q	Qbar
0	1	Q	Qbar
1	0	0	1
1	1	1	0

Diagrams of JK flipflop and D flipflop:



Verilog codes:

JK flipflop:

```
23 module jk_ff(j,k,clk,q,qbar);
24 input j,k,clk;
25 output q,qbar;
26
27 reg qn,q,qbar;
28
29 initial
30 begin
31 q=0;
32 qbar=1;
33 end
34
35 always@(posedge clk)
36 begin
37 if(j==0 && k == 0)
38    qn = q;
39 else if(j == 0 && k == 1)
40      qn = 0;
41 else if(j == 1 && k == 0)
42       qn = 1;
43 else
44        qn = ~q;
45 q = qn;
46 qbar = ~qn;
47 end
48 endmodule
```

Test bench code:

```
23 module tb_jk_ff;
24 reg j,k,clk;
25 wire q,qbar;
26
27 jk_ff a1(j,k,clk,q,qbar);
28
29 initial
30 begin
31 j=0;k=0;clk=0;
32 end
33
34 always
35 begin
36 #10 clk = ~clk;
37 #20 j = 0;k = 1;
38 #20 j = 1;k = 1;
39 #20 j = 1;k = 1;
40 #20 j = 0;k = 0;
41 end
42 endmodule
```

D flipflop:

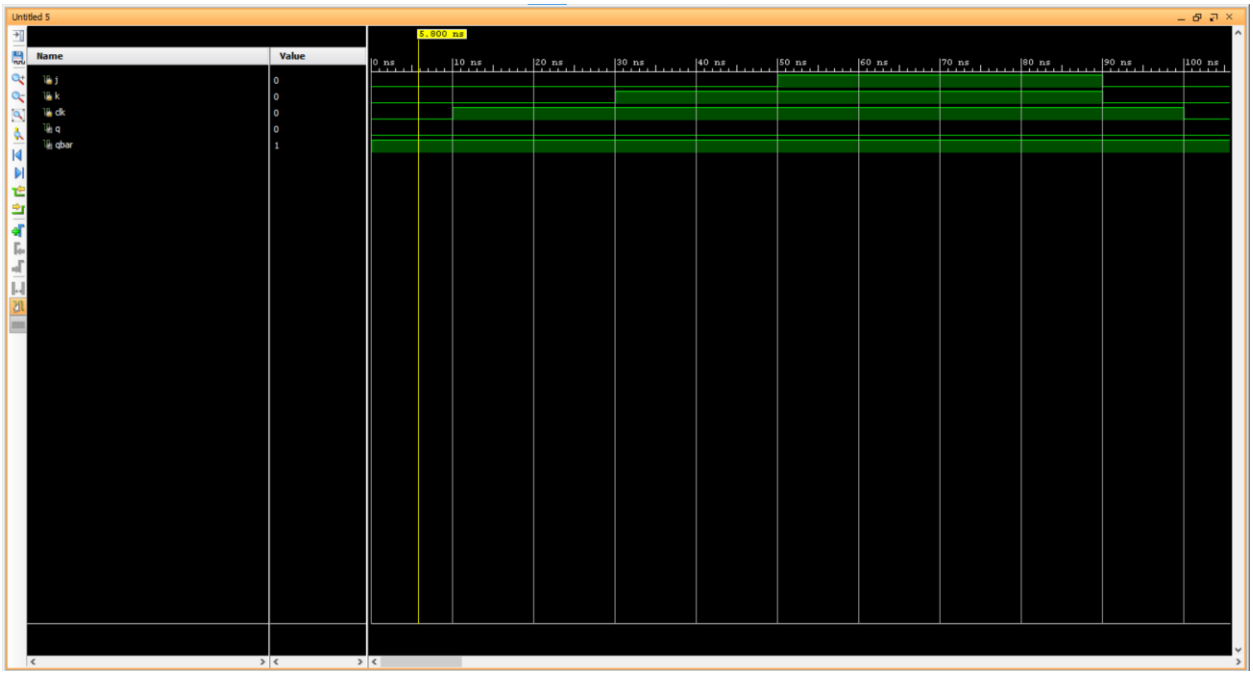
```
23 module d_ff(clk,rst,d,q,qbar);
24 input clk,rst,d;
25 output q,qbar;
26 reg q,qbar;
27 initial
28 begin
29 q = 1'b0;qbar = 1'b1;
30 end
31 always @ (posedge clk or posedge rst)
32 begin
33     if (rst == 1)
34         q <= 1'd0;
35     else
36         q <= d;
37 assign qbar = !q;
38 end
39 endmodule
```

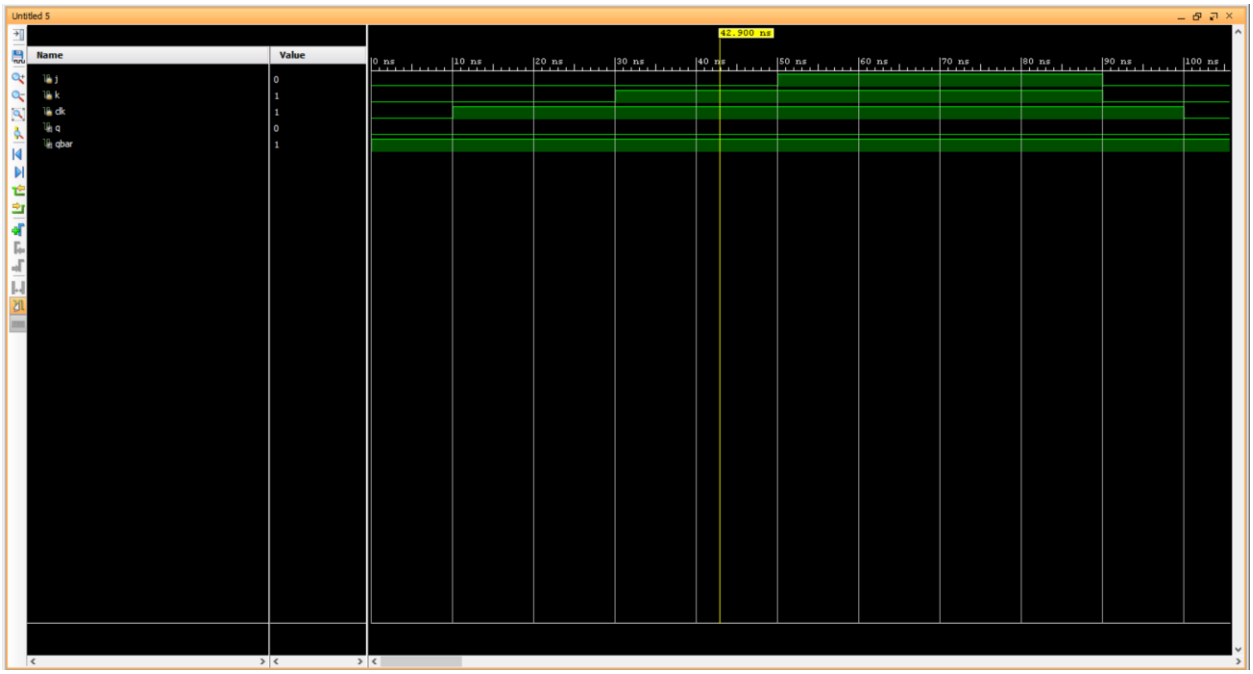
Test bench code:

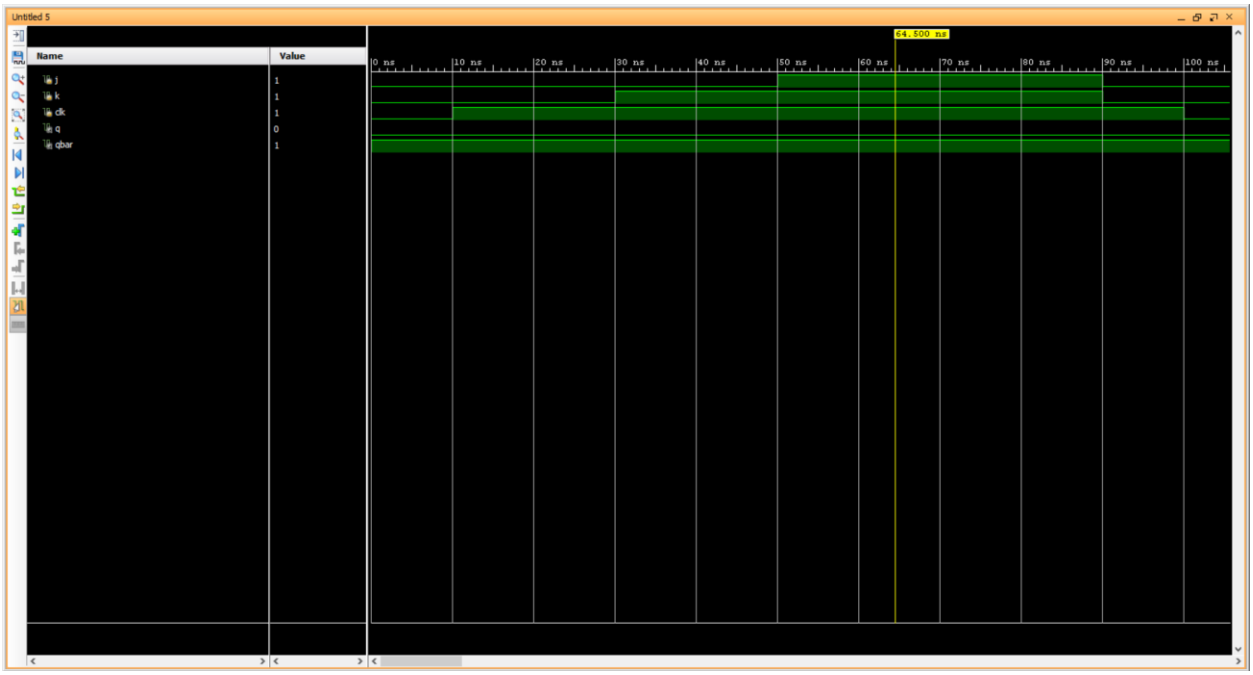
```
23 module tb_d_ff;
24 reg clk,rst,d;
25 wire q,qbar;
26 d_ff d1(clk,rst,d,q,qbar);
27 initial
28 begin
29 clk = 0;rst = 0;d = 0;
30 #20 rst = 0; d = 1;
31 #20 rst = 1; d = 0;
32 #20 rst = 0; d = 0;
33 #20 rst = 1; d = 1;
34 end
35 always
36 begin
37 #5 clk = !clk;
38 end
39 endmodule
```

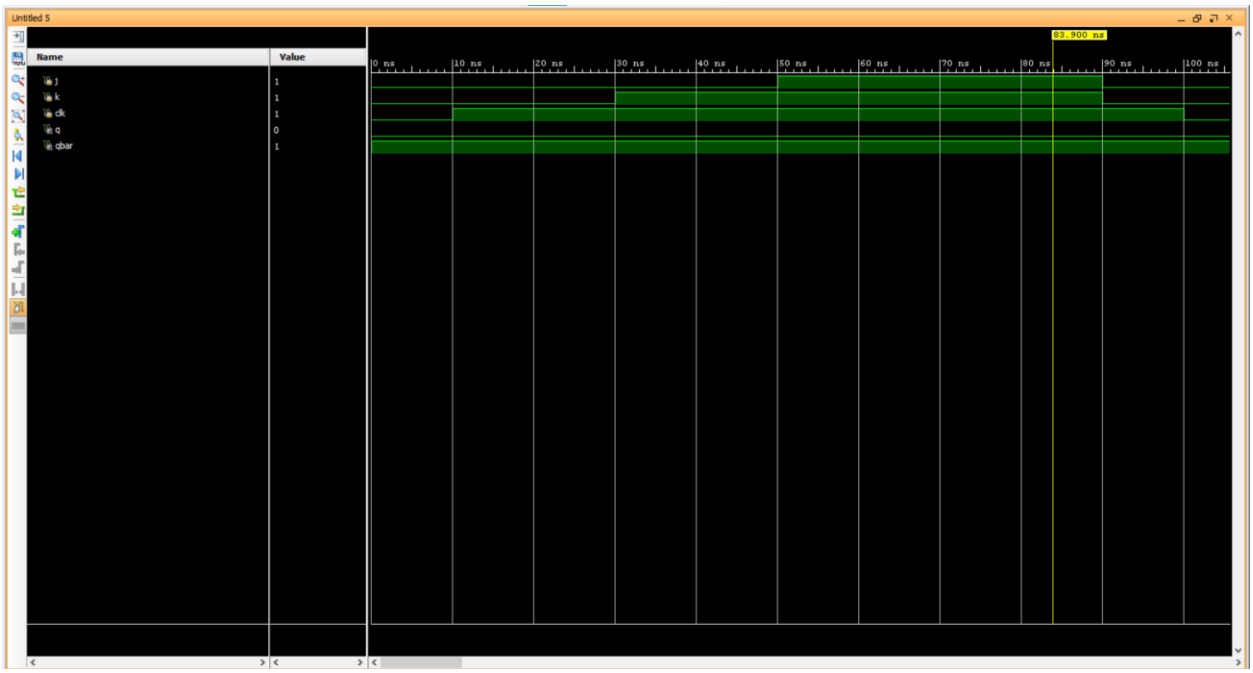
Outputs:

JK flipflop:




Untitled 5
Name
Value
j
k
clk
q
qbar
0
1
1
0
1
42.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns

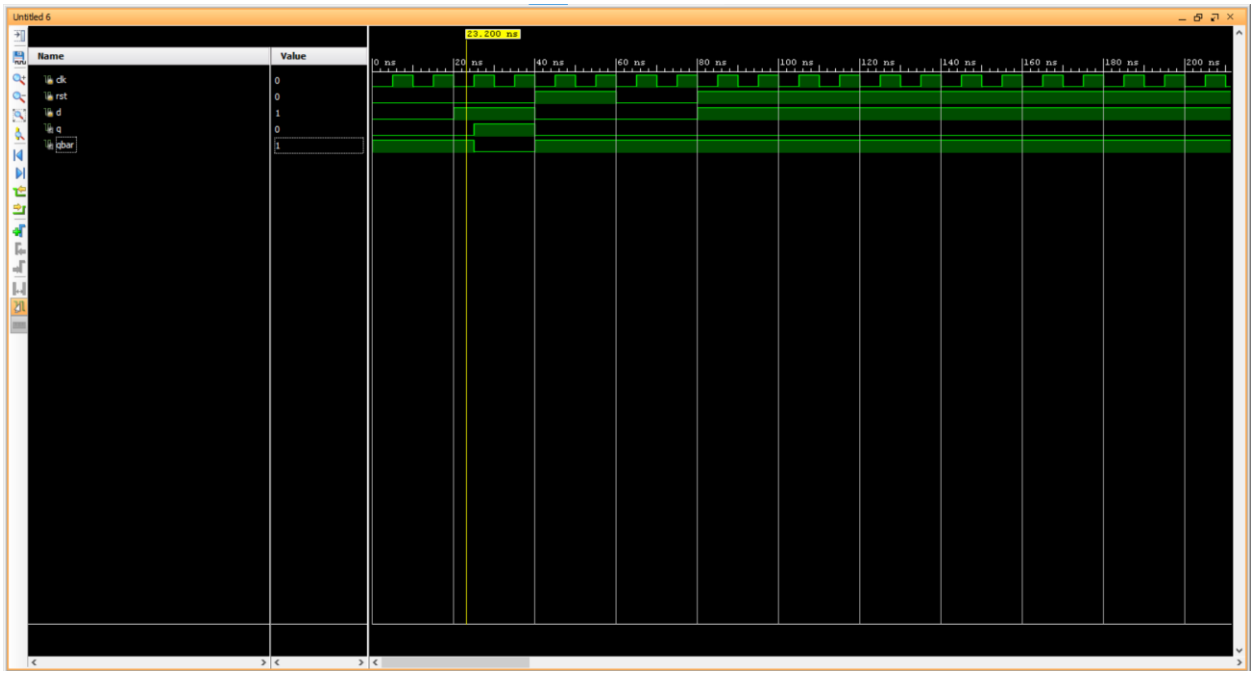

Untitled 5
Name
Value
j
k
clk
q
qbar
1
1
1
0
1
64.500 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns

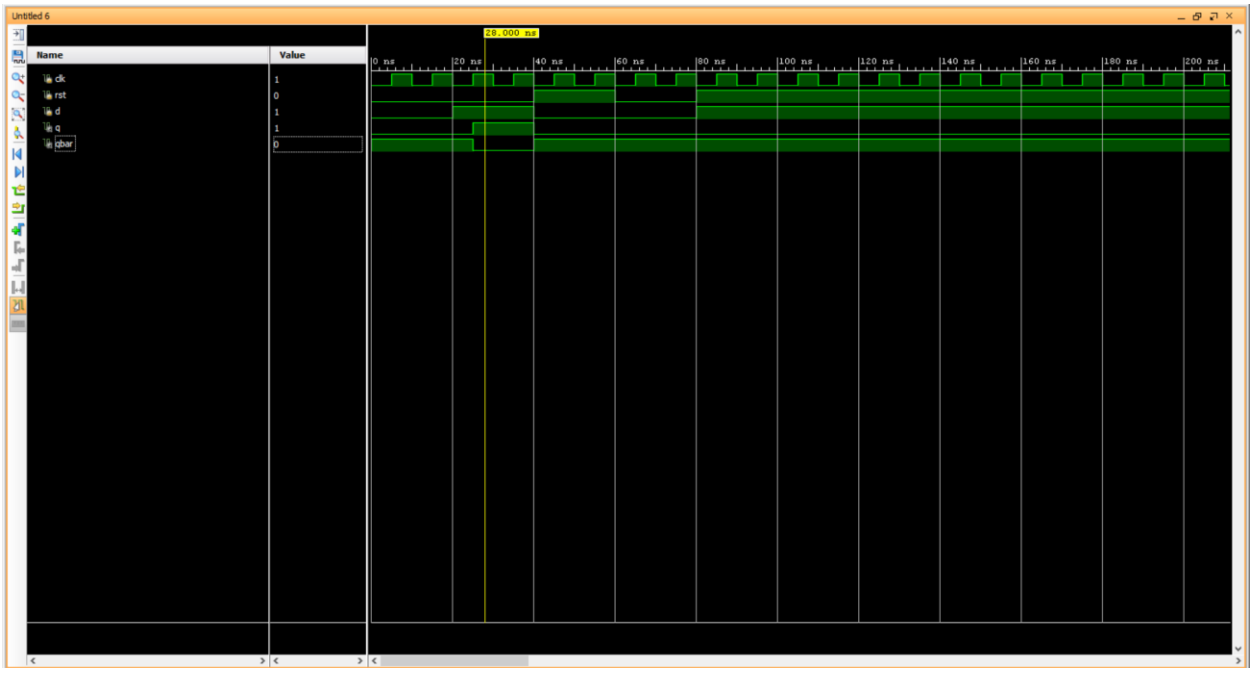

Untitled 5
Name
Value
j
k
clk
q
qbar
1
1
1
0
1
83.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns

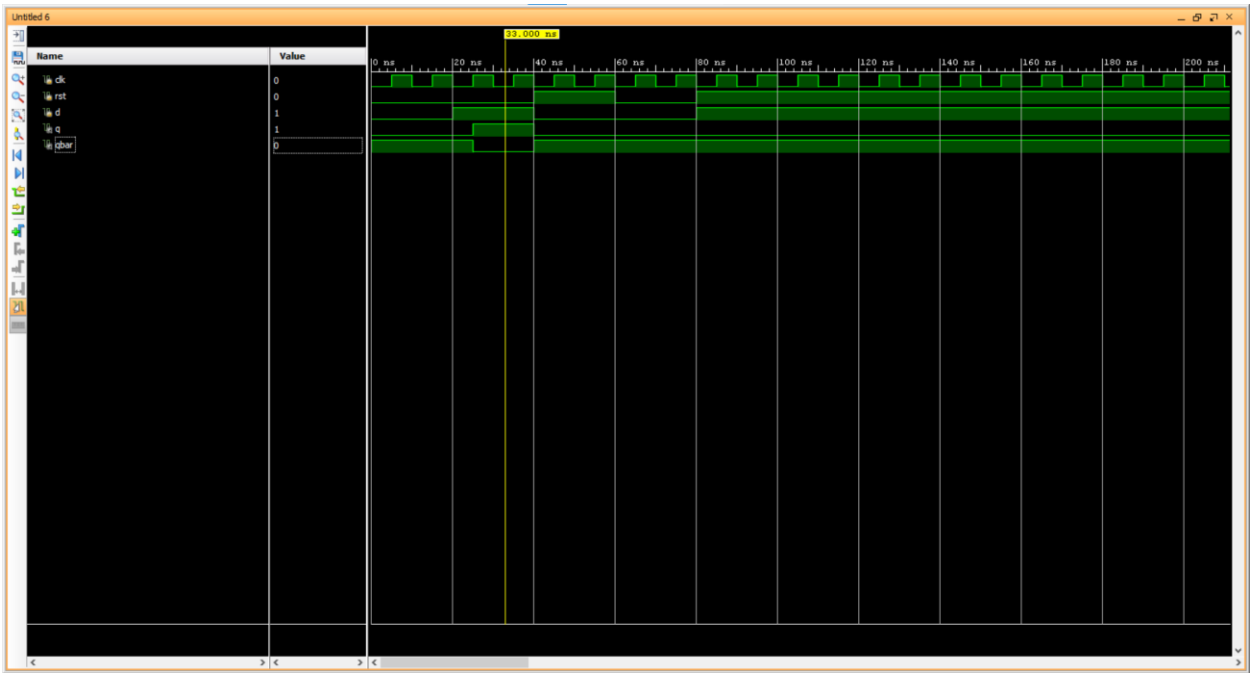
D flipflop:

Untitled 6
Name
Value
clk
rst
d
q
qbar
0
0
0
0
1
12.600 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Name
Value
clk
rst
d
q
qbar
1
0
0
0
1
5.800 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns


Untitled 6
Name
Value
clk
rst
d
q
qbar
0
0
1
0
1
23.200 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

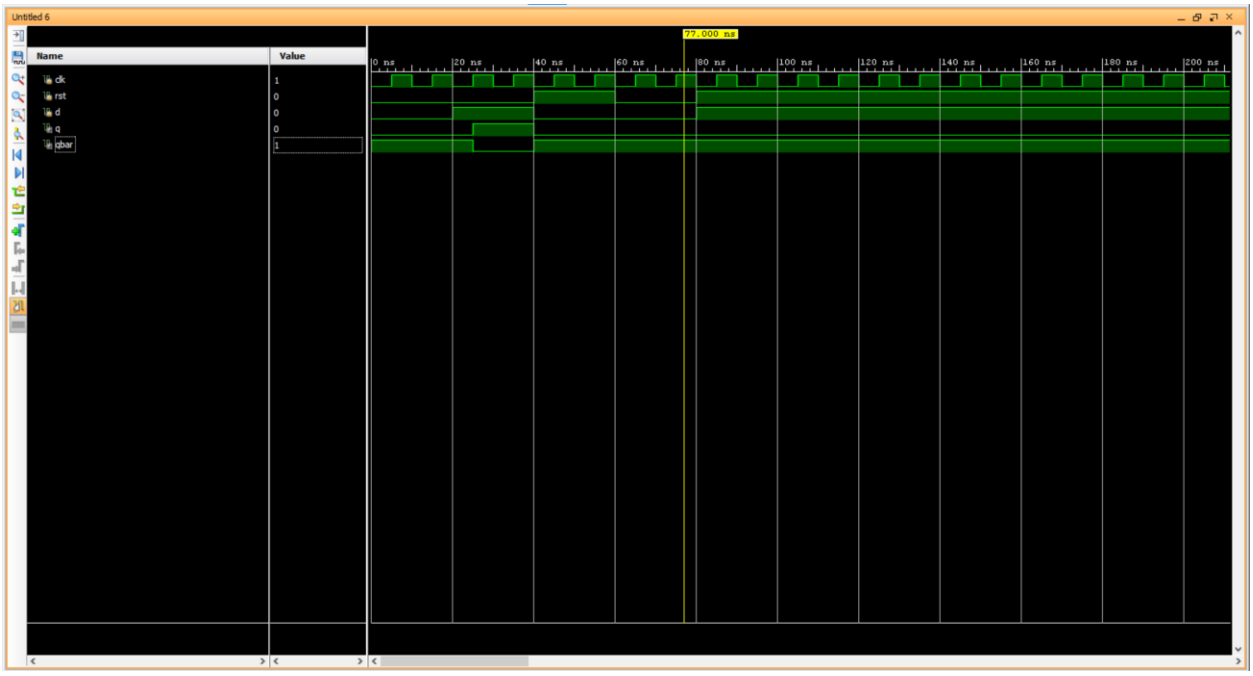

Untitled 6
Name
Value
clk
rst
d
q
qbar
1
0
1
1
0
28.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

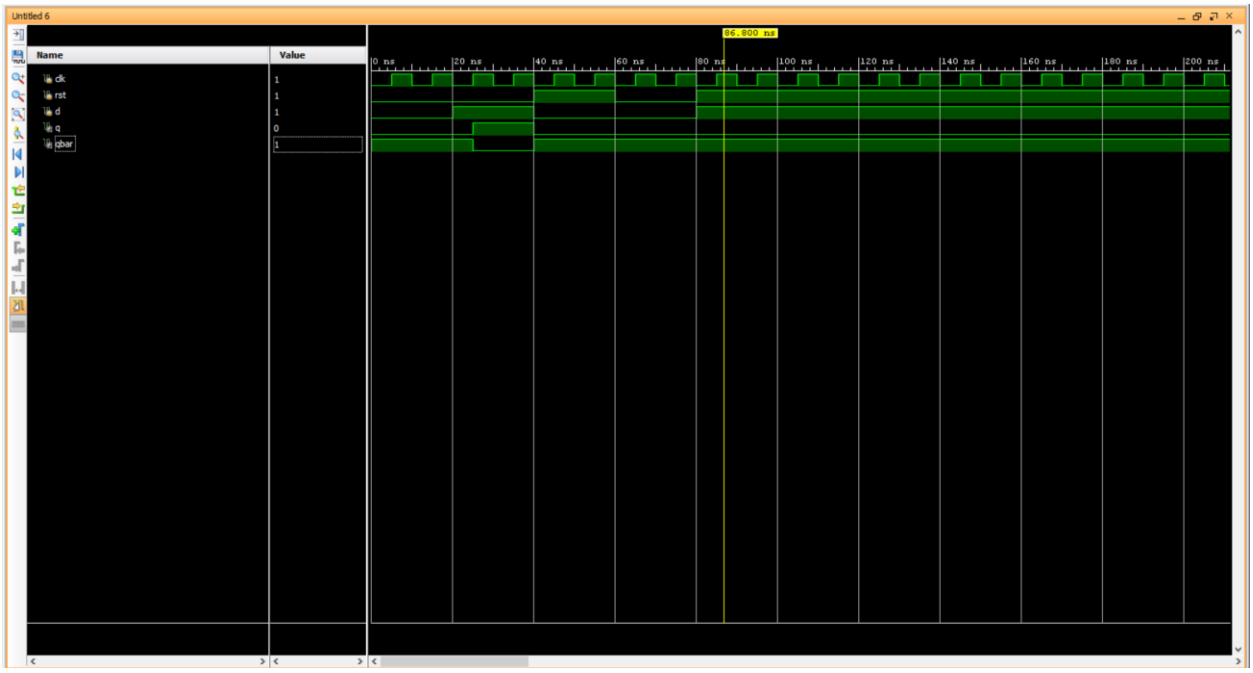

Untitled 6
Name
Value
clk
rst
d
q
qbar
0
0
1
1
0
33.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Untitled 6
Name
Value
clk
rst
d
q
qbar
0
1
0
0
1
44.200 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Untitled 6
Name
Value
clk
rst
d
q
qbar
1
1
0
0
1
40.200 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Untitled 6
64.200 ns
Name
Value
clk
rst
d
q
qbar
0
0
0
0
1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns


Untitled 6
77.000 ns
Name
Value
clk
rst
d
q
qbar
1
0
0
0
1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns


Untitled 6
Name
Value
clk
rst
d
q
qbar
1
1
1
0
1
86.800 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Untitled 6
Name
Value
clk
rst
d
q
qbar
0
1
1
0
1
94.200 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

Conclusion: in this I got knowledge in different types of flipflops in that SR flipflop and JK flipflop and D flipflop I learnt