H.T.No. | | | | | | | | | | |

Code No: CT3518 **SRGEC-R20**

II B.Tech II Semester Supplementary Examinations, January 2023

COMPUTER ORGANIZATION

(Computer Science and Engineering, Artificial Intelligence and Data Science & Information Technology)

Time: 3 Hours **Max. Marks: 70**

Note: Answer one question from each unit.
All questions carry equal marks.

5 × 14 = 70M

UNIT-I

1. a) Design a Bus system for four registers each of size eight bits. (8M)
   b) Describe hardware implementation for logical microoperations with a neat sketch. (6M)

(OR)

2. a) How is the Register Reference instruction different from memory referenced instruction? (7M)
   b) Explain hardware implementation for shift microoperations. (7M)

UNIT-II

3. a) With an example specify internal organization of registers in the instruction format. (6M)
   b) Illustrate Selection of address for control memory. (8M)

(OR)

4. a) Write the machine code for the expression X=(A-B)*(C-D) using different instruction formats. (6M)
   b) Use the mapping procedure to generate the micro instruction address for the following op-codes. (8M)

   (i) 1011 (ii) 1101 (iii) 0011 (iv) 1100

UNIT-III

5. a) Write a short note on main memory. (6M)
   b) Explain Associate mapping and Direct mapping process in Cache memory. (8M)

(OR)

6. a) Memory is organized hierarchically, Support the statement. (7M)
   b) Describe RAM and ROM Chip with block diagram and function table. (7M)

UNIT-IV

7. a) Explain strobe mechanism for asynchronous data transfer. (7M)
   b) Explain about programmed I/O for data transfer. (7M)

(OR)

8. a) Explain Types of Interrupts with an example for each. (7M)

   b) Explain with a neat diagram, system configuration incorporating an I/O processor. (7M)

UNIT-V

9. a) Explain Flynn's classification of systems. (7M)

   b) Draw flowchart for addition and subtraction operation on floating point numbers. (7M)

(OR)

10. a) What are the pipeline conflicts that cause the instruction pipeline to deviate from its normal operation? (7M)

    b) Illustrate with an example Booth multiplication algorithm. (7M)

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