8.4 Register Maps

8.4.1 Control Port Registers- Quick Reference

Register Quick Reference ~ Page 0

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P0-R1	Reserved	Reserved	Reserved	RSTM	Reserved	Reserved	Reserved	RSTR	0
			0	0	0	0	0	0	0	0	
2	2	P0-R2	Reserved	Reserved	Reserved	RQST	Reserved	Reserved	Reserved	RQPD	0
			0	0	0	0	0	0	0	0	
3	3	P0-R3	Reserved	Reserved	Reserved	RQMB	Reserved	Reserved	Reserved	RQMA	0
			0	0	0	0	0	0	0	0	
4	4	P0-R4	Reserved	Reserved	Reserved	PLCK	Reserved	Reserved	Reserved	PLLE	1
			0	0	0	0	0	0	0	1	
5	5	P0-R5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6	6	P0-R6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	7	P0-R7	Reserved	Reserved	Reserved	DEMP	Reserved	Reserved	Reserved	SDSL	0
			0	0	0	0	0	0	0	0	
8	8	P0-R8	Reserved	Reserved	G2OE	INTMUTE	G0OE	G1OE	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
9	9	P0-R9	Reserved	Reserved	SCLKP	SCLKO	Reserved	Reserved	Reserved	LRCKFSO	0
			0	0	0	0	0	0	0	0	
10	A	P0-R10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	B	P0-R11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
12	C	P0-R12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RSCLK	RLRCKFS	7C
			0	1	1	1	1	1	0	0	
13	D	P0-R13	Reserved	SREF			Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
14	E	P0-R14	Reserved	SDAC			Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
15	F	P0-R15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...		...	...								...
17	H	P0-R17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
18	12	P0-R18	Reserved	Reserved	Reserved	Reserved	Reserved	GREF			0
			0	0	0	0	0	0	0	0	
19	13	P0-R19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RQSY	10
			0	0	0	0	1	0	0	0	
20	14	P0-R20	Reserved	Reserved	Reserved	Reserved	PPDV				0
			0	0	0	0	0	0	0	0	
21	15	P0-R21	Reserved	Reserved	Reserved	PJDV					0
			0	0	0	0	0	0	0	0	
22	16	P0-R22	Reserved	Reserved	PDDV (MSB)						0
			0	0	0	0	0	0	0	0	
23	17	P0-R23	PDDV (LSB)								0
			0	0	0	0	0	0	0	0	
24	18	P0-R24	–	–	–	–	PRDV				0
			Reserved	Reserved	Reserved	Reserved	0	0	0	0	
25	19	P0-R25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
26	1A	P0-R26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
27	1B	P0-R27	Reserved	DDSP							0
			0	0	0	0	0	0	0	0	
28	1C	P0-R28	Reserved	DDAC							0
			0	0	0	0	0	0	0	0	
29	1D	P0-R29	Reserved	DNCP							0
			0	0	0	0	0	0	0	0	
30	1E	P0-R30	Reserved	DOSR							0
			0	0	0	0	0	0	0	0	
31	1F	P0-R31	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
32	20	P0-R32	DSCLK								0
			0	0	0	0	0	0	0	0	
33	21	P0-R33	DLRCKFS								0
			0	0	0	0	0	0	0	0	
34	22	P0-R34	FSSP		Reserved	I16E	Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
35	23	P0-R35	IDAC (MSB)								1
			0	0	0	0	0	0	0	1	
36	24	P0-R36	IDAC (LSB)								0
			0	0	0	0	0	0	0	0	
37	25	P0-R37	IPLK	DCAS	IDCM	IDCH	IDSK	IDBK	IDFS	Reserved	0
			0	0	0	0	0	0	0	–	
38	26	P0-R38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
39	27	P0-R39	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
40	28	P0-R40	Reserved	Reserved	AFMT		Reserved	Reserved	ALEN		2
			0	0	0	0	0	0	1	0	
41	29	P0-R41	AOFS								0
			0	0	0	0	0	0	0	0	
42	2A	P0-R42	Reserved	Reserved	Reserved	AUPB		Reserved	AUPA		11
			0	0	0	1	0	0	0	1	
43	2B	P0-R43	Reserved	Reserved	Reserved	Reserved	PSEL				1
			0	0	0	0	0	0	0	1	
44	2C	P0-R44	Reserved	Reserved	Reserved	Reserved	Reserved	CMDP			0
			0	0	0	0	0	0	0	0	
45	2D	P0-R45	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
58	3A	P0-R58	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	3B	P0-R59	Reserved	AMTB			Reserved	AMTA			0
			0	0	0	0	0	0	0	0	
60	3C	P0-R60	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCTL		0
			0	0	0	0	0	0	0	0	
61	3D	P0-R61	VOLB								30
			0	0	1	1	0	0	0	0	
62	3E	P0-R62	VOLA								30
			0	0	1	1	0	0	0	0	

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
63	3F	P0-R63	VNDF		VNDS		VNUF		VNUS		22
			0	0	1	0	0	0	1	0	
64	40	P0-R64	VEDF		VEDS		Reserved	Reserved	Reserved	Reserved	2
			0	0	0	0	0	0	1	0	
65	41	P0-R65	Reserved	Reserved	Reserved	Reserved	Reserved	ACTL	AMLE	AMRE	4
			0	0	0	0	0	1	0	0	
66	42	P0-R66	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
81	51	P0-R81	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
82	52	P0-R82	Reserved	Reserved	Reserved	G1SL					0
			0	0	0	0	0	0	0	0	
83	53	P0-R83	Reserved	Reserved	Reserved	G0SL					0
			0	0	0	0	0	0	0	0	
84	54	P0-R84	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
85	55	P0-R85	Reserved	Reserved	Reserved	G2SL					0
			0	0	0	0	0	0	0	0	
86	56	P0-R86	Reserved	Reserved	GOUT2	Reserved	GOUT0	GOUT1	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
87	57	P0-R87	Reserved	Reserved	GINV2	Reserved	GINV0	GINV1	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
88	58	P0-R88	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
89	59	P0-R89	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
90	5A	P0-R90	Reserved	Reserved	Reserved	B1OV	A1OV	B2OV	A2OV	SFOV	0
			0	0	0	0	0	0	0	0	
91	5B	P0-R91	Reserved	DTFS			DTSR				38
			0	0	1	1	1	0	0	0	
92	5C	P0-R92	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DTBR		0
			0	0	0	0	0	0	0	0	
93	5D	P0-R93	DTBR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	40
			0	1	0	0	0	0	0	0	
94	5E	P0-R94	Reserved	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0	0
			0	0	0	0	0	0	0	0	
95	5F	P0-R95	Reserved	Reserved	Reserved	LTSH	Reserved	CKMF	CSRF	CERF	0
			0	0	0	0	0	0	0	0	
96	60	P0-R96	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
107	6B	PO-R107	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
108	6C	P0-R108	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AMBM	AMAM	33
			0	0	1	1	0	0	1	1	
109	6D	P0-R109	Reserved	Reserved	Reserved	SDTM	Reserved	Reserved	Reserved	SHTM	0
			0	0	0	0	0	0	0	0	
110	6E	PO-R110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
113	71	PO-R113	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
114	72	P0-R114	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MTST		3
			0	0	0	0	0	0	1	1	
115	73	P0-R115	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FSMM		0
			0	0	0	0	0	0	0	0	
116	74	P0-R116	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
117	75	P0-R117	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
118	76	P0-R118	BOTM	Reserved	Reserved	Reserved	PSTM				85
			1	0	0	0	0	1	0	1	
119	77	P0-R119	Reserved	Reserved	GPIN						2D
			0	0	1	0	1	1	0	1	
120	78	P0-R120	Reserved	Reserved	Reserved	AMFB	Reserved	Reserved	Reserved	AMFA	0
			0	0	0	0	0	0	0	0	
121	79	P0-R121	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DAMD	0
			0	0	0	0	0	0	0	0	
122	7A	P0-R122	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EIFM	0
			0	0	0	0	0	0	0	0	

Register Quick Reference ~ Page 1

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P1-R1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OSEL	0
			0	0	0	0	0	0	0	0	
2	2	P1-R2	Reserved	Reserved	Reserved	BAGN	Reserved	Reserved	Reserved	AAGN	0
			0	0	0	0	0	0	0	0	
3	3	P1-R3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4	4	P1-R4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5	5	P1-R5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UEPD	UIPD	11
			0	0	0	1	0	0	0	1	
6	6	P1-R6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AMCT	0
			0	0	0	0	0	0	0	0	
7	7	P1-R7	Reserved	Reserved	Reserved	AGBB	Reserved	Reserved	Reserved	AGBA	0
			0	0	0	0	0	0	0	0	
8	8	P1-R8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RCMF	0
			0	0	0	0	0	0	0	0	
9	9	P1-R9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCPD	0
			0	0	0	0	0	0	0	0	

Register Quick Reference ~ Page 44

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P44-R1	Reserved	Reserved	Reserved	Reserved	ACRM	AMDC	ACRS	ASCW	0
			0	0	0	0	0	0	0	0	

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Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
63	3F	P253-63	PLLFLEX1								0
			0	0	0	0	0	0	0	0	
64	40	P253-64	PLLFLEX2								0
			0	0	0	0	0	0	0	0	

8.4.2 Control Port Registers- Detailed Description

8.4.2.1 P0-R1

Reset Modules [4] (R/W)	00000000
This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode.	
Normal	- - - 0 - - - -
Reset modules	- - - 1 - - - -

Reset Register [0] (R/W)	0000000 0
This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported).	
Normal	- - - - - - - 0
Reset mode registers	- - - - - - - 1

8.4.2.2 P0-R2

Standby Request [4] (R/W)	00000000
When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply.	
Normal operation	- - - 0 - - - -
Standby mode	- - - 1 - - - -
Powerdown Request [0] (R/W)	**0000000 0**
When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode.	
Normal operation	- - - - - - - 0
Powerdown mode	- - - - - - - 1

8.4.2.3 P0-R3

Mute Channel B [4] (R/W)	00000000
This bit issues soft mute request for the Channel B. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - 0 - - - -
Mute	- - - 1 - - - -

Mute Channel A [0] (R/W)	0000000**0**
This bit issues soft mute request for the Channel A. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - - - - - 0
Mute	- - - - - - - 1

8.4.2.4 P0-R4

PLL Lock Flag [4] (Read Only)	000**0**0001
This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked.	
The PLL is locked	- - - 0 - - - -
The PLL is not locked	- - - 1 - - - -
PLL Enable [0] (R/W)	**0000000**1
This bit enables or disables the internal PLL. When PLL is disabled, the master clock is switched to the MCLK.	
Disable PLL	- - - - - - - 0
Enable PLL	- - - - - - - 1

8.4.2.5 P0-R7

De-Emphasis Enable [4] (R/W)	000**0**0000
This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1 kHz sampling rate, but can be changed by reprogramming the appropriate coeffients via the coefficient spaces provided in each HybridFlow.	
De-emphasis filter is disabled	- - - 0 - - - -
De-emphasis filter is enabled	- - - 1 - - - -
SDOUT Select [0] (R/W)	**0000000**0
This bit selects what is being output as SDOUT via GPIO pins.	
SDOUT is the DSP output (post-processing)(1)	- - - - - - - 0
SDOUT is the DSP input (pre-processing)	- - - - - - - 1

(1) Some HybridFlows offer several paths from which to take the SDOUT signal. In this case, this bit should be cleared, and the appropirate mixer/mux function in the HybridFlow should be used to determine which processed signal should be presented as the SDOUT signal.

8.4.2.6 P0-R8

GPIO2 Output Enable [5] (R/W)	00**0**00000
This bit sets the direction of the GPIO2 pin	
GPIO2 is input	- - - 0 - - - - -
GPIO2 is output	- - - 1 - - - - -
GPIO0 Output Enable [3] (R/W)	**0000**0**000**
This bit sets the direction of the GPIO0 pin	
GPIO0 is input	- - - - - 0 - - -
GPIO0 is output	- - - - - 1 - - -
GPIO1 Output Enable [2] (R/W)	**00000**0**00**
This bit sets the direction of the GPIO1 pin	
GPIO1 is input	- - - - - 0 - -
GPIO1 is output	- - - - - 1 - -

8.4.2.7 P0-R9

SCLK Polarity [5] (R/W)	00**0**00000
This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCK/FS and SDIN edges are aligned to the rising edge of the SCLK. Normally they are assumed to be aligned to the falling edge of the SCLK.	
Normal SCLK mode	- - - 0 - - - - -
Inverted SCLK mode	- - - 1 - - - - -

SCLK Output Enable [4] (R/W)	00000000
This bit sets the SCLK pin direction to output for I2S master mode operation. In I^2S master mode the TAS5754M outputs the reference SCLK and LRCK/FS, and the external source device provides the SDIN according to these clocks. Use P0-R32 to program the division factor of the MCLK to yield the desired SCLK rate (normally $64F_S$)	
SCLK is input (I^2S slave mode)	- - - 0 - - - -
SCLK is output (I^2S master mode)	- - - 1 - - - -
LRCK/FS Output Enable [0] (R/W)	**0000000 0**
This bit sets the LRCK/FS pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCK/FS, and the external source device provides the SDIN according to these clocks. Use P0/R33 to program the division factor of the SCLK to yield $1F_S$ for LRCK/FS.	
LRCK/FS is input (I^2S slave mode)	- - - - - - - 0
LRCK/FS is output (I^2S master mode)	- - - - - - - 1

8.4.2.8 P0-R12

Master Mode SCLK Divider Reset [1] (R/W)	0111110 0
This bit, when set to 0, will reset the MCLK divider to generate SCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.	
Master mode SCLK clock divider is reset	- - - - - - - 0 -
Master mode SCLK clock divider is functional	- - - - - - - 1 -
Master Mode LRCK/FS Divider Reset [0] (R/W)	**0111110 0**
This bit, when set to 0, will reset the SCLK divider to generate LRCK/FS clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.	
Master mode LRCK/FS clock divider is reset	- - - - - - - 0
Master mode LRCK/FS clock divider is functional	- - - - - - - 1

8.4.2.9 P0-R13

PLL Reference [6:4] (R/W)	0000 0000
This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode.	
The PLL reference clock is MCLK	- 0 0 0 - - - -
The PLL reference clock is MCLK	- 0 0 1 - - - -
Reserved	- 1 0 0 - - - -
The PLL reference clock is GPIO (selected using P0-R18)	- 1 1 1 - - - -

8.4.2.10 P0-R14

DAC Clock Source [6:4] (R/W)	0000 0000
These bits select the source clock for DAC clock divider.	
Master clock (PLL/MCLK and OSC auto-select)	- 0 0 0 - - - -
PLL clock	- 0 0 1 - - - -
Reserved	- 0 1 0 - - - -
MCLK clock	- 0 1 1 - - - -
SCLK clock others:	- 1 0 0 - - - -
Others: reserved (muted)	

8.4.2.11 P0-R18

GPIO Source for PLL Reference clock [2:0] (R/W)	00000 000
These bits select the GPIO pins as clock input source when GPIO is selected as the PLL reference clock source.	
Reserved	- - - - - 0 0 0
Reserved	- - - - - 0 0 1
GPIO1 functions as clock input source	- - - - - 0 1 0

GPIO Source for PLL Reference clock [2:0] (R/W)	00000000
GPIO0 functions as clock input source	- - - - - 0 1 1
Reserved	- - - - - 1 0 0
GPIO2 functions as clock input source	- - - - - 1 0 1
Others: reserved (muted)	

8.4.2.12 P0-R19

Synchronization Request [0] (R/W)	00010000
This bit, when set to 1 will issue the clock resynchronization by synchronously resets the DAC, CP and OSR clocks. The actual clock resynchronization takes place when this bit is set back to 0, where the DAC, CP and OSR clocks are resumed at the beginning of the audio frame.	
Resume DAC, CP and OSR clocks synchronized to the beginning of audio frame	- - - - - - - 0
Halt DAC, CP and OSR clocks as the beginning of re-synchronization process	- - - - - - - 1

8.4.2.13 P0-R20

PLL Divider P-Factor [3:0] (R/W)	00000000
These bits set the PLL divider P factor. These bits are ignored in clock auto set mode.	
Sets the PLL divider P factor to P=1	- - - - 0 0 0 0
Sets the PLL divider P factor to P=2	- - - - 0 0 0 1
Sets the PLL divider P factor to P=3	- - - - 0 0 1 0
...	...
Sets the PLL divider P factor to P=13	- - - - 1 1 0 0
Sets the PLL divider P factor to P=14	- - - - 1 1 0 1
Sets the PLL divider P factor to P=15	- - - - 1 1 1 0
Prohibited (do not set this value)	- - - - 1 1 1 1

8.4.2.14 P0-R21

PLL Divider J-Factor [4:0] (R/W)	00000000
These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Prohibited (do not set this value)	- - - 0 0 0 0 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 1	- - - 0 0 0 0 1
Sets the J part if the overall PLL multiplication factor J.D * R to J = 2	- - - 0 0 0 1 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 3	- - - 0 0 0 1 1
...	...
Sets the J part if the overall PLL multiplication factor J.D * R to J = 61	- - - 1 1 1 0 1
Sets the J part if the overall PLL multiplication factor J.D * R to J = 62	- - - 1 1 1 1 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 63	- - - 1 1 1 1 1

8.4.2.15 P0-R22

PLL Divider D-Factor (Most Significant Bit) [5:0] (Least Significant Bit) [7:0] (R/W)	Decimal
These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0000	0
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0001	1
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0010	2
...	...
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9997	9997
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9998	9998
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9999	9999

8.4.2.16 P0-R24

PLL Divider R-Factor [3:0] (R/W)	00000000
These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Sets the R part if the overall PLL multiplication factor J.D * R to R = 1	- - - - 0 0 0 0
Sets the R part if the overall PLL multiplication factor J.D * R to R = 2	- - - - 0 0 0 1
Sets the R part if the overall PLL multiplication factor J.D * R to R = 3	- - - - 0 0 1 0
...	...
Sets the R part if the overall PLL multiplication factor J.D * R to R = 14	- - - - 1 1 0 1
Sets the R part if the overall PLL multiplication factor J.D * R to R = 15	- - - - 1 1 1 0
Sets the R part if the overall PLL multiplication factor J.D * R to R = 16	- - - - 1 1 1 1

8.4.2.17 P0-R27

DSP Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the DSP clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the DSP clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the DSP clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the DSP clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the DSP clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the DSP clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.18 P0-R28

DAC Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the DAC clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the DAC clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the DAC clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the DAC clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the DAC clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the DAC clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.19 P0-R29

NCP Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the NCP clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the NCP clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the NCP clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the NCP clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the NCP clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the NCP clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.20 P0-R30

OSR Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode.	

OSR Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the OSR clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the OSR clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the OSR clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the OSR clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the OSR clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the OSR clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.21 P0-R32

Master Mode SCLK Divider [6:0] (R/W)	00000000
These bits set the MCLK divider value to generate I2S master SCLK clock.	
These bits set the source clock divider value for the SCLK clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the SCLK clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the SCLK clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the SCLK clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the SCLK clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the SCLK clock Divide by 128	- 1 1 1 1 1 1 1

8.4.2.22 P0-R33

Master Mode LRCK/FS Divider [7:0] (R/W)	00000000
These bits set the I2S master SCLK clock divider value to generate I2S master LRCK/FS clock.	
These bits set the source clock divider value for the LRCK/FS clock. Divide by 1	0 0 0 0 0 0 0 0
These bits set the source clock divider value for the LRCK/FS clock. Divide by 2	0 0 0 0 0 0 0 1
These bits set the source clock divider value for the LRCK/FS clock. Divide by 3	0 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the LRCK/FS clock. Divide by 254	1 1 1 1 1 1 0 1
These bits set the source clock divider value for the LRCK/FS clock. Divide by 255	1 1 1 1 1 1 1 0
These bits set the source clock divider value for the LRCK/FS clock. Divide by 256	1 1 1 1 1 1 1 1

8.4.2.23 P0-R34

16x Interpolation [4] (R/W)	00000000
This bit enables or disables the 16x interpolation mode	
8x interpolation	- - - 0 - - - -
16x interpolation	- - - 1 - - - -
Switching Frequency Speed Mode [1:0] (R/W)	**000000000**
These bits select the F_S operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode.	
Single speed (f_{SW} ≤ 48 kHz)	- - - - - - 0 0
Double speed (48 kHz ≤ f_{SW} ≤ 96 kHz)	- - - - - - 0 1
Quad speed (96 kHz ≤ f_{SW} ≤ 192 kHz)	- - - - - - 1 0

8.4.2.24 P0-R35

Available DSP Clock Cycles (MSB) [7:0] (R/W)	00000001
These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock F_S ratio. These bits are ignored in clock auto set mode.	
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 0

Available DSP Clock Cycles (MSB) [7:0] (R/W)	00000001
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 1
DSP clock:F_S ratio = x	0 0 0 0 0 0 1 0
...	...
DSP clock:F_S ratio = x	1 1 1 1 1 1 0 1
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 0
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 1

8.4.2.25 P0-R36

Available DSP Clock Cycles (LSB) [7:0] (R/W)	00000000
These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock F_S ratio. These bits are ignored in clock auto set mode.	
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 0
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 1
DSP clock:F_S ratio = x	0 0 0 0 0 0 1 0
...	...
DSP clock:F_S ratio = x	1 1 1 1 1 1 0 1
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 0
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 1

8.4.2.26 P0-R37

Ignore F_S Detection [6] (R/W)	00000000
This bit controls whether to ignore the F_S detection. When ignored, F_S error will not cause a clock error.	
Regard F_S detection	- 0 - - - - - -
Ignore F_S detection	- 1 - - - - - -
Ignore SCLK Detection [5] (R/W)	**00000000**
This bit controls whether to ignore the SCLK detection against LRCK/FS. The SCLK must be stable between $32F_S$ and $256F_S$ inclusive or an error will be reported. When ignored, a SCLK error will not cause a clock error.	
Regard SCLK detection	- - 1 - - - - -
Ignore SCLK detection	- - 0 - - - - -
Ignore MCLK Detection [4] (R/W)	**00000000**
This bit controls whether to ignore the MCLK detection against LRCK/FS. Only some certain MCLK ratios within some error margin are allowed. When ignored, an MCLK error will not cause a clock error.	
Regard MCLK detection	- - - 0 - - - -
Ignore MCLK detection	- - - 1 - - - -
Ignore Clock Halt Detection [3] (R/W)	**00000000**
This bit controls whether to ignore the MCLK halt (static or frequency is lower than acceptable) detection. When ignored an MCLK halt will not cause a clock error.	
Regard MCLK halt detection	- - - - - - 0 -
Ignore MCLK halt detection	- - - - - - 1 -
Ignore LRCK/FS and SCLK Missing Detection [2] (R/W)	**00000000**
This bit controls whether to ignore the LRCK/FS and SCLK missing detection. The LRCK/FS and SCLK need to be in low state (not only static) to be deemed missing. When ignored an LRCK/FS and SCLK missing will not cause the DAC go into powerdown mode.	
Regard LRCK/FS and SCLK missing detection	- - - - - 0 - -
Ignore LRCK/FS and SCLK missing detection	- - - - - 1 - -
Disable Clock Divider Autoset [1] (R/W)	**00000000**
This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually.	
Enable clock auto set	- - - - - - 0 -

Disable Clock Divider Autoset [1] (R/W)	0000000**0**
Disable clock auto set	- - - - - - 1 -
Ignore PLL Lock Detection [0] (R/W)	**0000000**0
This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at P0-R4, bit 4 is always correct regardless of this bit.	
PLL unlocks raise clock error	- - - - - - - 0
PLL unlocks are ignored	- - - - - - - 1

8.4.2.27 P0-R40

I^2S Data Format [5:4] (R/W)	00**00**0010
These bits control both input and output audio interface formats for DAC operation.	
Input and output audio interface formats for DAC operation is I^2S	- - 0 0 - - - -
Input and output audio interface formats for DAC operation is TDM/DSP	- - 0 1 - - - -
Input and output audio interface formats for DAC operation is RTJ	- - 1 0 - - - -
Input and output audio interface formats for DAC operation is LTJ	- - 1 1 - - - -
I^2S Word Length [1:0] (R/W)	**000000010**
These bits control both input and output audio interface sample word lengths for DAC operation.	
Input and output audio interface sample word length for DAC operation is 16 bits	- - - - - - 0 0
Input and output audio interface sample word length for DAC operation is 20 bits	- - - - - - 0 1
Input and output audio interface sample word length for DAC operation is 24 bits	- - - - - - 1 0
Input and output audio interface sample word length for DAC operation is 32 bits	- - - - - - 1 1

8.4.2.28 P0-R41

I^2S Shift [7:0] (R/W)	00000000
These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample.	
Offset (number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample) is 0 SCLK (no offset)	0 0 0 0 0 0 0 0
Offset is 1 SCLK	0 0 0 0 0 0 0 1
Offset is 2 SCLKs	0 0 0 0 0 0 1 0
...	...
Offset is 254 SCLKs	1 1 1 1 1 1 0 1
Offset is 255 SCLKs	1 1 1 1 1 1 1 0
Offset is 256 SCLKs	1 1 1 1 1 1 1 1

8.4.2.29 P0-R42

Channel B DAC Data Path [5:4] (R/W)	00**00**0001
These bits control the Channel B audio data path connection.	
Zero data (mute)	- - 0 0 - - - -
Channel B data	- - 0 1 - - - -
Channel A data	- - 1 0 - - - -
Reserved (do not set)	- - 1 1 - - - -
Channel A DAC Data Path [1:0] (R/W)	**000000001**
These bits control the Channel A audio data path connection.	
Zero data (mute)	- - - - - - 0 0
Channel A data	- - - - - - 0 1
Channel B data	- - - - - - 1 0
Reserved (do not set)	- - - - - - 1 1

8.4.2.30 P0-R43

DSP Program Selection [4:0] (R/W)	00000001
These bits select the DSP program to use for audio processing.	
Reserved (do not set)	- - - 0 0 0 0 0
8x, 4x, or 2x FIR interpolation filter with de-emphasis	- - - 0 0 0 0 1
8x, 4x, or 2x Low latency IIR interpolation filter with de-emphasis	- - - 0 0 0 1 0
16x FIR interpolation filter with de-emphasis	- - - 0 0 0 1 1
16x Low latency IIR interpolation filter with de-emphasis	- - - 0 0 1 0 0
Fixed process flow with configurable parameters	- - - 0 0 1 0 1
Reserved (do not set)	- - - 0 0 1 1 0
8× Ringing-less low latency FIR interpolation filter without de-emphasis	- - - 0 0 1 1 1
Others: Reserved (do not set)	...
User program in RAM	- - - 1 1 1 1 1

8.4.2.31 P0-R44

Clock Missing Detection Period [2:0] (R/W)	00000000
These bits set how long both SCLK and LRCK/FS keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode.	
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 1 second	- - - - - 0 0 0
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 2 seconds	- - - - - 0 0 1
...	...
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 7 seconds	- - - - - 1 1 0
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 8 seconds	- - - - - 1 1 1

8.4.2.32 P0-R59

Auto Mute Time for Channel B [6:4] (R/W)	00000000
These bits specify the length of consecutive zero samples at Channel B before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.	
Length of consecutive zero samples before the channel can be auto muted is 21 ms	- 0 0 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 106 ms	- 0 0 1- - - -
Length of consecutive zero samples before the channel can be auto muted is 213 ms	- 0 1 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 533 ms	- 0 1 1 - - - -
Length of consecutive zero samples before the channel can be auto muted is 1.07 seconds	- 1 0 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 2.13 seconds	- 1 0 1 - - - -
Length of consecutive zero samples before the channel can be auto muted is 5.33 seconds	- 1 1 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 10.66 seconds	- 1 1 1 - - - -
Auto Mute Time for Channel A [2:0] (R/W)	**00000000**
These bits specify the length of consecutive zero samples at Channel A before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.	
Length of consecutive zero samples before the channel can be auto muted is 21 ms	- - - - - 0 0 0
Length of consecutive zero samples before the channel can be auto muted is 106 ms	- - - - - 0 0 1
Length of consecutive zero samples before the channel can be auto muted is 213 ms	- - - - - 0 1 0
Length of consecutive zero samples before the channel can be auto muted is 533 ms	- - - - - 0 1 1
Length of consecutive zero samples before the channel can be auto muted is 1.07 seconds	- - - - - 1 0 0
Length of consecutive zero samples before the channel can be auto muted is 2.13 seconds	- - - - - 1 0 1
Length of consecutive zero samples before the channel can be auto muted is 5.33 seconds	- - - - - 1 1 0

Auto Mute Time for Channel A [2:0] (R/W)	00000000
Length of consecutive zero samples before the channel can be auto muted is 10.66 seconds	- - - - - 1 1 1

8.4.2.33 P0-R60

Digital Volume Control [1:0] (R/W)	0000000 00
These bits control the behavior of the digital volume.	
The volume for Channels A and B are independent	- - - - - - 0 0
Channel A volume follows Channel B setting	- - - - - - 0 1
Channel B volume follows Channel A setting	- - - - - - 1 0
Reserved (The volume for Channels A and B are independent)	- - - - - - 1 1

8.4.2.34 P0-R61

Channel B Digital Volume [7:0] (R/W)	00110000
These bits control the Channel B digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.	
Channel B digital volume is 24 dB	0 0 0 0 0 0 0 0
Channel B digital volume is 23.5 dB	0 0 0 0 0 0 0 1
Channel B digital volume is 23 dB.	0 0 0 0 0 0 1 0
...	...
Channel B digital volume is 0.5 dB	0 0 1 0 0 0 0 0
Channel B digital volume is 0 dB	0 0 1 1 0 0 0 0
Channel B digital volume is –0.5 dB	0 0 1 1 0 0 0 1
...	...
Channel B digital volume is –102.5 dB	1 1 1 1 1 1 0 1
Channel B digital volume is –103 dB	1 1 1 1 1 1 1 0
Reserved	1 1 1 1 1 1 1 1

8.4.2.35 P0-R62

Channel A Digital Volume [7:0] (R/W)	00110000
These bits control the Channel A digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.	
Channel A digital volume is 24 dB	0 0 0 0 0 0 0 0
Channel A digital volume is 23.5 dB	0 0 0 0 0 0 0 1
Channel A digital volume is 23 dB.	0 0 0 0 0 0 1 0
...	...
Channel A digital volume is 0.5 dB	0 0 1 0 0 0 0 0
Channel A digital volume is 0 dB	0 0 1 1 0 0 0 0
Channel A digital volume is –0.5 dB	0 0 1 1 0 0 0 1
...	...
Channel A digital volume is –102.5 dB	1 1 1 1 1 1 0 1
Channel A digital volume is –103 dB	1 1 1 1 1 1 1 0
Reserved	1 1 1 1 1 1 1 1

8.4.2.36 P0-R63

Digital Volume Normal Ramp-Down Frequency [7:6] (R/W)	00100010
These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by SPK_MUTE pin or P0-R3.	
The frequency of the digital volume updates is every 1 F_S period	0 0 - - - - - -
The frequency of the digital volume updates is every 2 F_S period	0 1 - - - - - -
The frequency of the digital volume updates is every 4 F_S period	1 0 - - - - - -

Digital Volume Normal Ramp-Down Frequency [7:6] (R/W)	00100010
Directly sets the volume to zero (Instant mute)	1 1 - - - - - -
Digital Volume Normal Ramp Down Step [5:4] (R/W)	**00100010**
These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by SPK_MUTE pin or P0-R3.	
Decrement by 4 dB for each update	- - 0 0 - - - -
Decrement by 2 dB for each update	- - 0 1 - - - -
Decrement by 1 dB for each update	- - 1 0 - - - -
Decrement by 0.5 dB for each update	- - 1 1 - - - -
Digital Volume Normal Ramp-Up Frequency [3:2] (R/W)	**00100010**
These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by SPK_MUTE pin or P0-R3.	
The frequency of the digital volume updates is every 1 F_S period	- - - - 0 0 - -
The frequency of the digital volume updates is every 2 F_S period	- - - - 0 1 - -
The frequency of the digital volume updates is every 4 F_S period	- - - - 1 0 - -
Directly sets the volume to zero (Instant unmute)	- - - - 1 1 - -
Digital Volume Normal Ramp Up Step [1:0] (R/W)	**00100010**
These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by SPK_MUTE pin or P0-R3.	
Increment by 4 dB for each update	- - - - - - 0 0
Increment by 2 dB for each update	- - - - - - 0 1
Increment by 1 dB for each update	- - - - - - 1 0
Increment by 0.5 dB for each update	- - - - - - 1 1

8.4.2.37 P0-R64

Digital Volume Emergency Ramp Down Frequency [7:6] (R/W)	00000010
These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.	
The frequency of the digital volume updates is every 1 F_S period	0 0 - - - - - -
The frequency of the digital volume updates is every 2 F_S period	0 1 - - - - - -
The frequency of the digital volume updates is every 4 F_S period	1 0 - - - - - -
Directly sets the volume to zero (Instant mute)	1 1 - - - - - -
Digital Volume Emergency Ramp Down Step [5:4] (R/W)	**00000010**
These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.	
Decrement by 4 dB for each update	- - 0 0 - - - -
Decrement by 2 dB for each update	- - 0 1 - - - -
Decrement by 1 dB for each update	- - 1 0 - - - -
Decrement by 0.5 dB for each update	- - 1 1 - - - -

8.4.2.38 P0-R65

Auto Mute Control [2] (R/W)	00000100
This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with P0-R59.	
Auto mute Channel B and Channel A independently	- - - - - 0 - -
Auto mute Channels A and Channel B only when both channels are about to be auto muted	- - - - - 1 - -
Auto Mute Channel B [1] (R/W)	**00000100**
This bit enables or disables auto mute on Channel A. Note that when Channel A auto mute is disabled and the P0-R65, bit 2 is set to 1, the Channel B will also never be auto muted.	
Disable Channel A auto mute	- - - - - - - 0 -
Enable Channel A auto mute	- - - - - - - 1 -

Auto Mute Channel A [0] (R/W)	00000100
This bit enables or disables auto mute on Channel B. Note that when Channel B auto mute is disabled and the P0-R65, bit 2 is set to 1, the Channel A will also never be auto muted.	
Disable Channel B auto mute	- - - - - - - 0
Enable Channel B auto mute	- - - - - - - 1

8.4.2.39 P0-R82

GPIO1 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO1. To actually output the selected signal, the GPIO1 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO1 output	- - - 0 0 0 0 1
Register GPIO1 output (P0-R86, bit 2)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channel A and Channel B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.40 P0-R83

GPIO0 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO0. To actually output the selected signal, the GPIO0 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO0 output	- - - 0 0 0 0 1
Register GPIO0 output (P0-R86, bit 2)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channel A and Channel B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.41 P0-R85

GPIO2 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO2 output	- - - 0 0 0 0 1
Register GPIO2 output (P0-R86, bit 5)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channels A and B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.42 P0-R86

GPIO2 Output Control [5] (R/W)	00000000
This bit controls the GPIO2 output when the selection at P0-R85 is set to 0010 (register output).	
Output low	- - - 0 - - - - -
Output high	- - - 1 - - - - -
GPIO0 Output Control [3] (R/W)	**00000000**
This bit controls the GPIO0 output when the selection at P0-R83 is set to 0010 (register output).	
Output low	- - - - - 0 - - -
Output high	- - - - - 1 - - -
GPIO1 Output Control [2] (R/W)	**00000000**
This bit controls the GPIO1 output when the selection at P0-R82 is set to 0010 (register output).	
Output low	- - - - - 0 - -
Output high	- - - - - 1 - -

8.4.2.43 P0-R87

GPIO2 Output Inversion [5] (R/W)	00000000
This bit controls the polarity of GPIO2 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - 0 - - - - -
Inverted	- - - 1 - - - - -
GPIO0 Output Inversion [3] (R/W)	**00000000**
This bit controls the polarity of GPIO0 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - - - 0 - - -
Inverted	- - - - - 1 - - -

GPIO1 Output Inversion [2] (R/W)	00000000
This bit controls the polarity of GPIO1 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - - - 0 - -
Inverted	- - - - - 1 - -

8.4.2.44 P0-R90

Channel B-1 Overflow [4] (Read Only)	00000000
This bit indicates whether the Channel B of DSP first output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - 0 - - - -
Overflow occurred	- - - 1 - - - -
Channel A-1 Overflow [3] (Read Only)	**00000000**
This bit indicates whether the Channel A of DSP first output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - 0 - - -
Overflow occurred	- - - - - 1 - - -
Channel B-2 Overflow [2] (Read Only)	**00000000**
This bit indicates whether the Channel B of DSP second output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - 0 - -
Overflow occurred	- - - - - 1 - -
Channel A-2 Overflow [1] (Read Only)	**00000000**
This bit indicates whether the Channel A of DSP second output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - - - 0 -
Overflow occurred	- - - - - - - 1 -
Shifter Overflow [0] (Read Only)	**00000000**
This bit indicates whether overflow occurred in the DSP shifter (possible sample corruption). This bit is sticky and is cleared when read.	
No overflow	- - - - - - - 0
Overflow occurred	- - - - - - - 1

8.4.2.45 P0-R91

Detected F_S [6:4] (Read Only)	00111000
These bits indicate the currently detected audio sampling rate.	
Error (out-of-valid range)	- 0 0 0 - - - -
8 kHz	- 0 0 1 - - - -
16 kHz	- 0 1 0 - - - -
32 kHz to 48 kHz	- 0 1 1 - - - -
88.2 kHz to 96 kHz	- 1 0 0 - - - -
176.4 kHz to 192 kHz	- 1 0 1 - - - -
Reserved	- 1 1 1 - - - -
Detected MCLK Ratio [3:0] (Read Only)	**00111000**
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz.	
Ratio error (The MCLK ratio is not allowed)	- - - - 0 0 0 0
MCLK = 32 F_S	- - - - 0 0 0 1
MCLK = 48 F_S	- - - - 0 0 1 0
MCLK = 64 F_S	- - - - 0 0 1 1
MCLK = 128 F_S	- - - - 0 1 0 0
MCLK = 192 F_S	- - - - 0 1 0 1
MCLK = 256 F_S	- - - - 0 1 1 0
MCLK = 384 F_S	- - - - 0 1 1 1

Detected MCLK Ratio [3:0] (Read Only)	00111000
MCLK = 512 F_S	- - - - 1 0 0 0
MCLK = 768 F_S	- - - - 1 0 0 1
MCLK = 1024 F_S	- - - - 1 0 1 0
MCLK = 1152 F_S	- - - - 1 0 1 1
MCLK = 1536 F_S	- - - - 1 1 0 0
MCLK = 2048 F_S	- - - - 1 1 0 1
MCLK = 3072 F_S	- - - - 1 1 1 0

8.4.2.46 P0-R92

Detected SCLK Ratio [0] (Read Only)	00000000
This bit is the MSB of the 9 bit word that describes the currently detected SCLK to LRCK/FS Ratio. Binary to decimal conversion gives ratio.	
Decode with P0-93 to determine value.	- - - - - - - 0
	- - - - - - - 1

8.4.2.47 P0-R93

Detected SCLK Ratio [7:0] (Read Only)	00000000
These bits are bit 1 through bit 8 of the 9 bit word that describes the currently detected SCLK to LRCK/FS Ratio. Binary to decimal conversion gives ratio.	
LSB of 9 bit word	- - - - - - - 0
2nd LSB of 9 bit word	- - - - - - 0 -
...	...
2nd MSB of 9 bit word (MSB is found in P0-R92-B0)	0 - - - - - - -
Detected MCLK Ratio [3:0] (Read Only)	**00111000**
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz.	
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz. Ratio error (The MCLK ratio is not allowed)	- - - - 0 0 0 0
MCLK = 32 F_S	- - - - 0 0 0 1
MCLK = 48 F_S	- - - - 0 0 1 0
MCLK = 64 F_S	- - - - 0 0 1 1
MCLK = 128 F_S	- - - - 0 1 0 0
MCLK = 192 F_S	- - - - 0 1 0 1
MCLK = 256 F_S	- - - - 0 1 1 0
MCLK = 384 F_S	- - - - 0 1 1 1
MCLK = 512 F_S	- - - - 1 0 0 0
MCLK = 768 F_S	- - - - 1 0 0 1
MCLK = 1024 F_S	- - - - 1 0 1 0
MCLK = 1152 F_S	- - - - 1 0 1 1
MCLK = 1536 F_S	- - - - 1 1 0 0
MCLK = 2048 F_S	- - - - 1 1 0 1
MCLK = 3072 F_S	- - - - 1 1 1 0

8.4.2.48 P0-R94

Clock Detector Status [6] (Ready Only)	00000000
This bit indicates whether the MCLK clock is present or not.	
MCLK is present	- 0 - - - - - -

Clock Detector Status [6] (Ready Only)	00000000
MCLK is missing (halted)	- 1 - - - - - -
Clock Detector Status 5 [5] (Ready Only)	**00000000**
This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled.	
PLL is locked	- - 1 - - - - -
PLL is unlocked	- - 0 - - - - -
Clock Detector Status 4 [4] (Ready Only)	**00000000**
This bit indicates whether the both LRCK/FS and SCLK are missing (tied low) or not.	
LRCK/FS and/or SCLK is present	- - - 0 - - - -
LRCK/FS and SCLK are missing	- - - 1 - - - -
Clock Detector Status 3 [3] (Read Only)	**00000000**
This bit indicates whether the combination of current sampling rate and MCLK ratio is valid for clock auto set.	
The combination of FS:MCLK ratio is valid	- - - - - 0 - - -
Error (clock auto set is not possible)	- - - - - 1 - - -
Clock Detector Status 2 [2] (Read Only)	**00000000**
This bit indicates whether the MCLK is valid or not. The MCLK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCK/FS is less than or equal to 5 SCLKs, this flag will be asserted (MCLK invalid reported).	
MCLK is valid	- - - - - 0 - -
MCLK is invalid	- - - - - 1 - -
Clock Detector Status 1 [1] (Read Only)	**00000000**
This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-256F_S to be valid.	
SCLK is valid	- - - - - - - 0 -
SCLK is invalid	- - - - - - - 1 -
Clock Detector Status 0 [0] (Read Only)	**00000000**
This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and P0-R37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore).	
Sampling rate is valid	- - - - - - - 0
Sampling rate is invalid	- - - - - - - 1

8.4.2.49 P0-R95

Latched Clock Halt [4] (Ready Only)	00000000
This bit indicates whether MCLK halt has occurred. The bit is cleared when read.	
MCLK halt has not occurred	- - - 0 - - - -
MCLK halt has occurred since last read	- - - 1 - - - -
Clock Missing [2] (Read Only)	**00000000**
This bit indicates whether the LRCK/FS and SCLK are missing (tied low).	
One or both of LRCK/FS SCLK is present	- - - - - 0 - -
Both LRCK/FS and SCLK are missing	- - - - - 1 - -
Clock Resync Request [1] (Read Only)	**00000000**
This bit indicates whether the clock resynchronization is in progress.	
Not resynchronizing	- - - - - - - 0 -
Clock resynchronization is in progress	- - - - - - - 1 -
Clock Error [0] (Read Only)	**00000000**
This bit indicates whether a clock error is being reported.	
Clock is valid	- - - - - - - 0
Clock is invalid (Error)	- - - - - - - 1

8.4.2.50 P0-R108

Channel B Analog Mute Monitor [1] (Read Only)	00110011
This bit is a monitor for Channel B analog mute status.	
Mute	- - - - - - - 0 -
Unmute	- - - - - - - 1 -
Channel A Analog Mute Monitor [0] (Read Only)	**00110011**
This bit is a monitor for Channel A analog mute status.	
Mute	- - - - - - - 0
Unmute	- - - - - - - 1

8.4.2.51 P0-R109

Short Detect Monitor [4] (Ready Only)	00000000
This bit indicates whether line output short is occurring on the DAC_OUTx line.	
Normal (No short)	- - - 0 - - - -
Line output is being shorted	- - - 1 - - - -
Short Detected Monitor [0] (Read Only)	**00000000**
This bit indicates whether line output short on DAC_OUTx has occurred since last read. This bit is sticky and is cleared when read.	
No short	- - - - - - - 0
Line output short occurred	- - - - - - - 1

8.4.2.52 P0-R114

SPK_MUTE Decoder Status[1:0] (Read Only)	00000000
These bits indicate the output of the SPK_MUTE level decoder for monitoring purpose.	
VDD > SPK_MUTE	- - - - - - 0 0
VDD ≤ SPK_MUTE < 0.7 × VDD	- - - - - - 0 1
Reserved (do not set)	- - - - - - 1 0
0.7 × VDD ≤ SPK_MUTE	- - - - - - 1 1

8.4.2.53 P0-R115

F_S Speed Mode Monitor [1:0] (Read Only)	00000000
These bits indicate the actual F_S operation mode being used. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled.	
Single speed (f_S ≤ 48 kHz)	- - - - - - 0 0
Double speed (48 kHz ≤ f_S ≤ 96 kHz)	- - - - - - 0 1
Quad speed (96 kHz ≤ f_S ≤ 192 kHz)	- - - - - - 1 0

8.4.2.54 P0-R117

DSP Boot Done Flag [7] (R/W)	00000000
This bit indicates whether the DSP boot is completed.	
DSP is booting	0 - - - - - - -
DSP boot completed	1 - - - - - - -
Power State [3:0] (Read Only)	**00000000**
These bits indicate the current power state of the DAC	
Powerdown	- - - - 0 0 0 0
Wait for CP voltage valid	- - - - 0 0 0 1
Calibration	- - - - 0 0 1 0
Calibration	- - - - 0 0 1 1

Power State [3:0] (Read Only)	00000000
Volume ramp up	- - - - 0 1 0 0
Run (Playing)	- - - - 0 1 0 1
Line output short or low impedance	- - - - 0 1 1 0
Volume ramp down	- - - - 0 1 1 1
Standby	- - - - 1 0 0 0

8.4.2.55 P0-R119

GPIO2 Input State [5] (Read Only)	00101101
This bit indicates the logic level at GPIO2 pin.	
GPIO2 logic level low	- - - 0 - - - - -
GPIO2 logic level high	- - - 1 - - - - -
GPIO0 Input State [3] (Read Only)	**00101101**
This bit indicates the logic level at GPIO0 pin.	
GPIO0 logic level low	- - - - - 0 - - -
GPIO0 logic level high	- - - - - 1 - - -
GPIO1 Input State [2] (Read Only)	**00101101**
This bit indicates the logic level at GPIO1 pin.	
GPIO1 logic level low	- - - - - 0 - -
GPIO1 logic level high	- - - - - 1 - -

8.4.2.56 P0-R120

Auto Mute Flag for Channel B [4] (Read Only)	00000000
This bit indicates the auto mute status for Channel B.	
Not auto muted	- - - 0 - - - -
Auto muted	- - - 1 - - - -
Auto Mute Flag for Channel A [0] (Read Only)	**00000000**
This bit indicates the auto mute status for Channel A.	
Not auto muted	- - - - - - - 0
Auto muted	- - - - - - - 1

8.4.2.57 P0-R121

DAC Mode [0] (R/W)	00000000
This bit controls the DAC mode.	
Mode1	- - - - - - - 0
Mode2	- - - - - - - 1

8.4.2.58 P1-R2

Analog Gain Control for Channel B [4] (R/W)	00000000
This bit controls the Channel B analog gain.	
0 dB	- - - 0 - - - -
–6 dB	- - - 1 - - - -
Analog Gain Control for Channel A [0] (R/W)	**00000000**
This bit controls the Channel A analog gain.	
0 dB	- - - - - - - 0
–6 dB	- - - - - - - 1

8.4.2.59 P1-R5

External UVP Control [1] (R/W)	00010001
This bit enables or disables detection of power supply drop via SPK_MUTE pin (external UVLO protection).	
Enabled	- - - - - - - 0 -
Disabled	- - - - - - - 1 -
Internal UVP Control [0] (R/W)	**00010001**
This bit enables or disables internal detection of AVDD voltage drop (internal UVLO protection).	
Enabled	- - - - - - - 0
Disabled	- - - - - - - 1

8.4.2.60 P1-R6

Analog Mute Control [0] (R/W)	00000000
This bit enables or disables analog mute following digital mute.	
Enabled	- - - - - - - 0
Disabled	- - - - - - - 1

8.4.2.61 P1-R7

Analog +10% Gain for Channel B [4] (R/W)	00000000
This bit enables or disables amplitude boost mode for Channel B.	
Normal amplitude	- - - 0 - - - -
+10% (+0.8 dB) boosted amplitude	- - - 1 - - - -
Analog +10% Gain for Channel A [0] (R/W)	**00000000**
This bit enables or disables amplitude boost mode for Channel A.	
Normal amplitude	- - - - - - - 0
+10% (+0.8 dB) boosted amplitude	- - - - - - - 1

8.4.2.62 P1-R8

VCOM Reference Ramp-Up [0] (R/W)	00000000
This bit controls the VCOM voltage ramp up speed.	
Normal ramp-up time is approximately 600 ms with external capacitance = 1 µF	- - - - - - - 0
Fast ramp-up time is approximately 3 ms with external capacitance = 1 µF	- - - - - - - 1

8.4.2.63 P1-R9

VCOM Power-Down Control [0] (R/W)	00000000
This bit controls VCOM powerdown switch.	
VCOM is powered on	- - - - - - - 0
VCOM is powered down	- - - - - - - 1

8.4.2.64 P44-R1

Active CRAM Monitor [3] (Read Only)	00000000
This bit indicates which CRAM is being accessed by the DSP when adaptive mode is disabled. When adaptive mode is enabled, this bit has no meaning.	
CRAM A is being used by the DSP	- - - - - 0 - - -
CRAM B is being used by the DSP	- - - - - 1 - - -

Adaptive Mode Control [2] (R/W)	00000000
This bit controls the DSP adaptive mode. When in adaptive mode, only CRAM A is accessible via serial interface when the DSP is disabled (DAC in standby state), while when the DSP is enabled (DAC is run state) the CRAM A can only be accessed by the DSP and the CRAM B can only be accessed by the serial interface, or vice versa depending on the value of CRAMSTAT. When not in adaptive mode, both CRAM A and B can be accessed by the serial interface when the DSP is disabled, but when the DSP is enabled, no CRAM can be accessed by serial interface. The DSP can access either CRAM, which can be monitored at SWPMON.	
Adaptive mode disabled	- - - - - 0 - -
Adaptive mode enabled	- - - - - 1 - -
Active CRAM Selection [1] (Read Only)	**00000000**
This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I^{2}C)	
CRAM A is active and being used by the DSP	- - - - - - - 0 -
CRAM B is active and being used by the DSP	- - - - - - - 1 -
Switch Active CRAM [0] (R/W)	**00000000**
This bit is used to request switching roles of the two buffers, (switching the active buffer role between CRAM A and CRAM B). This bit is cleared automatically when the switching process completed.	
No switching requested or switching completed	- - - - - - - 0
Switching is being requested	- - - - - - - 1

8.4.2.65 P253-R63

Clock Flex Register No. 1 [7:0] (R/W)	00000000
Using this register allows the PLL I/O to be set to GPIOs.	
Set to 0x11	0 0 0 0 0 0 0 0
	0 0 0 0 0 0 0 1
	0 0 0 0 0 0 1 0
...	...
	0 0 1 0 0 0 0 0
	0 0 1 1 0 0 0 0
	0 0 1 1 0 0 0 1
	...
	1 1 1 1 1 1 0 1
	1 1 1 1 1 1 1 0
	1 1 1 1 1 1 1 1

8.4.2.66 P253-R64

Clock Flex Register No. 2 [7:0] (R/W)	00000000
Using this register allows the PLL I/O to be set to GPIOs.	
Set to 0x11	0 0 0 0 0 0 0 0
	0 0 0 0 0 0 0 1
	0 0 0 0 0 0 1 0
...	...
	0 0 1 0 0 0 0 0
	0 0 1 1 0 0 0 0
	0 0 1 1 0 0 0 1
	...
	1 1 1 1 1 1 0 1
	1 1 1 1 1 1 1 0
	1 1 1 1 1 1 1 1

9 Applications and Implementation

9.1 Application Information

One of the most significant benefits of the TAS5754M device is the ability to be used in a variety of applications and with an assortment of signal processing options. This section details the information needed to configure the device for several popular configurations and provides guidance on integrating the TAS5754M device into the larger system.

9.1.1 External Component Selection Criteria

The *Supporting Component Requirements* table in each application description section lists the details of the supporting required components in each of the *System Application Schematics*.

Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design, to ease inventory management, and reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor may be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, a several unique resistors, having all the same size and value but with different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation may seem excessive, the benefits of having fewer components in the design may far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in it during normal use case.

9.1.2 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list were intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extends from the TAS5754M device between two pads of a surface mount component and into to the surrounding copper for increased heat-sinking of the device. While components may be offered in smaller or larger package sizes, it is highly recommended that the package size remain identical to that used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, optimizing thermal, electromagnetic, and audio performance of the TAS5754M device in circuit in the final system.

9.1.3 Amplifier Output Filtering

The TAS5754M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the *L-C Filter*, due to the presence of an inductive element *L* and a capacitive element *C* to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that do not have other circuits which are sensitive to EMI, a simple ferrite bead or ferrite bead and capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors may be preferred due to audio characteristics. Refer to the application report SLOA119 for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

9.2 Typical Applications

9.2.1 2.0 (Stereo BTL) System

For the stereo (BTL) PCB layout, see Figure 87.

A 2.0 system generally refers to a system in which there are two full range speakers without a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a *stereo pair*, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

It is important to note that the HybridFlows which have been developed for specifically for stereo applications will frequently apply the same equalizer curves to the left channel and the right channel. This maximizes the processing capabilities of each HybridFlow by minimizing the cycles required by the BiQuad filters.

When two signals that are not two separate signals, but instead are derived from a single signal which is separated into low frequency and high frequency by the signal processor, the application is commonly referred to as 1.1 or *Bi-Amped* systems. The 2.0 (Stereo BTL) System application is shown in Figure 80.