Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation

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ABSTRACT

In recent years, on-chip interconnect has had an increasingly important impact on overall system performance. Much work has been done to develop algorithms which can efficiently and accurately predict delay through on-chip interconnect. These algorithms compute a reduced-order approximation (usually based on the "Elmore delay") for voltage-transfer ratios (from source to loads) in an RC-tree model for the interconnect. However, much less emphasis has been placed on accurately approximating the *driving-point* characteristic at the root of an RC-tree. A good driving-point approximation is needed to accurately predict how delay through a gate is influenced by the interconnect which that gate must drive. Macromodels for on-chip gates typically only consider total capacitance of the driven interconnect, completely ignoring series resistance. In this paper, we present an efficient algorithm which accounts for series resistance by computing a reduced-order approximation for the driving-point admittance of an RC-tree. Using an ECL clock buffer as an example, we demonstrate a significant improvement in accuracy.

1. INTRODUCTION

1.1 Interconnect Delay

"Interconnect delay" has two distinct components, which can best be illustrated by considering a simplified net with no branching and only one load gate (see Fig. 1). Let $T_{AB}(0)$ represent delay through an *unloaded* source gate. Let $T_{AB}(L)$ represent delay through the same source gate *loaded* by an interconnect net of length L. Because of loading effects on the source gate, $T_{AB}(L)$ exceeds $T_{AB}(0)$.

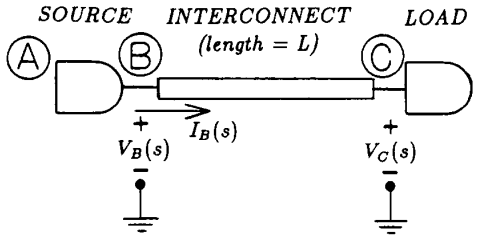

Figure 1: Simplified net (for illustrating components of T_{int}).

We define "interconnect delay" as follows:

$$T_{int} \triangleq T_{AC} - T_{AB}(0) = [T_{AB}(L) - T_{AB}(0)] + T_{BC}. \quad (1)$$

The two components are: *extra source gate delay* ($T_{AB}(L) - T_{AB}(0)$), which is the focus of this paper; and *propagation delay* (T_{BC}), which has been extensively analyzed [2]-[4].

1.2 Delay Modeling

On-chip interconnect is well modeled by RC-trees [1]. In the last several years, research has been active on fast algorithms for on-chip delay estimation and bounding using RC-tree models [2]-[6]. These algorithms have proven to be useful alternatives to "exact" numerical simulation (e.g., SPICE [7]), where computation time becomes quite large even for relatively small circuits. However, regarding interconnect delay, the cited works [2]-[6] concentrate mainly on the propagation component (T_{BC}). A reduced-order approximation, based on the "Elmore delay" [8], is computed for the voltage-transfer ratio ($V_C(s)/V_B(s)$) from the source gate output to a given load gate input. See Section 2 for a brief review of these voltage-transfer ratio approximations.

In this paper, we concentrate on the extra source gate component ($T_{AB}(L) - T_{AB}(0)$) of T_{int}. We compute a reduced-order approximation for the driving-point admittance ($I_B(s)/V_B(s)$) seen from the output of the source gate. This approximation for the driving-point admittance of interconnect is *independent* of any modeling approximations made for the non-linear behavior of the source gate. Our approximation accounts for distributed series resistance present in the interconnect. Earlier works take one of the following approaches:

1. The source gate is modeled simply with a linear output resistance. Delay through the loaded source gate ($T_{AB}(L)$) is approximated by computing the Elmore delay to point B [2]-[4]. However, this is just the model source gate output resistance times the total load net capacitance to ground. Series resistance present in the interconnect does not influence this delay calculation.

2. The source gate is modeled more accurately with a non-linear macromodel. However, the source gate output waveform ($v_B(t)$) is approximated with a macromodel response which is influenced by the driven net only through the net's total capacitance (again, series interconnect resistance is not considered) [5],[6].

2. VOLTAGE-TRANSFER RATIO APPROXIMATIONS

In this section, we review two commonly used approximations for a voltage-transfer ratio in an RC-tree. The approximation which is most widely used today is based on the early work of Elmore [8] and was first developed for RC-tree models of on-chip interconnect in [2]. In situations demanding greater accuracy, a higher-order extension developed by Horowitz [5] has proven useful. Both approximations are influenced by the presence and distribution of series interconnect resistance.

Let $h(t)$, $h_{ELM}(t)$, and $h_{HOR}(t)$ denote respectively: the exact, the Elmore approximate, and the Horowitz approximate unit voltage impulse response at a given load in an RC-tree. Let $H(s)$, $H_{ELM}(s)$, and $H_{HOR}(s)$ denote respectively, at the same load, the Laplace transforms of these impulse responses. The Elmore approximate transfer function has a single pole:

$$H_{ELM}(s) = \frac{1}{1 + s\tau_D}. \tag{2}$$

The Elmore time constant (τ_D) is determined by matching the *first moment* of the exact impulse response:

$$\int_0^\infty t h_{ELM}(t)dt = \int_0^\infty t h(t)dt. \tag{3}$$

The Horowitz approximate transfer function has two poles and one zero:

$$H_{HOR}(s) = \frac{1 + s\tau_z}{(1 + s\tau_1)(1 + s\tau_2)}. \tag{4}$$

The three parameters in Horowitz's approximation (τ_z, τ_1, and τ_2) are determined by matching the *first two moments* of the exact impulse response and the *"sum of the open-circuit time constants"* (i.e., the coefficient of s in the denominator of the exact transfer function):

$$\int_0^\infty t h_{HOR}(t)dt = \int_0^\infty t h(t)dt \tag{5}$$

$$\int_0^\infty t^2 h_{HOR}(t)dt = \int_0^\infty t^2 h(t)dt \tag{6}$$

$$\frac{1 + b_1 s + b_2 s^2 + \cdots}{1 + (\tau_1 + \tau_2)\, s + a_2 s^2 + \cdots} = H(s). \tag{7}$$

3. DRIVING-POINT ADMITTANCE APPROXIMATIONS

In this section, we present three successively higher-order circuit approximations for the driving-point admittance of a general RC tree (see Fig. 2). Let $Y(s)$ denote the exact driving-point admittance of the RC tree. Within some circle of convergence, we can represent $Y(s)$ by its Taylor series expansion around $s = 0$:

$$Y(s) = \sum_{n=1}^{\infty} y_n s^n. \tag{8}$$

For $1 \le i \le 3$, the circuit approximation $Y_{APPi}(s)$ shown in Fig. 2 matches the expansion (8) to order i.

Let $y(t)$ denote the inverse Laplace transform of $Y(s)$ (i.e., $y(t)$ is the response current into a general RC tree caused by an applied unit voltage impulse). Matching higher-order terms in (8) is mathematically equivalent to matching higher-order *time moments* of $y(t)$ since:

$$y_n = \frac{(-1)^n}{n!} \int_0^\infty t^n y(t)dt. \tag{9}$$

So, the approximations described in this section (for a driving-point admittance) are quite analogous to those described in the previous section (for a voltage-transfer ratio).

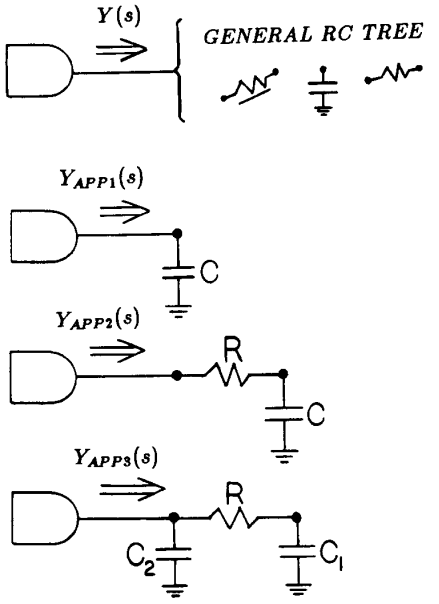

Figure 2: Circuit approximations for the driving-point admittance of a general RC-tree model for an interconnect net.

The approximation $Y_{APP1}(s) = Cs$, where $C = y_1 = C_{LOAD}$ is simply the total load net capacitance to ground, is widely used. In fact, data book descriptions of gates from semiconductor vendors use gate delay as a function of load net capacitance to characterize the drive capability of their cells. However, we show in Section 5 that significant errors can result from ignoring metal resistance.

The RC-lump approximation,

$$Y_{APP2}(s) = \frac{sC}{1 + sRC} = \sum_{n=1}^{\infty} (-1)^{n-1} R^{n-1} C^n s^n, \tag{10}$$

matches (8) to second order by setting:

$$C = y_1 \quad (= C_{LOAD}) \tag{11}$$

$$R = -y_2/y_1^2. \tag{12}$$

The CRC pi-segment approximation,

$$Y_{APP3}(s) = sC_2 + \frac{sC_1}{1 + sRC_1} = (C_1 + C_2)\, s + \sum_{n=2}^{\infty} (-1)^{n-1} R^{n-1} C_1^n s^n, \tag{13}$$

provides even more accuracy by matching (8) to third order:

$$C_1 = y_2^2/y_3 \quad (14)$$

$$C_2 = y_1 - \left(y_2^2/y_3\right) \quad (15)$$

$$R = -y_3^2/y_2^3. \quad (16)$$

Note that $C_1 + C_2 = y_1 = C_{LOAD}$ in the pi-segment approximation.

We have found that either second- or third-order matching provides sufficient accuracy in all cases of practical interest to us. Though, in principle, arbitrarily high orders of the driving-point admittance could be matched with appropriate lumped circuit models. In this section, it is assumed the necessary series expansion coefficients of $Y(s)$ (i.e., y_1, y_2, and y_3) are known. In Section 4, we present an efficient algorithm for computing these coefficients.

4. ALGORITHM FOR SERIES COEFFICIENTS

In this section, we present our algorithm for computing (the first three) Taylor series expansion coefficients of $Y(s)$ which are needed to perform the matching to a lumped circuit approximation described in Section 3. The algorithm starts at the leaf nodes of an RC tree and works back to the source in a finite sequence of steps.

The algorithm consists of four rules which allow the Taylor series expansion coefficients of the driving-point admittance *looking downstream of a given point in the tree* to be correctly propagated further upstream (see Fig. 3). Rules #1–3 involve movement upstream, along a single branch, past respectively: a lumped capacitor to ground, a series lumped resistor, and a uniform distributed RC segment. Rule #4 involves combining two or more different admittance expansions in parallel at a branch point in the tree.

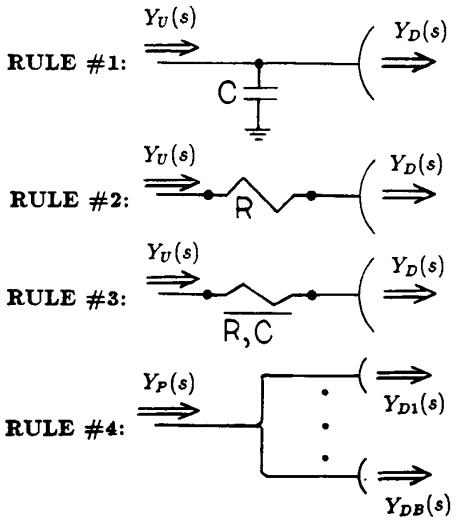

Figure 3: Four rules for upstream propagation of driving-point admittance expansion coefficients.

For rules #1–3, denote the known admittance expansion (looking downstream from the point which is immediately *downstream* of the circuit element to be traversed) by:

$$Y_D(s) = \sum_{n=1}^{3} (y_D)_n s^n + o\left(s^4\right). \quad (17)$$

Denote the unknown admittance expansion (looking downstream from the point which is immediately *upstream* of the circuit element to be traversed) by:

$$Y_U(s) = \sum_{n=1}^{3} (y_U)_n s^n + o\left(s^4\right). \quad (18)$$

Rule #1 states that for upstream traversal of a lumped capacitor (C) to ground:

$$(y_U)_1 = (y_D)_1 + C \quad (19)$$

$$(y_U)_2 = (y_D)_2 \quad (20)$$

$$(y_U)_3 = (y_D)_3. \quad (21)$$

Rule #2 states that for upstream traversal of a series lumped resistor (R):

$$(y_U)_1 = (y_D)_1 \quad (22)$$

$$(y_U)_2 = (y_D)_2 - R(y_D)_1^2 \quad (23)$$

$$(y_U)_3 = (y_D)_3 - 2R(y_D)_1(y_D)_2 + R^2(y_D)_1^3. \quad (24)$$

Rule #3 states that for upstream traversal of a uniform distributed RC segment (total capacitance C, and total resistance R):

$$(y_U)_1 = (y_D)_1 + C \quad (25)$$

$$(y_U)_2 = (y_D)_2 - R\left[(y_D)_1^2 + C(y_D)_1 + \frac{1}{3}C^2\right] \quad (26)$$

$$(y_U)_3 = (y_D)_3 - R\left[2(y_D)_1(y_D)_2 + C(y_D)_2\right] + R^2\left[(y_D)_1^3 + \frac{4}{3}C(y_D)_1^2 + \frac{2}{3}C^2(y_D)_1 + \frac{2}{15}C^3\right]. \quad (27)$$

For rule #4, let B (≥ 2) denote the number of branches to be combined in parallel. Denote the B known downstream admittance expansions by:

$$Y_{Di}(s) = \sum_{n=1}^{3} (y_{Di})_n s^n + o\left(s^4\right); \quad 1 \leq i \leq B. \quad (28)$$

Denote the admittance expansion of the parallel combination by:

$$Y_P(s) = \sum_{n=1}^{3} (y_P)_n s^n + o\left(s^4\right). \quad (29)$$

Parallel admittances simply add together, and so do corresponding terms of their Taylor series expansions. Hence, rule #4 states:

$$(y_P)_1 = \sum_{i=1}^{B} (y_{Di})_1 \quad (30)$$

$$(y_P)_2 = \sum_{i=1}^{B} (y_{Di})_2 \quad (31)$$

$$(y_P)_3 = \sum_{i=1}^{B} (y_{Di})_3. \quad (32)$$

5. RESULTS

To conclude, we show plots of driver delay versus metal loading. The metal loading we consider is an unbranched uniform distributed RC segment, which has a driving-point admittance of precisely:

$$Y(s) = \sqrt{\frac{sC_{LOAD}}{R_{LOAD}}} \tanh\left(\sqrt{sC_{LOAD}R_{LOAD}}\right), \qquad (33)$$

where C_{LOAD} is the total capacitance and R_{LOAD} is the total series resistance of the segment.

The first-order (purely capacitive) approximation is $C = C_{LOAD}$, which ignores resistance in the metal load. The second-order (RC-lump) approximation works out to be:

$$C = C_{LOAD} \qquad (34)$$

$$R = \frac{1}{3}R_{LOAD}. \qquad (35)$$

The third-order (pi-segment) approximation works out to be:

$$C_1 = \frac{5}{6}C_{LOAD} \qquad (36)$$

$$C_2 = \frac{1}{6}C_{LOAD} \qquad (37)$$

$$R = \frac{12}{25}R_{LOAD}. \qquad (38)$$

We compare the driver delay using each of these approximate loads to driver delay using the fully distributed load.

The driver we use is an ECL differential clock buffer. The two differential outputs are each loaded identically (by (33), or by one of its reduced-order lumped circuit approximations). Gate delay is measured as the crossing time of the signals at the buffer input to the crossing time at the buffer output. Gate delay (T_{AB}) is normalized to unloaded gate delay ($T_{AB}(0)$). Total metal capacitance (C_{LOAD}) is normalized to the maximum allowable load capacitance (C_{MAX}), given the sizing of our clock buffer.

To illustrate the importance of metal *resistance*, we use two different metal widths: a high-resistance "narrow" metal, and a low-resistance "wide" metal. Physically, wide metal is twice the width of narrow metal. For a given total metal capacitance, the total series resistance of a narrow metal segment is 3.2 times that of a wide segment (not the ideal factor of 4, because of a fringing-field capacitance component). As can be seen in Figs. 4 and 5, progressively longer metal lengths require progressively higher-order lumped circuit approximations to accurately model the "resistive shielding" of capacitance which is located far away from the driver.

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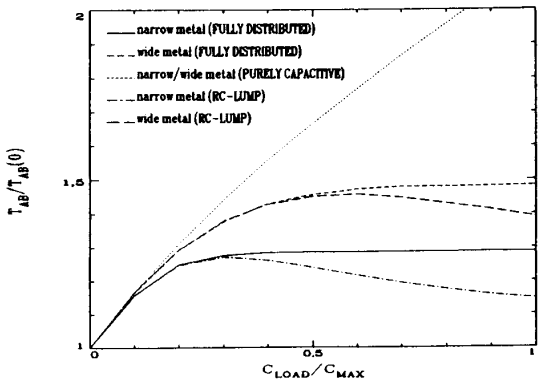

Figure 4: Comparisons for $Y_{APP1}(s)$ and $Y_{APP2}(s)$.

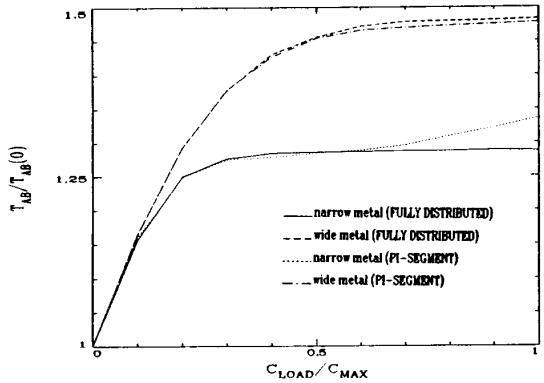

Figure 5: Comparison for $Y_{APP3}(s)$.