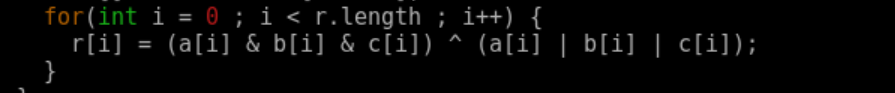
**Ternary Logic Optimization**

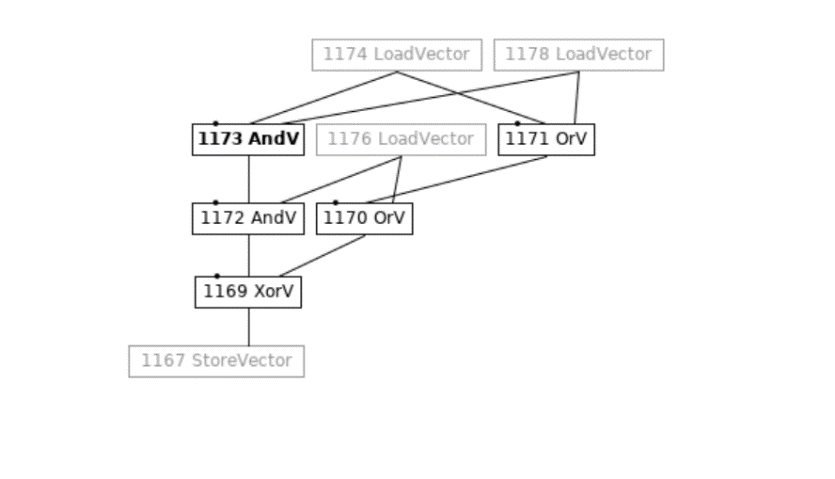
Algorithm:

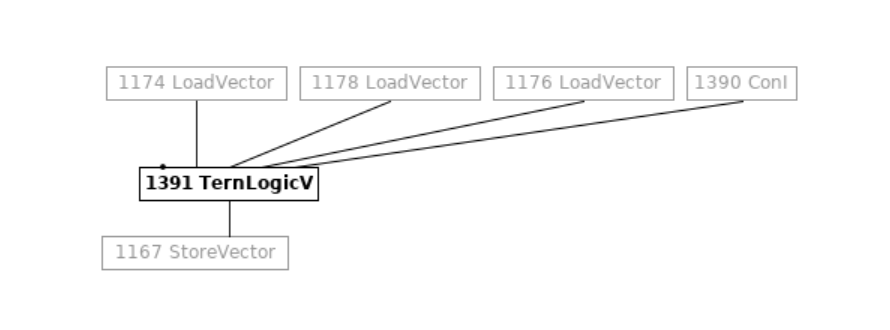
1. Bottom up traversal over logic expression cones constrained by number of inputs. Multi-driving logic nodes prevents folding.

Features : AVX512F [AVX512VL] : VPTERNLOGD/VPTERNLOGQ

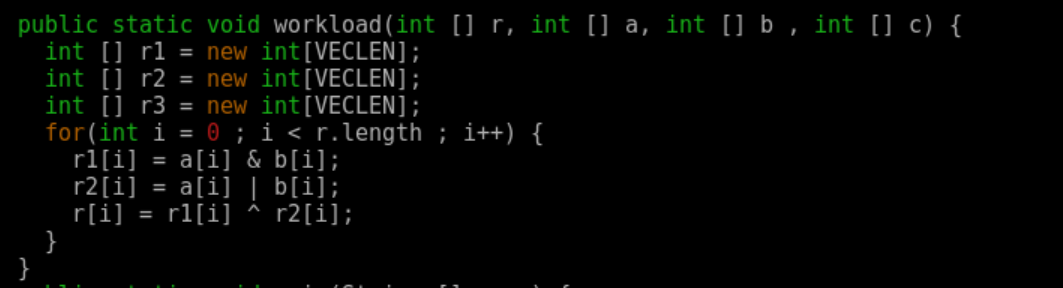
1. Non-dependent logical expressions folding:

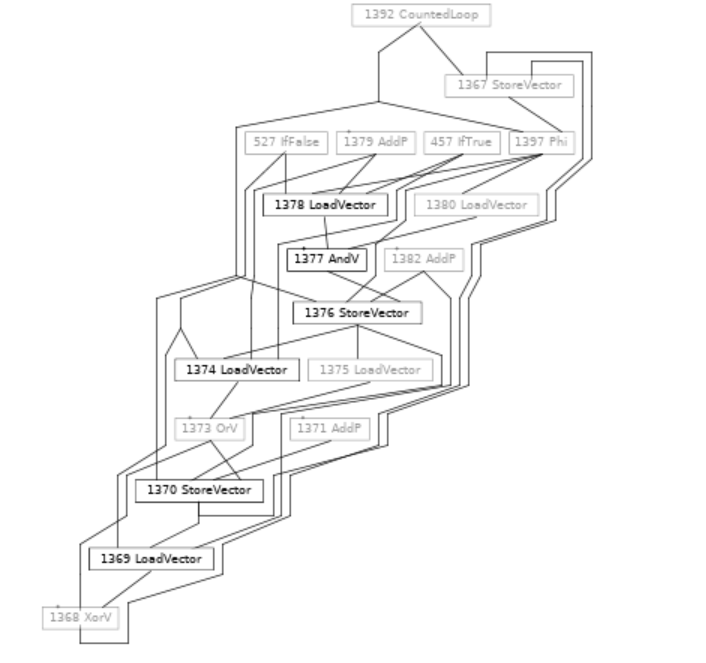


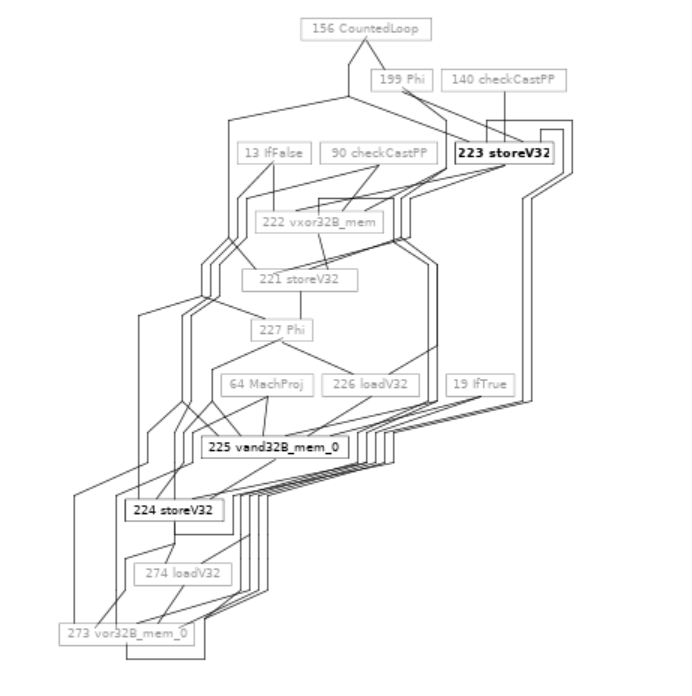


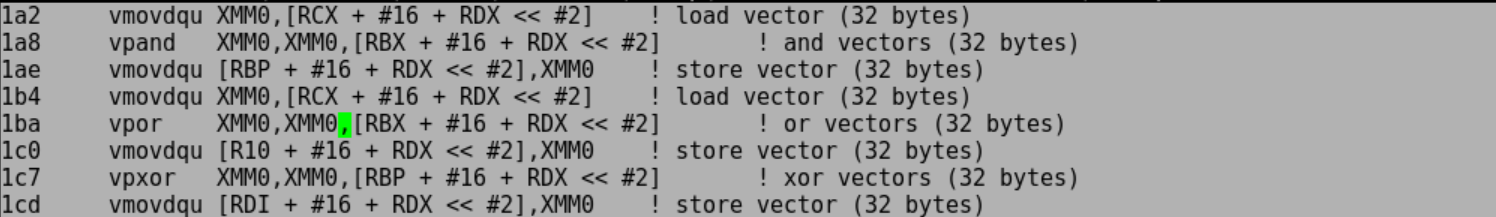


1. Depedent logical expression folding: Redundant StoreVector increses the driver count of the logic expression node which prevents folding.

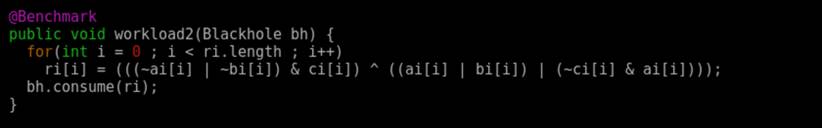




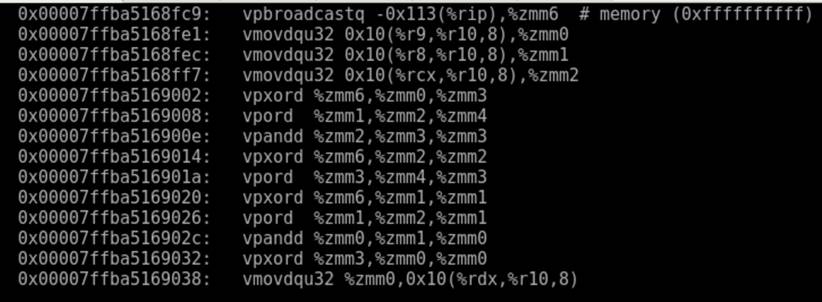




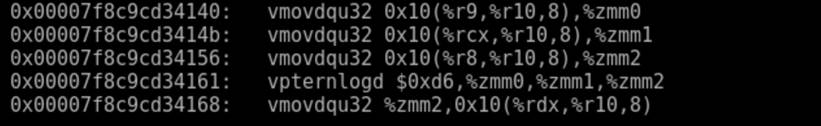
Performance analysis



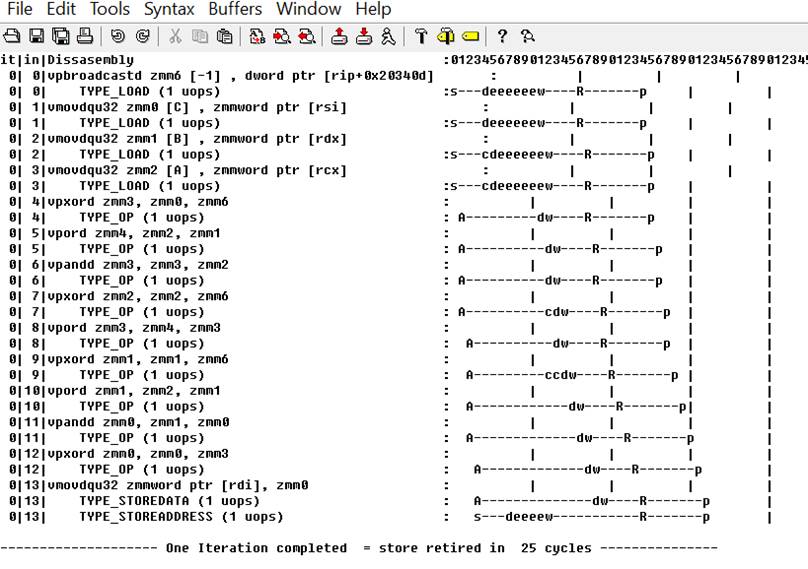
**Original C2 JIT assembly sequence:**



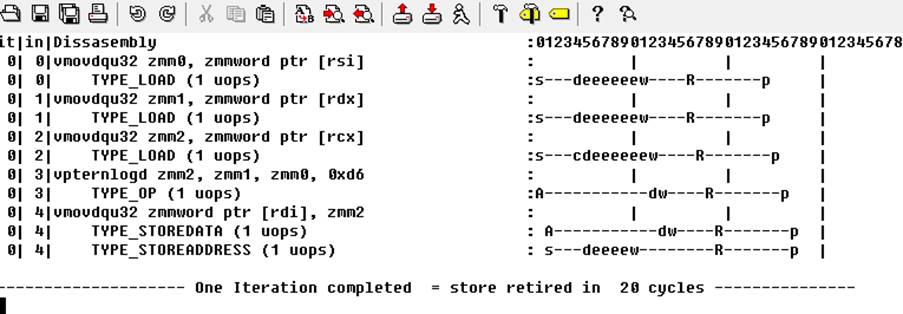
**New C2 JIT assembly sequence:**



**Detailed micro-architectural analysis using  IACA (original code)**



**Detailed micro-architectural analysis using  IACA (new code)**



**5 cycles gain per iteration with vpternlogd**

**IACA based analysis does not take into consideration dynamic conditions like TLB/Cache misses**

**which play a significant role in overall performance numbers.**

**Results of perf runs (10 iterations) over original and new asm sequence generated by C2.**

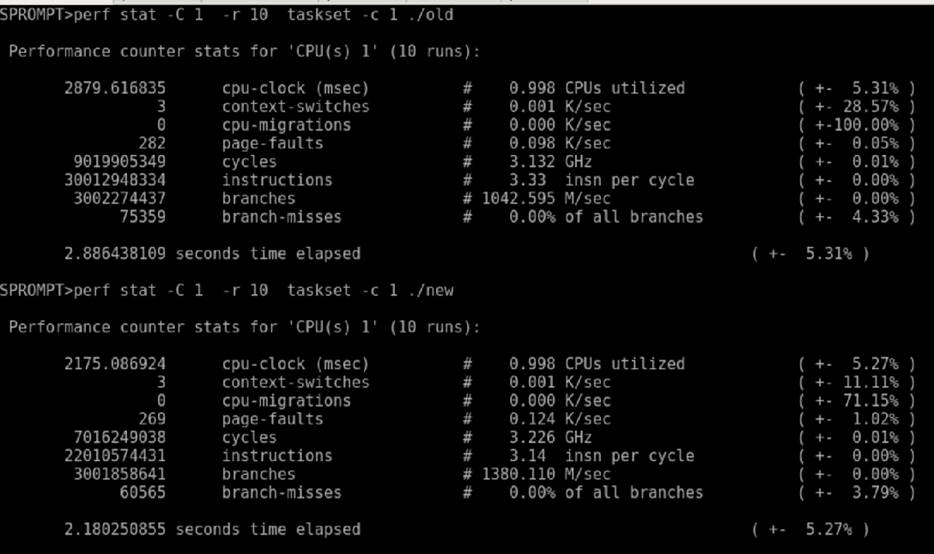
**Data collected by extracting C2 generated sequence and running it though standalone**

**C application using embedded assembly (inline asm).**

**Platform: SKX**

**New application : with vpternlogd**

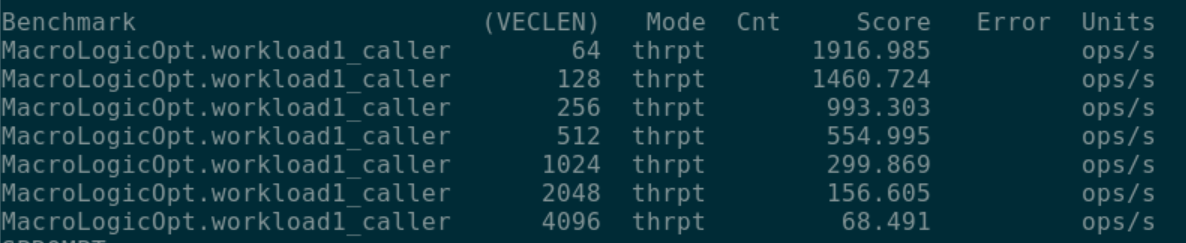
**Old application : with AVX512 logic operations**



It is roughly showing similar gain (~1.25x) as claimed by the Inter Optimization Manual section 17.7 Example 17-11.

Following are JMH scores which does significant performance difference specially for higher vector lengths :

Old Scores



New Scores:

