



Jatin Gupta

Bachelor of Technology
in Computer Science Engineering
Indian Institute Of Technology, Ropar

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EDUCATION

Degree	Institute/Board	CGPA/Percentage	Year
Bachelor of Technology	Indian Institute of Technology, Ropar	7.52 (Till 5th Sem)	2020-2024
Senior Secondary	Central Board of Secondary Education	93%	2020
Secondary	Central Board of Secondary Education	86%	2018

PROJECTS

- Railway Reservation System** November 2022 - December 2022
Database management system **Github**
 - This Project Facilitates passengers to book tickets, Passengers has to provide train number and date of journey for which the ticket is to be booked
 - Through concurrency control protocols, it can manage simultaneous access from multiple users to the database system.
 - PostgreSQL is used as the primary data warehouse for this project, Front-end Part is designed using Java.
- Dynamic-Graph-Connectivity** Nov 2022 - Dec 2022
Algorithm Design **Github**
 - The project aims to Find connectivity in Fully Dynamic Graph in PolyLogarithmic Time per Operation.
 - The implementation is based upon the **research paper** published by Monika Henzinger and Valerie King.
 - It outputs Whether two nodes are connected or not, User can add or delete edges whereas number of nodes would be fixed.
- Implementation of Utility-Based Cache Partitioning** April 2022 - May 2022
Computer Architecture **Github**
 - The goal of this project is to implement Utility Cache based partitioning (UCP) in Champsim, a trace-based microarchitecture simulator using C++ language.
 - In Multicore Processors, the lowest level cache is shared by all cores, So instead of static partitioning Using utility-based partitioning, allocated dynamic cache memory to different cores to Minimise Miss count.
- Syntax Checker For C Language** Mar 2022 - Apr 2022
Deepti R. Bathula **Github**
 - This Toy Compiler Performs Lexical Analysis and Syntax Analysis for given piece of code Using Lex And Yacc.
 - The code was tokenised using Lex, and the tokens were parsed using Yacc.
- Smart Car Parking System using Verilog** Oct 2021 - Nov 2021
Digital Logic Design **Github**
 - The Main Objective of This Project is to automate parking System implemented Using Finite-state machine in verilog HDL.
 - This project ensures the safety of Parked cars and prevents collisions between entering a car and exiting cars.
- Web Projects** June 2021 - Aug 2021
Personal **Github**
 - Youtube **Clone** developed Using React And React Libraries. Data is fetched from Youtube API.
 - Responsive Portfolio **Website** developed Using HTML, CSS, JS

TECHNICAL SKILLS

- Programming Languages:** C/C++, Javascript, Python, Java, Perl
- Front-End Web Technologies:** HTML5, CSS, Bootstrap, React
- Libraries/ frameworks/ OS:** Matplotlib, Numpy, Pandas, Linux, git, Tinkercad, Latex

KEY COURSES TAKEN

- CSE:** Algorithm & Data Structure, Computer Architecture, Programming Paradigms, Digital Logic Design
- Maths:** Discrete Mathematics, Probability and Statistics, Advanced Calculus and Linear Algebra
- Others:** Economics, Signals and Systems, Basic Electronics , Tinkering Lab

POSITIONS OF RESPONSIBILITY

- Team Member, Event Management Team**, Zeitgeist, IIT Ropar Apr. 2021 - May 2021
- Team Member, Publicity Team**, Advitiya, IIT Ropar Apr. 2021 - May 2021
- JEE Mentor**, S.H.V.M School Dec. 2020 - June 2021

ACHIEVEMENTS / CERTIFICATES

- Qualified JEE Advanced 2020**, Among top 1% 2020
- Qualified JEE Mains 2020**, Among top 1% 2020
- Competitive Programming**, Global Rank 168 CodeChef Starters 31 Division 2 Codechef
- Complete JAVASCRIPT with HTML5, CSS3 from zero to Expert-2022**, Completed Udemy Course Udemy
- Intro to React: Build a Youtube App 2021**, Completed Udemy Course Udemy
- Master C++ Programming From Beginner To Advance**, Completed Udemy Course Udemy