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Electronics Engg.
Part III
EC331 Assignment

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Q. To develop the process parameters required to form a MOSFET transistor.

The formation of a MOSFET transistor consists of the following steps:

CMOS transistors are fabricated on silicon wafers using a process similar to lithography processes in printing presses.

On each step, different materials are deposited or etched.

First, we will start with blank wafer and build the inverter from the bottom up

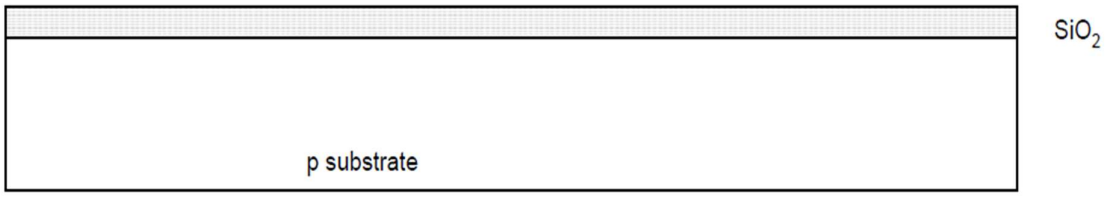
In the first step we will form the n-well and cover wafer with protective layer of SiO2

We will then remove the layer where n-well should be built and implant or diffuse n-type dopants into exposed wafer

We will then strip off SiO2.

Step 1. Oxidation.

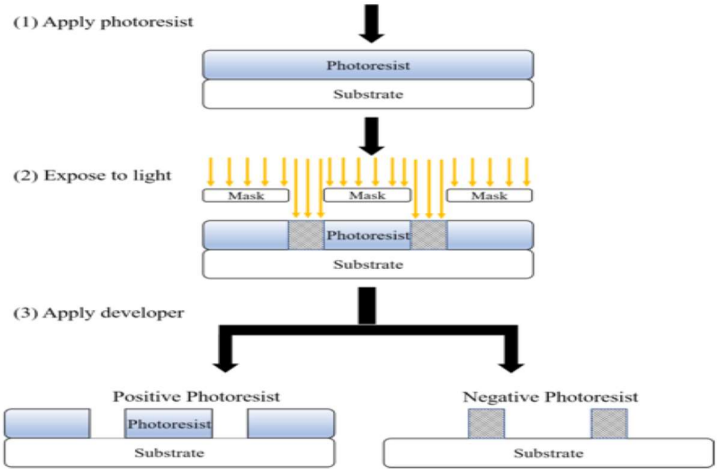
We grow SiO2 on top of Si wafer. The oxidation is done at a temperature of 900-1200 degree Celsius with water and oxygen in an oxidation furnace.



Step II. Photoresist.

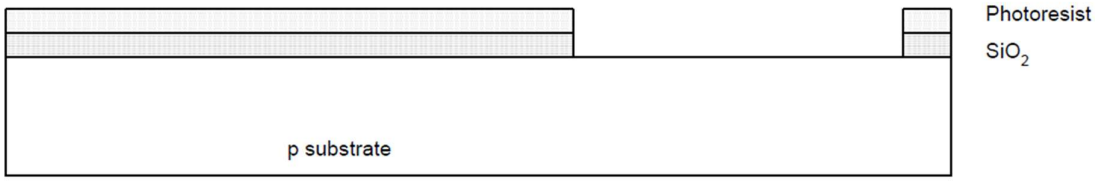
We then apply the photoresist, which is a light-sensitive organic polymer which softens when exposed to light.

It is then exposed to light to strip off the photoresist where n-well is to be applied.



Step III. Etching.

We then etch the exposed oxide layer with hydrofluoric acid.



We then strip off the remaining oxide using HF and are back to bare wafer with n-well

Step IV. Polysilicon

Then a thin layer of oxide is deposited.

The oxidation is done at a temperature of 900-1200 degree Celsius with water and oxygen in an oxidation furnace.

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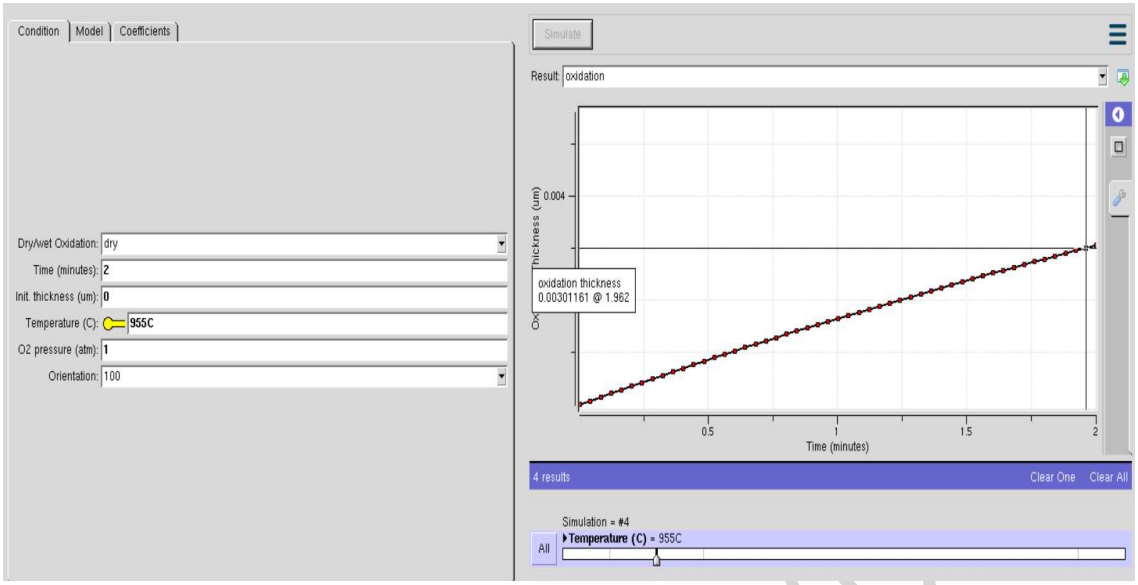
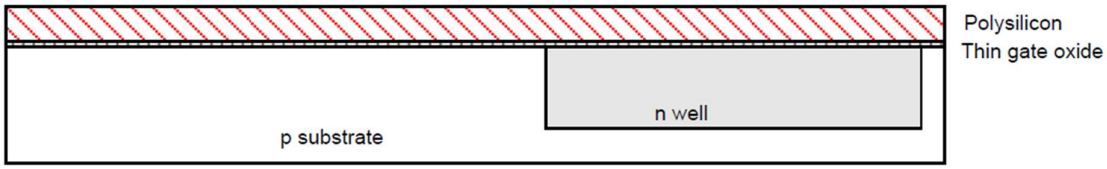


To develop a oxide layer 3nm thick, we use dry oxidation at a temperature of 955 degree Celsius and at a oxygen pressure of 1 atm for 120 seconds. Further, we use 100 (miller indices) orientation.



Dry oxidation is used in comparison to wet oxidation because it has high density and has less defects.

This is followed by Chemical Vapor Deposition (CVD) of silicon layer. We place wafer in furnace with Silane gas (SiH4), which forms many small crystals called polysilicon

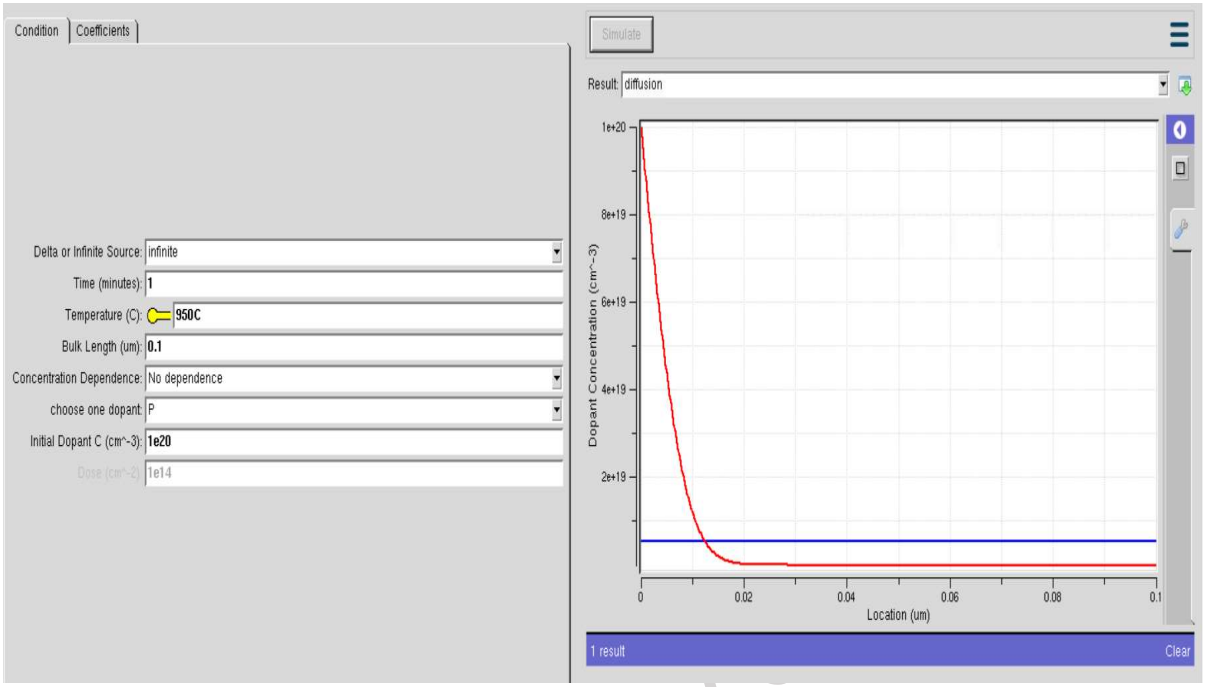
Polysilicon is heavily doped silicon to make it a good conductor.

Step V. N-diffusion

We pattern oxide and form n+ regions.

We use infinite source diffusion at 950 degree Celsius with a bulk length of 0.1um and initial dopant concentration of 1e20 per cubic centimetre. The diffusion process is carried out for 60 seconds.

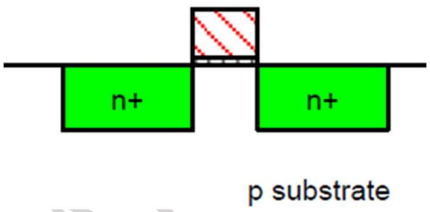
The results are plotted.



It is a Self-aligned process where gate blocks diffusion.

Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing.

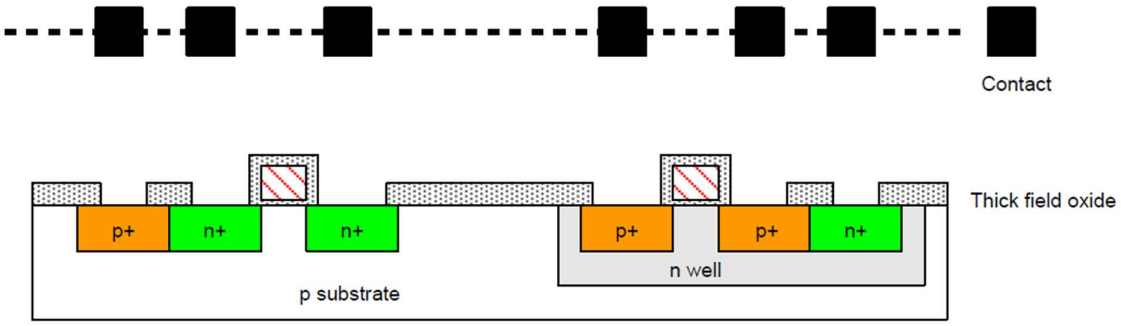
The oxide is stripped off to complete patterning step.



Similar set of steps are followed to form p+ diffusion regions for PMOS source and drain and substrate contact.

Step VI. Metallization

Now we need to wire together the devices. We cover chip with thick field oxide and etch the oxide where contact cuts are needed.



We then sputter aluminium over the whole wafer and remove excess metal to form wires.

This forms our final MOSFET transistor.

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