INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Department of Computer Sc & Engg

Computer Organisation and Architecture (CS31001)

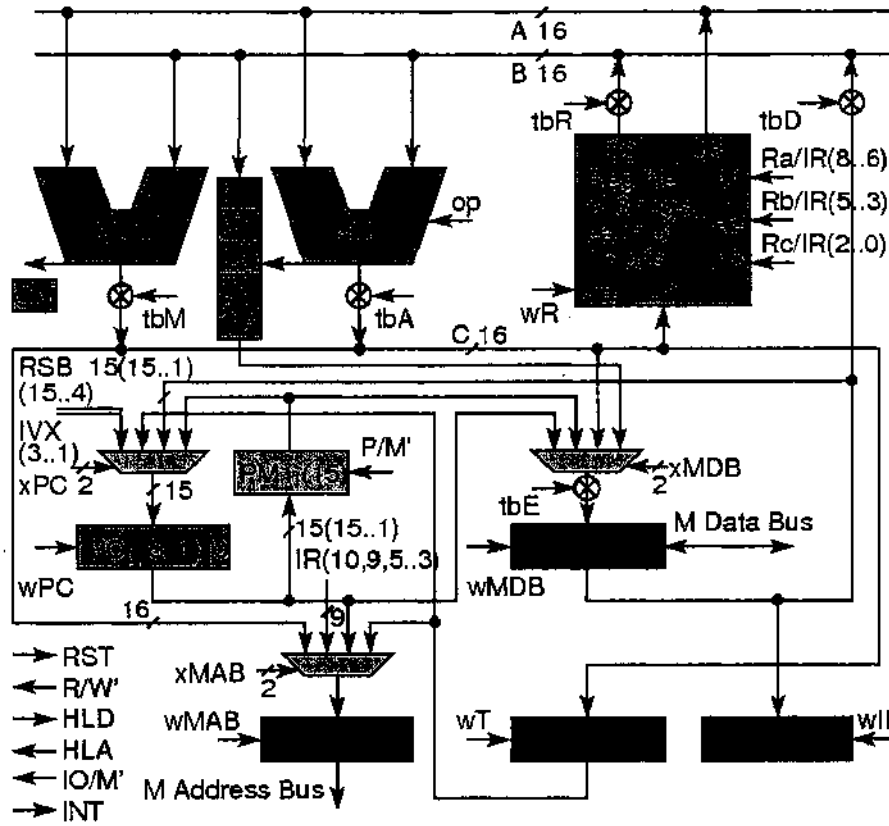
Mid-semester (Autumn)

Place: F-116 *Date:* Mon, Sep 13, 2010 *Time:* 2-4pm (AN), 2 hours

Students: 76 *Marks:* 110

Answer ALL the questions

1. Consider the CPU in the given figure. If you need to make minor assumptions then state them clearly while answering.



(a) List the micro-operations along with necessary assertions of control signals, wrt the given data path, to fetch an instruction. 2+5

(b) The `STM R M` instruction, for storing the contents of register **R** at the memory location **M**, consists of the main instruction word followed by a 16-bit address.

List the micro-operations along with necessary assertions of control signals, wrt the given data path, to realise this instruction, beyond instruction fetch. 3+6

(c) The **HLT** instruction for suspending instruction execution and waiting for an interrupt. `PM1 (15)` in the data path is a 15-bit incrementer/decrementer.

List the micro-operations along with necessary assertions of control signals, wrt the given data path, to realise this instruction, beyond instruction fetch. 3+6

(d) The `RTI` instruction causes a return from interrupt (service routine) and resumption of the program from where it was interrupted.

List the micro-operations along with necessary assertions of control signals, wrt the given data path, to realise this instruction, beyond instruction fetch. 3+7

2. *Answer this question for* **5 marks** *only.*

   (a) With the help of a diagram describe design of a CPU controller based on the state-table method. 5

   (b) With the help of a diagram describe design of a CPU controller based on the delay-element method. 5

3. A CPU uses memory addresses of 32 bits. Its main memory is made up of several memory modules. Each main memory module can store 2 Mi bytes (1Mi = 2^{20}) and has a chip select (CS) pin (module enabled if CS=1, memory data port tristated if CS=0). Main memory word size is of 2 bytes (data port has 16 bits). Each lines of the cache is divided into 4 slots of 4 bytes each. Describe with the help of a labelled diagram, the interleaved organisation of the main memory (using the main memory modules) so that transfer between the main memory and the cache happens in the unit of a complete cache line. 20

4. A direct mapped cache consists of 64 lines of 16 words per line. Both the word size and the memory address width of the CPU are of 32 bits.

   (a) Describe with the help of a labelled diagram the organisation of the cache and how main memory addresses are mapped to cache locations. 15

   (b) Compute the hit ratio for a program that starts from memory address location 0 and runs to location 200 and then loops 10 times from locations 200..256. 15

   (c) The hit time for a cache access is 10 ns, and the miss time is 200 ns, which includes the time to transfer the missed line from the main memory to the cache. Compute the effective memory access time for the described run of the above program. 5

5. A set associative cache is required to implement the LRU scheme for cache line replacement. To simplify the design each set is kept only two way associative. Design the (circuit level) mechanism to effect LRU replacement withing each (fully associative) set. 15