Extra

Indian Institute of Technology Kharagpur

AUTUMN Semester, 2018
COMPUTER SCIENCE AND ENGINEERING

CS31007: Computer Organization and Architecture

Mid-semester Examination

Full Marks: 60

Time allowed: 2 hours

INSTRUCTIONS: This exam is closed notes and closed books. This question paper has two pages. Use of calculators is allowed. ATTEMPT ALL QUESTIONS.

1. (a) Consider the following C function that calculates and returns the Greatest Common Divisor (GCD) of two positive integers a and b by repeated subtraction (a is implicitly assumed to be greater than b when the function is called for the first time):

```
int gcd (int a, int b)
{
   int temp;
   while (1) {
    while ((temp = a - b) > 0) a = temp;
    if (!temp) return b;
    temp = a; a = b; b = temp;
   }
}
```

Write a MIPS-32 procedure gcd corresponding tc the above algorithm. The gcd procedure makes the result available in register $v0. Assume variable a is mapped to register $a0 and variable b is mapped to register $a1 when the procedure is called. (8 marks)

(b) Draw a simple schematic diagram of the overall architecture of a hardware implementation of the above algorithm to calculate the GCD of two N-bit positive integers, and then write the complete Verilog description of the circuit. Your Verilog description should correspond to the architecture you have drawn, and should clearly differentiate the datapath and controlpath into separate modules. Clearly mention the role of the control signals you choose. **Your design should not use bulky hardware units like dividers or magnitude comparators.** (10 marks)

(c) Explain why modern processor design focus on increasing the number of cores on a single chip, instead of just increasing the processor clock frequency. (2 marks)

(d) Suppose that we can improve the floating point instruction performance of machine by a factor of 15 (the same floating point instructions run 15 times faster on this new machine). What percent of the instructions must be floating point to achieve an overall speedup of at least 4? (2 marks)

(e) Explain the different addressing modes supported by the MIPS-32 instruction set architecture, with neat schematic diagrams. Your answer should include on complete MIPS-32 instruction as example, for each addressing mode. (8 marks)

Consider unsigned integer multiplication with k-bit multiplier $X = x_{k-1}x_{k-2}\cdots x_1x_0$ and k-bit multiplicand $A = a_{k-1}a_{k-2}\cdots a_1a_0$. Traditional schoolbook multiplication teaches us to add left-shifted partial products (of the form $x_i \cdot A \cdot 2^i$) to get the final $2k$-bit product: $P = A \cdot X = \sum_{i=0}^{k-1} x_i \cdot A \cdot 2^i$. An easier alternative is not to left shift the partial products, but to shift the cumulative partial product P_j by one bit at every step to align it with the next partial product. Two versions of this algorithm can be devised:

- **Scheme-1:** in "multiplication by right shifts", the cumulative partial product after the j-th iteration is given by:
  $P_{j+1} = \left(P_j + x_j \cdot A \cdot 2^k\right) 2^{-1}$, with $P_0 = 0$. This scheme is used in *Booth's Multiplication Algorithm.*
- **Scheme-2:** in "multiplication by left shifts", the cumulative partial product after the j-th iteration is given by:
  $P_{j+1} = 2 \cdot P_j + x_{k-j-1} \cdot A$, with $P_0 = 0$.

Prove that for both these schemes $P_k = P = A \cdot X$. (4 marks)

Perform the following multiplication using *Booth's Multiplication Algorithm*: $(-97) \times 41 = -3977$. Show all intermediate steps clearly. (6 marks)

Explain in detail "write-back-with-write-allocate" and "write-back-with-no-write-allocate" schemes for cache memory in modern processors, with flow diagrams for each. (6 marks)

A processor has 32 byte main memory and an 8 byte direct-mapped cache. Table-1 shows the initial state of the cache: Show the evolution of the cache contents for the following memory address access

Table 1: Initial State of Cache

Index	V	Tag	Data
000	N		
001	Y	00	Mem[00001]
010	N		
011	Y	11	Mem[11011]
100	Y	10	Mem[10100]
101	Y	01	Mem[01101]
110	Y	00	Mem[10000]
111	N		

sequence, and mention Hit/Miss in each case:

11100 10001 00110 00010 11110 11011 00000 00111 10000

(8 marks)

Consider a magnetic hard disk with the following parameters: Average seek time 12 ms; Rotation rate 3600 RPM; Transfer rate 3.5 MB/second; number of sectors per track 64; Sector size 512 bytes; Controller overhead 5.5 ms. Calculate: (a) the average time to read a single sector, and, (b) the average time to read 8 KB in 16 consecutive sectors in the same cylinder. (4 marks)

Now suppose for the we have an array of four of the above-mentioned hard disks. They are all synchronized such that the arms on all the disks are always on the same sector within the track. The data is striped across the 4 disks so that 4 logically consecutive sectors can be read in parallel. Calculate the average time to read 32 kB of contiguous data from the disk array. (2 marks)