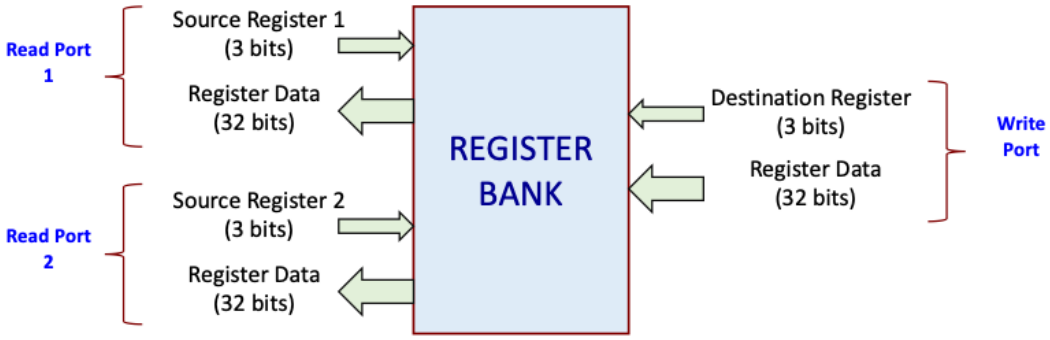
Verilog Assignment 5

Design a register bank and interface it with a 32-bit K-ALU.

a) Design a register bank in Verilog that contains eight registers R0, R1, …, R7, each of size 32-bits. The register R0 is read-only and always contains the value 0.

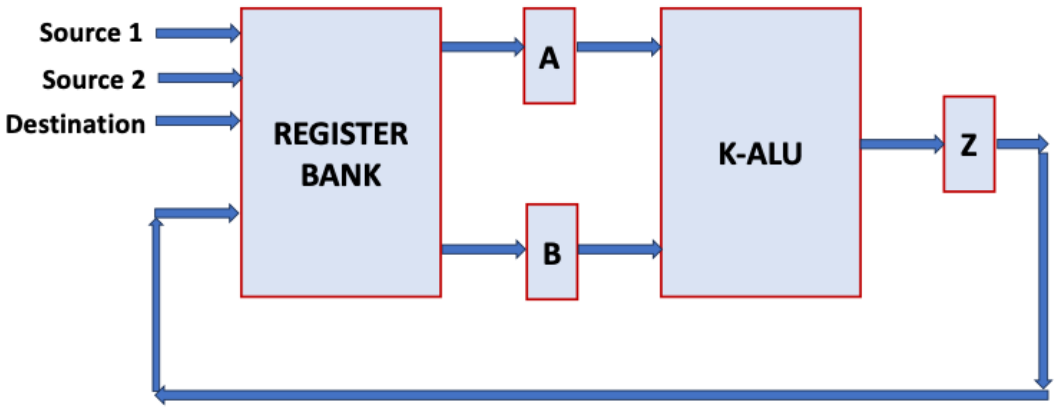
The register bank will have two read ports as shown below, where the contents of two registers can be read in the same clock cycle. Also, the register will have one write port. Assume that register write takes place at the positive edge of the clock, and register reads take place at the negative edge of the clock.



b) Extend the K-ALU design to handle 32-bit data, with the following guidelines.

Continue the modeling of multiplication and division in behavioral form. Do not implement the HAM functionality of the K-ALU; leave the corresponding function select combination unused.

Interface the register bank with the K-ALU, as follows.



c) Design a control path that takes a 3-bit input (c2, c1, c0), and performs the following operations:

c2	c1	c0	Function
0	0	0	R1 = R2 + R3
0	0	1	R4 = R1 – R5
0	1	0	R2 = R1 << R2
0	1	1	R7 = R1 >> R2
1	0	0	R6 = R1 * R2
1	0	1	R1 = R1 AND R2
1	1	0	R3 = R2
1	1	1	R6 = 0

Write a Verilog test bench to initialize the registers with some initial values, and test the functionalities.