PRACTICE PROBLEMS ON COMPUTER ARITHMETIC

1. Suppose that a full adder is implemented using AND, OR and NOT gates only, with the AND-OR circuits in 2-level realization. The delay of an n-input AND gate is 5n nanoseconds, delay of an n-input OR gate is (5n+ 2) nanoseconds, and the delay of a NOT gate is 3 nanoseconds. What will be the worst-case propagation delay to generate the sum and carry outputs? Show the steps of your calculation.
2. What will be the worst-case propagation delay of a 16-bit ripple-carry adder using full adders as specified in Q1.
3. Repeat Q2 for a 4-bit carry lookahead adder.
4. Represent−75 in (i) 8-bit 2's complement form, (ii) 64-bit 2's complement form. Suppose the above 64-bit number is shifted right by 3 positions, with the sign bit replicated during the shifting process. What will be the value of the number after shifting?
5. Suppose you have designed a 4-bit adder that adds two 2's complement numbers (A3,A2,A1,A0) and (B3,B2,B1,B0), to generate the sum (S3,S2,S1,S0) and the final carry Cout. Show gate-level circuit diagrams to generate the following: (i) Overflow flag (1 if overflow, 0 if not), (ii) Parity flag (1 if parity odd, 0 if even).
6. Design an optimized 12-bit carry select adder using (i) uniform sized adders, (ii) variable sized adders as basic building blocks.
7. Design an optimized 24-bit carry select adder using (i) uniform sized adders, (ii) variable sized adders as basic building blocks.
8. Show the schematic diagram for adding 12 16-bit numbers using carry save adders.
9. Estimate the worst-case propagation delay of a 4-bit combinational array multiplier, assuming that the delay of a basic gate (AND, OR, NOT) is T.
10. Using 6-bit number representation, multiply the unsigned numbers 45 and 38 using shift-and-add multiplication technique. Show all steps of the computation.
11. Using 6-bit number representation, multiply the numbers -19 and -17 using Booth's multiplication technique. Show all steps of the computation.
12. Explain how the bit pair recoding technique can reduce the worst-case time required for multiplication using Booth's algorithm.
13. For 5-bit number representations, carry out the division operation 29 / 12 using (i) restoring division algorithm, (ii) non-restoring division algorithm.
14. Consider a 48-bit floating-point number representation with 36-bit mantissa and 12-bit exponent. Estimate the number of significant digits that can be represented, and also the precision of the numbers. Make relevant assumptions as necessary.
15. Decode the following single-precision floating-point numbers. Assume that the numbers are represented in IEEE-754 format.
    a) 0011 1111 1000 0000 0000 0000 0000 0000
    b) 0100 0000 0110 0000 0000 0000 0000 0000
    c) 0100 1111 1101 0000 0000 0000 0000 0000
    d) 1000 0000 0000 0000 0000 0000 0000 0000
    e) 0111 1111 1000 0000 0000 0000 0000 0000
    f) 0111 1111 1101 0101 0101 0101 0101 0101