INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Mid-Autumn Semester Examination 2023-24

Date of Examination: **Session: (FN/AN)** **Duration: 2 Hrs** **Full Marks:60**

Subject No. : CS31007 **Subject : Computer Organization and Architecture**

Department: Computer Science and Engineering

Answer all the questions

All parts of a question must be answered together

1. Answer the following questions. **[5+5+(1+2)+2=15]**

a) In a processor, the instruction type, frequency of usage, and clock cycles required to execute are summarized as follows:

Instruction Type	Usage	Clock Cycles
LOAD & STORE	30%	3
Integer ALU Instruction	40%	2
Branch	20%	3
Floating-point add/subtract	10%	6

In a modification to the processor that also includes enhancements to the instruction set, the following changes are made: (i) the floating-point operations take 4 clock cycles, (ii) 20% of the integer ALU instructions are eliminated (that is, number of ALU instructions reduces by 20%), (iii) 30% of the ***remaining*** integer ALU instructions take 3 clock cycles while rest remain unchanged.

Compare the relative performances of the two versions of the processor.

b) Consider a stack-based computer architecture that has four unary operations **ADD**, **SUB**, **MUL** and **DIV**, each of which pops out two operands from the processor stack, operates on them, and pushes the result back into the stack. In addition, there is an instruction **PUSH X**, which pushes the contents of memory location **X** into the stack, and an instruction **POP X**, which pops an operand from the stack and stores it in memory location **X**.

Write a program in assembly language of the machine to evaluate the following expression:

```
RES = (A * (B - C)) + (D / (E + F))
```

Clearly state any assumptions you make.

c) State the main difference between the von-Neumann and Harvard architectures. How can the Harvard architecture prove to be beneficial when instructions are executed in a pipeline?

d) Explain the difference between ***indirect addressing*** and ***register indirect addressing*** with the help of illustrative examples.

2. Answer the following questions. **[4+4+3+4=15]**

a) For the MIPS32 instruction set architecture, assume that the opcodes for the instructions **SUB** and **LOAD** are **010011** (with the value of the **func** field as **111011**) and **100101** respectively. Show the complete 32-bit encoding of the following instructions:

i) `SUB R26, R11, R5` // R26 = R11 – R5

ii) `LOAD R3, -25(R10)` // R3 = Mem[R10-25]

b) Consider the following switch/case code segment in C, where the switch variable **option** can assume one of the three values in [0,2]:

```
switch (option) {
   case 0:  x = x + 5;  break;
   case 1:  x = x - 3;  break;
   case 2:  y = 8 * y;  break;
}
```

Write down the equivalent code segment in MIPS32 assembly language.

c) Show how you can do the following in MIPS32 assembly language?

i) Load the 32-bit value **2FFF ADAD** (in hexadecimal) in register **R5**.

ii) Branch to a label **Loop1** if **R1 < R2**, and to a label **Loop2** otherwise.

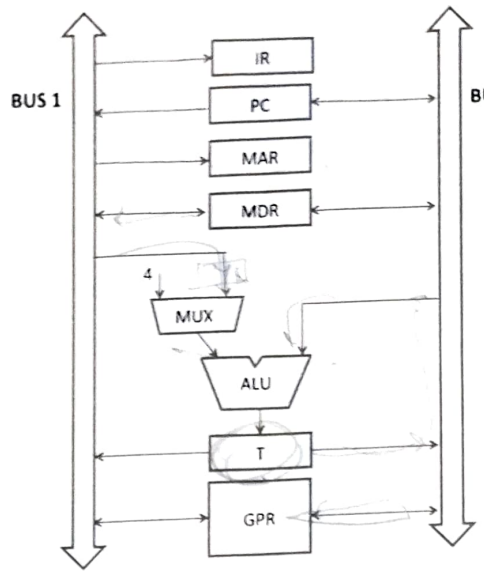
iii) Move the contents of register **R6** to **R8**.

```
lui $t0, 0x2FFF   # Load upper 16 bits (0x2FFF) into $t0
ori $t0, $t0, 0xADAD  # Combine with lower 16 bits (0xADAD)
```

d) Consider a memory system with two levels of cache memory, L1 and L2. Without the cache, memory operations consume 45% of the total execution time. It is experimentally found that the L1-cache speeds up 92% of all memory operations by a factor of 5, while the L2-cache speeds up 60% of the ***remaining*** memory operations by a factor of 2.5. Calculate the overall speedup achieved by using the cache memories ***using Amdahl's law***.

3. Answer the following questions. **[(3+3)+(4+2)+3=15]**

a) Consider the two-bus processor architecture as shown in the diagram. In addition to the standard registers IR, PC, MAR and MDR, there is a register bank containing eight general-purpose registers R0, R1, ..., R7, and a temporary register T. All the registers are 32-bits in size. MAR and MDR are connected to the memory system, which is not shown in the diagram.



Show the control signals along with the time steps for executing the following instructions:

i) **ADD R3,X** // R3 = R3 + Mem[X]

ii) **LOAD R5,X** // R5 = Mem[X]

Make relevant assumptions as needed. If there is any inconsistency in the architecture diagram, correct the same. Clearly state the assumptions you make.

b) With the help of a schematic diagram, briefly explain the concept of microprogrammed control unit design. Briefly explain how branches in microinstruction execution are handled.

c) In the design of the control unit for a processor, there are 150 control signals that can be divided into three groups **G1**, **G2** and **G3**. **G1** contains 35 control signals that can be activated either individually or in parallel. **G2** contains 75 control signals that are mutually exclusive (that is, at most one of them can be active at a time). Similarly, **G3** contains 40 control signals that are also mutually exclusive. Suggest a suitable encoding for the control signals that require the smallest number of bits without sacrificing concurrency.

4. Answer the following questions. **[7+4+4=15]**

a) Draw the schematic diagram to design a 256K x 16 memory system using 64K x 8 memory modules. Clearly show how the different address blocks are mapped to the individual memory modules.

b) Consider a computer system with two-level cache. Suppose that in 2000 memory references there are 100 misses in L1 cache and 20 misses in L2 cache. If the miss penalty of L2 is 100 clock cycles, hit time of L1 is 2 clock cycle, and hit time of L2 is 20 clock cycles, what will be the average memory access time in number of clock cycles?

c) What is memory interleaving? How does it help to improve the processor-memory bandwidth?