Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2024
COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog 1

INSTRUCTIONS: Please answer all the questions.
Special credit would be given for answers which are to-the-point.
Please ensure that your handwriting is legible.
If you prefer to submit printouts of the typed solutions, please typeset your work in LaTeX.

Introduction to Verilog Programming

In this assignment, we shall be designing and comparing two adder circuits using the Verilog Programming Language.

1. *Write the Verilog Code for an n-bit adder. Proceed step by step as follows:*

- *(a) A* Half Adder *is a combinational circuit, which takes in two input bits, a and b, and produces the sum bit, s and the carry-out bit, c. Write the truth-table for the assignments of s and c. Write the verilog code for the* Half Adder.
- *(b) A* Full Adder *is a combinational circuit, which takes in three input bits, a, b, and in addition a carry-in bit c_0, and produces the sum bit, s and the carry-out bit, c. Write the truth-table for the assignments of s and c in the Full-Adder. Write the verilog code for the* Full Adder.
- *(c) Implement two separate designs using behavioral and structural coding styles respectively.*
