PRACTICE PROBLEMS ON MEMORY SYSTEMS

1. A set-associative cache consists of 128 blocks divided into 8-block sets. The main memory contains 8192 blocks, each consisting of 64 words.

   a) The number of bits present in TAG field will be ___9_____.

   b) The number of bits present in SET field will be ___4_____.

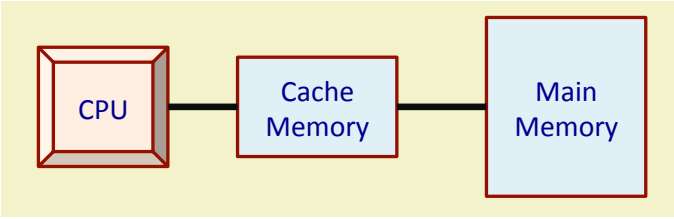
   c) The number of bits present in WORD field will be ___6_____.

2. In a two-level cache system, the hit time of the first-level cache (L1) is 12 nsec and that of the second-level cache (L2) is 30 nsec. If the hit rate of L1 is 95% and that of L2 is 98%, and the miss penalty on the L2 cache miss is 8 nsec, the average memory access time will be __13.508___ nsec.

3. Suppose that in 2000 memory references there are 100 misses in L1 cache and 20 misses in L2 cache. If the miss penalty of L2 is 100 clock cycles, hit time of L1 is 2 clock cycle, and hit time of L2 is 20 clock cycles, the average memory access time will be ____4_____ clock cycles.

4. Consider a 2-level memory hierarchy consisting of a single-level cache memory and the main memory. The access times for the cache memory and main memory are 2 nanoseconds and 20 nanoseconds respectively. Out of 20000 memory accesses, 16500 times the requested word is found in the cache memory. What will be the effective access time of the memory system? Assume that for a cache miss, the block containing the requested data is first brought into cache, and then the data is accessed from cache memory. 5.5

5. Consider a 2-level memory hierarchy consisting of cache memory and main memory as shown below. Assume that the main memory is byte addressable and of capacity 4 Gbyte, with an access time of 120 nanoseconds. The cache memory is of size 4 Mbyte, with an access time of 25 nanoseconds. Whenever there is a cache miss, the block containing the requested word is first transferred from main memory to cache memory, and then the data is accessed from cache.



   a) The value of cache hit ratio (in percentage) to achieve an overall memory access time of 30 nanoseconds will be __95.8_____ %.

   b) Suppose that the cache is split into an instruction cache and a data cache (both at the same level and with same access times), with hit ratios of 98.5% and 87.5% respectively. If 25% of all memory accesses are for data, the overall memory access time will be __30.1_____ nanoseconds.

   c) Consider a direct-mapped cache, with a block size of 2K bytes. Out of the memory addresses 5, 2258, 6149, 8197, 8824, 9709 and 10245 (all expressed in decimal), how many memory addresses will map to cache block B5?

   (Assume that the cache blocks are numbered as B0, B1, B2, B3, …, and $1K = 2^{10}$, $1M = 2^{20}$)

d) Consider a set-associative cache organization, with block size of 2K bytes and 4 blocks per set. If 'M' and 'N' denote the number of bits in the TAG and SET fields, the value of M + N (that, is, the sum of M and N) will be _____21_____.

e) For the set-associative cache organization, with block size of 2K bytes and 8 blocks per set, the memory address 6282 will map to cache set number _138_____. (Assume that the sets are numbered starting from 0)

6. A computer with a 2-level memory hierarchy consists of a cache memory and a main memory. Suppose that the cache is 6 times faster than the main memory, and the cache has a hit ratio of 95%. What will be the speedup attained by using the cache? 4.8

7. In an interleaved memory system, there are 4 memory modules M0, M1, M2, M3, each of capacity 16 Kbytes. The address decoder is fed with the address lines A0 and A1, while the address lines A2-A15 are connected to the memory modules. The memory addresses 20C5H and 20C6H will be mapped which memory modules? take module of whole 16 bit memory address with 4

8. A cache memory system with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If it is designed as a 16-way set associative cache, the length of the TAG field will be ___14_____ bits