Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2024 COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Arithmetic Logic Unit for Processors

Verilog Assignment: Design of K_ALU

In this assignment, you are required to design the KGP-Arithmetic Logic Unit (K-ALU). This K-ALU block has to be designed as an 8-bit Arithmetic Logic Unit. Your design must be extendable, in the sense that for future assignment(s) you should be able to extend it to a 32-bit version.

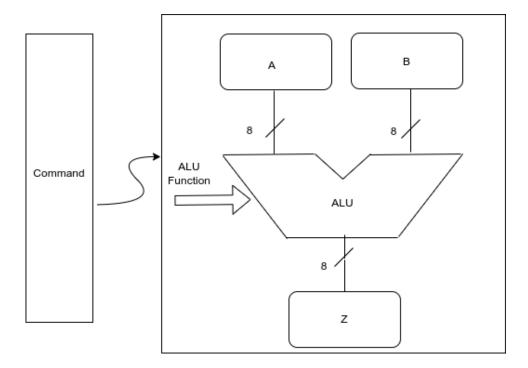


Figure 1: Top Level Diagram of K_ALU

1. The schematic block diagram of K_ALU is depicted in Figure 1. A and B refer to two 8-bit inputs, and Z the 8-bit output of K_ALU.

For the ALU operation, you need to specify the values of A and B, and also the ALU Function. Assume that this is represented by a 32-bit input Command whose description is shown in Figure 2.

The various functions that must be supported by K_ALU are shown in Table 1.

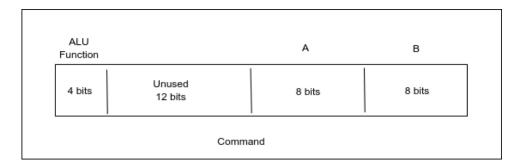


Figure 2: Structure of Command for K_ALU

Table 1: Functionalities of K_ALU

ALU Function	Function Realized
0 0 0 0	A + B
0 0 0 1	A - B
0 0 1 0	A * B
0 0 1 1	A/B
0 1 0 0	$A \wedge B$
0 1 0 1	$A \vee B$
0 1 1 0	$A \oplus B$
0 1 1 1	\overline{A}
1000	A
1 0 0 1	В
1 0 1 0	A << B
1 0 1 1	A >> B (logical)
1 1 0 0	A >> B (arithmetic)
1 1 0 1	A+4
1 1 1 0	A-4
1 1 1 1	HAM(A)

Note: HAM(A) indicates the Hamming weight of A

2. Write a Verilog top-level module to implement K_ALU, along with other modules as required. Other than multiplication and division, all other functions must be implemented in structural level.

For this assignment, implement multiplication and division in behavioral level; however, in some future assignment(s), you will have to replace these by equivalent structural designs.

3. Generate the bitmap file for the design and download it on the FPGA board. Verify the functionality of K_ALU by applying various Command inputs through switches, and observing the outputs on LEDs.