PRACTICE PROBLEMS ON INPUT-OUTPUT SYSTEMS

1. Consider a hard disk with sector size 2048 bytes, 5000 tracks per surface, 256 sectors per track, and 4 surfaces. If the disk platter rotates at 7200 rpm, and data from all four surfaces can be transferred in parallel, estimate the maximum data transfer rate.
2. A device with transfer rate of 20 KB/s is connected to a CPU. Data is transferred byte wise. Let the interrupt overhead be 6 µsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt-driven mode?
3. Suppose we want to read 2048 bytes in programmed I/O mode of transfer. The bus width is 32 bits. Each time an interrupt occurs, it takes 4 microseconds to service it (i.e. transfer 32 bits). How much CPU time is required to read 2048 bytes?
4. Assume that 25 instructions are required for each byte transfer using programmed I/O. If the clock frequency is 2 GHz and the average CPI is 2.8, what will be the data transfer rate in Mbytes/second. (Assume 1M = 1000)
5. Suppose we want to transfer 15,000 bytes of data in interrupt-driven mode of I/O transfer. It takes 2 microseconds to identify the source of the interrupt every time an interrupt occurs. On every interrupt, 64 bytes of data are transferred, and it takes 10 microseconds to service it. Calculate the total CPU time required to transfer the block of bytes.
6. Consider a system employing interrupt-driven I/O for a device that transfers data at 8 KB/s on a continuous basis. The interrupt processing takes about 100µsec and the I/O device interrupts the CPU for every byte transferred.

   While executing the ISR, the processor takes about 8µsec for the transfer of each byte. What is the fraction of CPU time consumed by the I/O device?
7. A DMA module is transferring bytes to main memory from an external device at 76800 bps. The CPU can fetch instructions at a rate of 2 million instructions per second. Assume instruction size is 32 bits. How much will the processor be slowed down due to DMA activity?
8. A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits bytes at a rate of 2400 bytes per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much time will the CPU be slowed down because of the DMA transfer?
9. Consider a disk drive with 16 surfaces, 512 tracks per surface, and 512 sectors per track, 1024 bytes per sector, and a rotation speed of 3600 rpm. The disk is operated in cycle stealing mode whereby whenever one 4-byte word is ready, it is sent to memory. Similarly for writing, the disk interface reads a 4-byte word from memory in each DMA cycle. The memory cycle time is 40 nsec. Find the maximum percentage of time that the CPU gets blocked during DMA operation.
10. A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up time for a DMA transfer takes 2000 clock cycles for the processor, and also assume that the handling of the interrupt on DMA completion requires 1000 clock cycles for the processor. The hard disk has a transfer rate of 4000 KB/s and average block size transferred is 8 KB. What fraction of the processor time is consumed by the disk, assuming that data are transferred only during the idle cycles of the CPU?