Mid-Semester Examination
Computer Organization and Architecture
(Course No: CS31001 and CS31007)

Autumn Semester, 2011
Time: 2 hours
Full Marks: 60

Attempt All Questions
Answer in Brief

1. When running an integer benchmark on a RISC machine, the average instruction mix was as follows:

Instructions	Average Frequency
Load	26 %
Store	9 %
Arithmetic	14 %
Compare	13 %
Cond. Branch	16 %
Uncond. Branch	1 %
Call/returns	2 %
Shift	4 %
Logical	9 %
Misc.	6 %

The following measurements of average CPI for individual instruction categories were made:

Instruction type	Average CPI (clock cycles)
All ALU instructions	1
Load-store	1.4
Conditional Branches:	
Taken	2.0
Not taken	1.5
Jumps	1.2

Assume that 60 % of the conditional branches are taken and that all instructions in the Misc. category are ALU instructions. What is the CPI of the benchmark on this RISC machine?

5 marks

2. Regarding the Instruction Set Architecture (ISA) of MIPS, studied in the class, answer the following questions:

   (a) A switch/case statement allows multiway branching based on the value of an integer value. In the following example, the switch variables can assume one of the three values in [0,2] and a different action is specified in each case.

```
switch(s){
    case 0: a = a + 1; break;
    case 1: a = a - 1; break;
    case 2: b = 2 * b; break;
    }
```

   Show how such a statement can be compiled into the MIPS assembly instructions.

   (b) The following program fragment computes a result $f(n)$ in register $s1 when given non-negative integer n in register $s0. Add appropriate comments to the instructions and characterize $f(n)$. Give a proper mathematical proof for any credit.

```
      add $t2,$s0,$s0
      addi $t2,$t2,1
      addi $t0,$zero,0
      addi $t1,$zero,1
loop: add $t0,$t0,$t1
      beq $t1,$t2,done
      addi $t1,$t1,2
      j loop
done: add $s1,$zero,$t0
```

10+10=20 marks

3. Draw a schematic diagram of the stack (showing the stack and frame pointers with arrows), corresponding to the following calling relationship:

```
main: jal abc
abc:  save $ra
      jal xyz
      restore $ra
      jr $ra
xyz:  jr $ra
```

   Draw the schematics for the following scenarios:

   (a) Within the main program, before calling the procedure abc.

   (b) Within procedure abc, before calling the procedure xyz.

   (c) Within procedure xyz.

   (d) Within procedure abc, after return from the procedure xyz.

   (e) Within the main program, after return from the procedure abc.

10 marks

4. For each of the following pseudoinstructions, write the corresponding produced by the URISC assembler. Use $at1 and $at2 as assembler registers.

   (a) parta: uswap src1,src2 # exchange (src1) and (src2)

   (b) partb: ubeq src1,src2,label #if (src1)=(src2), goto label

10 marks

5. An instruction set is composed of h different instruction classes, with the execution time of class-i instructions being $3 + i$ ns, $1 \leq i \leq h$. Answer the following questions:

   (a) What is the clock cycle time for a single cycle execution time?

   (b) Consider a multi-cycle implementation with a clock cycle of 1 ns, and assume that class-i instructions can then be executed in $3 + i$ clock cycles; that is ignore any overhead associated with multicycle control.

      i. Derive the performance advantage (speed up factor) of multicycle control relative to single-cycle control, assuming that the various instruction classes are used with the same frequency. Prove that the performance benefit is an increasing function of h, that is any speed up is possible for a suitably large value of h.

   (c) Draw a multi-cycle execution unit and explain how the load instruction is executed.

   (d) Discuss conditions under which a mutli-cycle implementation of a control would be decidedly inferior to single-cycle implementation.

2+6+5+2=15 marks