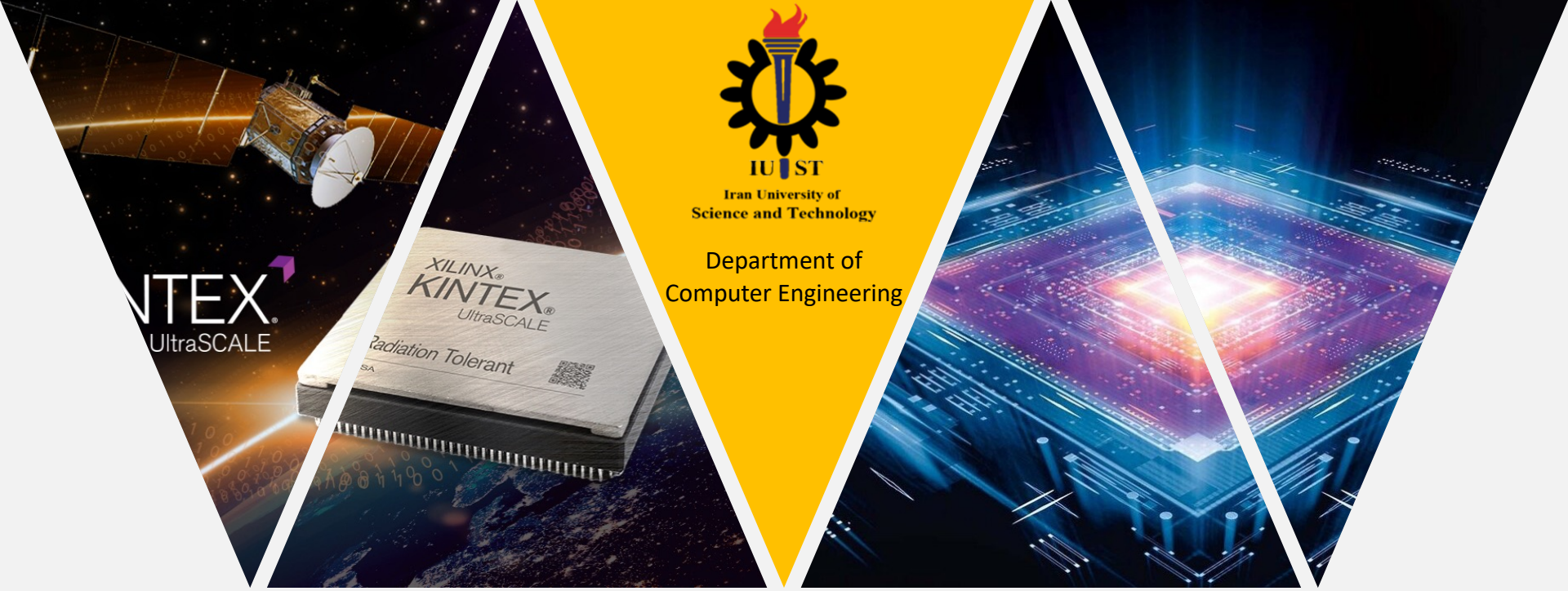

IUST
Iran University of
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Department of
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Computer Architecture Laboratory

Advanced Digital Timer Implementation Cont.

Lecturer: Ali Javadi

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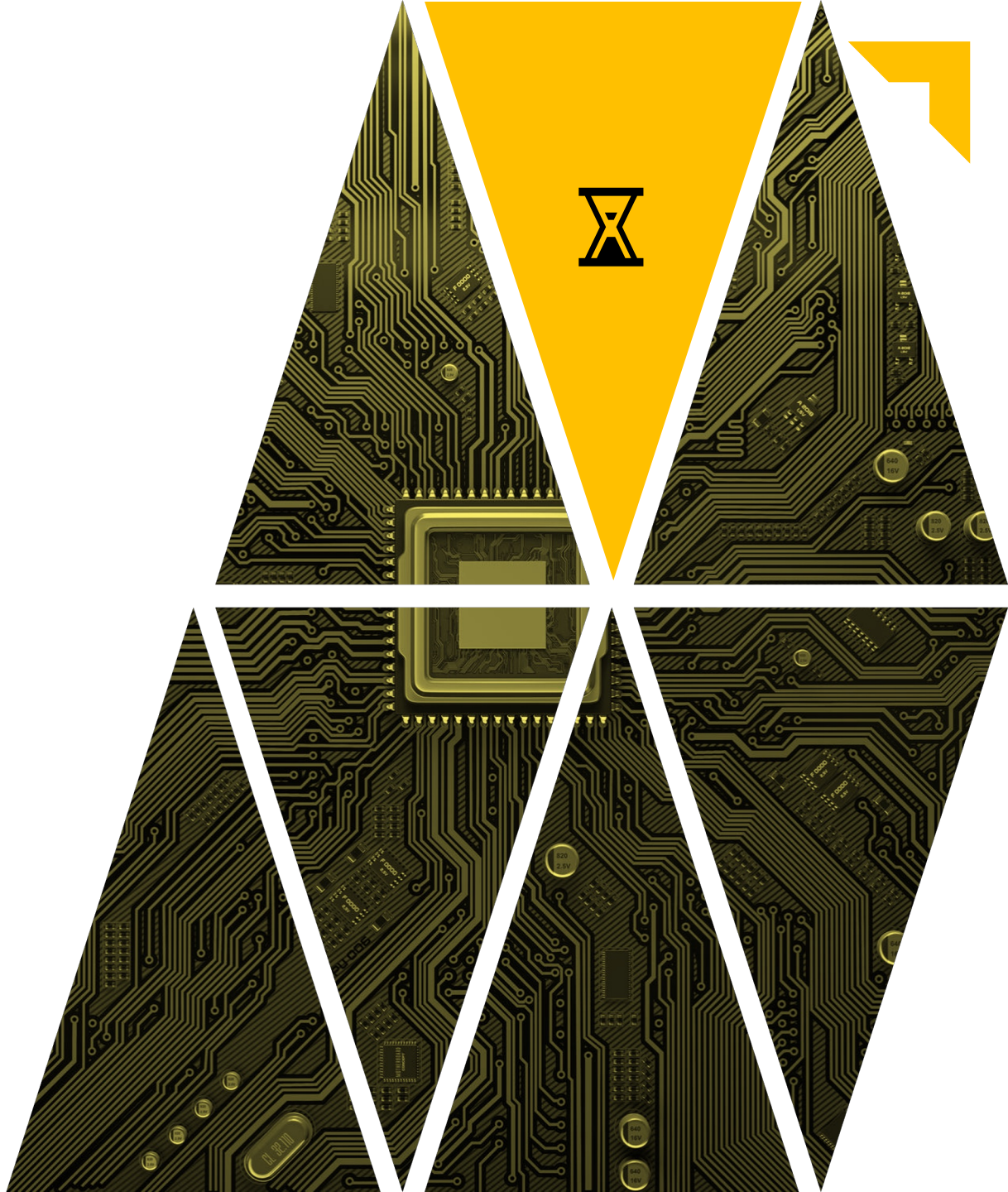
4th session

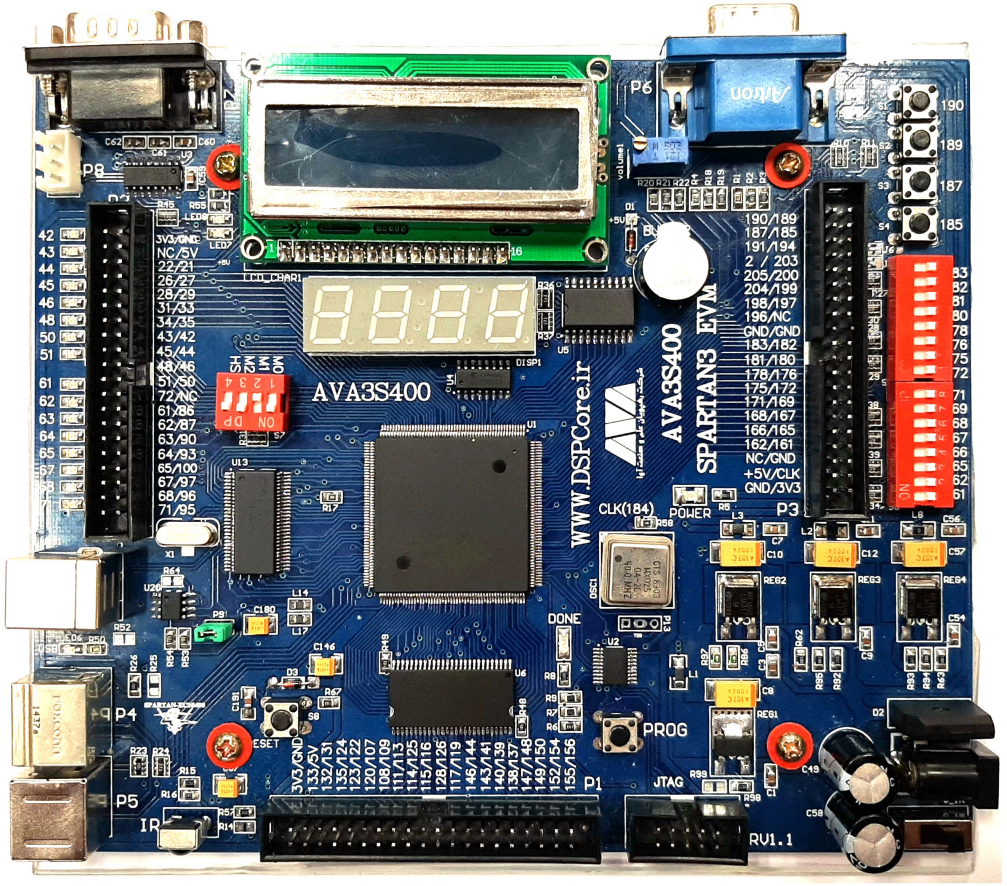
CPS LAB
IUST
Cyber-Physical Systems Laboratory

Overview

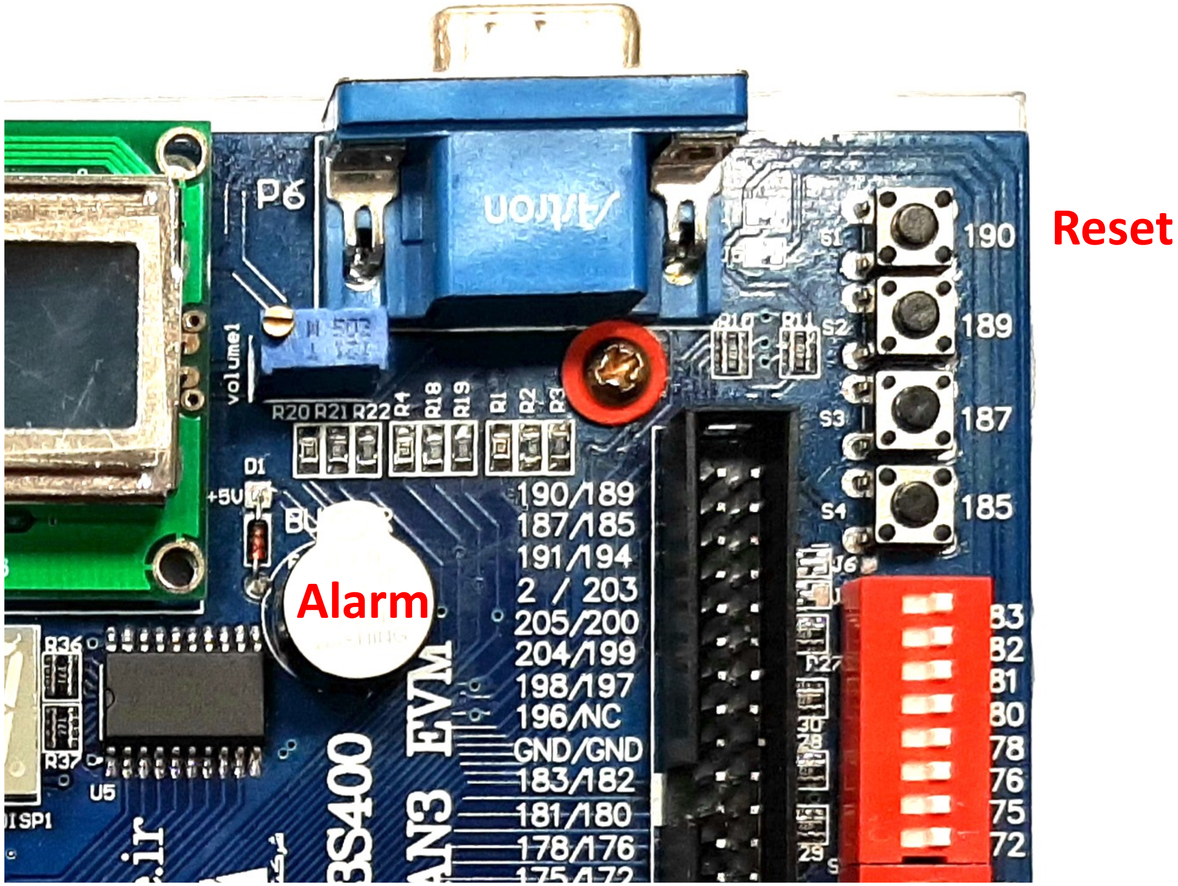
- Reset & Alarm
- Start/Stop
- Binary Output
- Experiment



Reset & Alarm

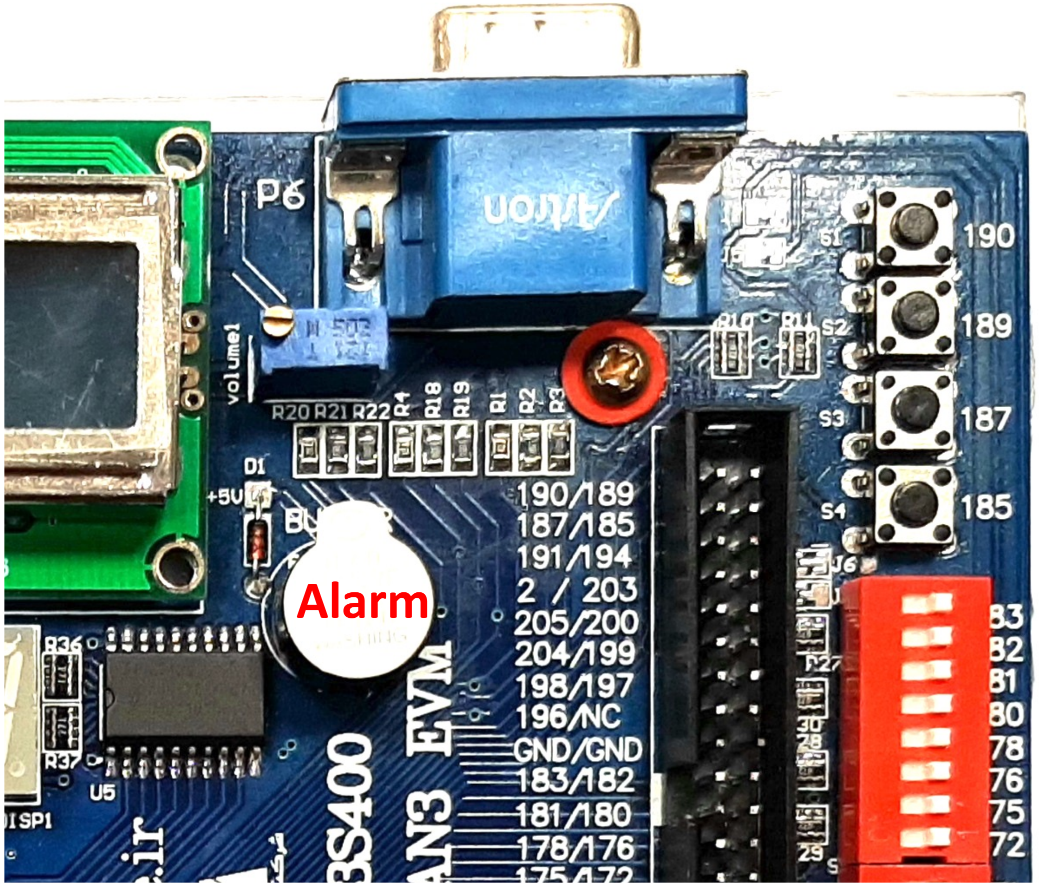

AVA3S400
WWW.DSPCore.ir
SPARTAN3 EVM
CLK(184)
POWER
DONE
PROG
JTAG
RESET
P1
P3
P4
P5
P6
P8
RV1.1

Reset & Alarm



Reset
Alarm
190
189
187
185
190/189
187/185
191/194
2 / 203
205/200
204/199
198/197
196/NC
GND/GND
183/182
181/180
178/176

Start / Stop

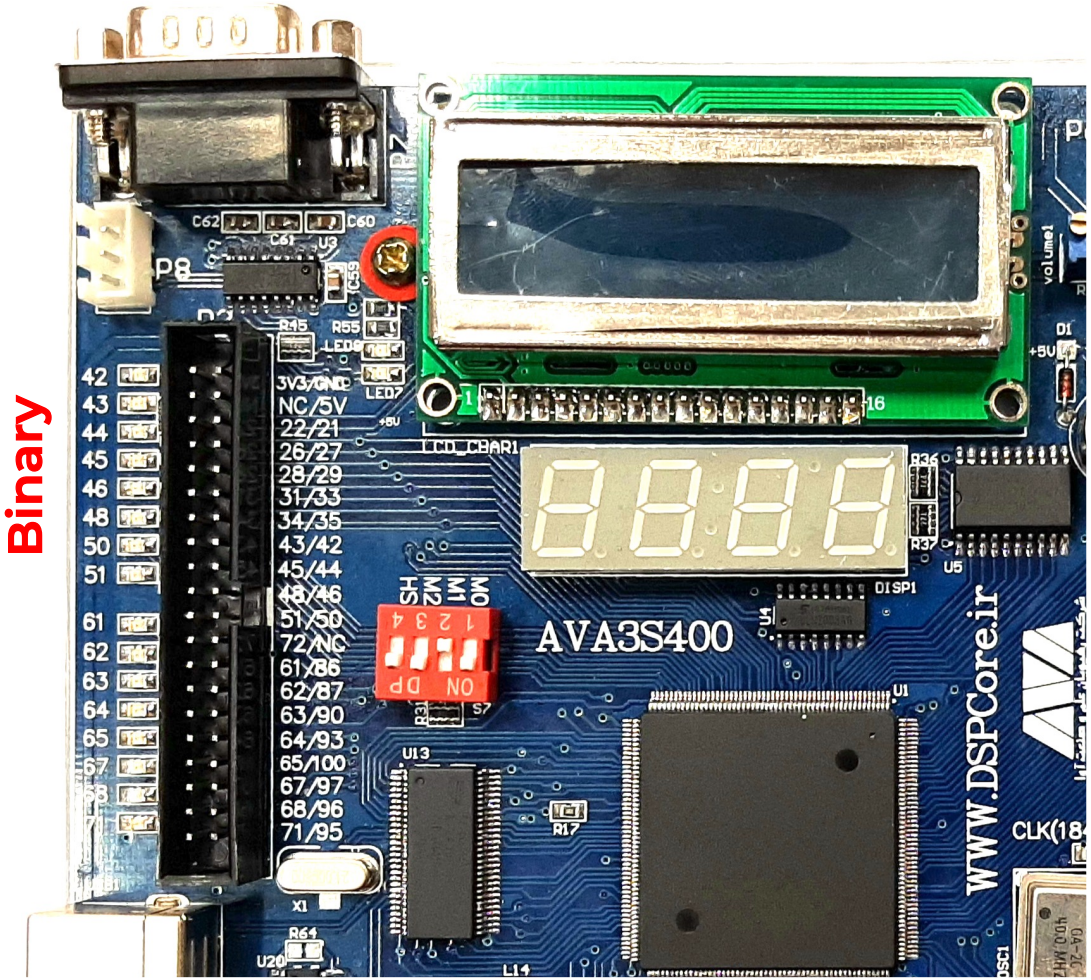


Reset

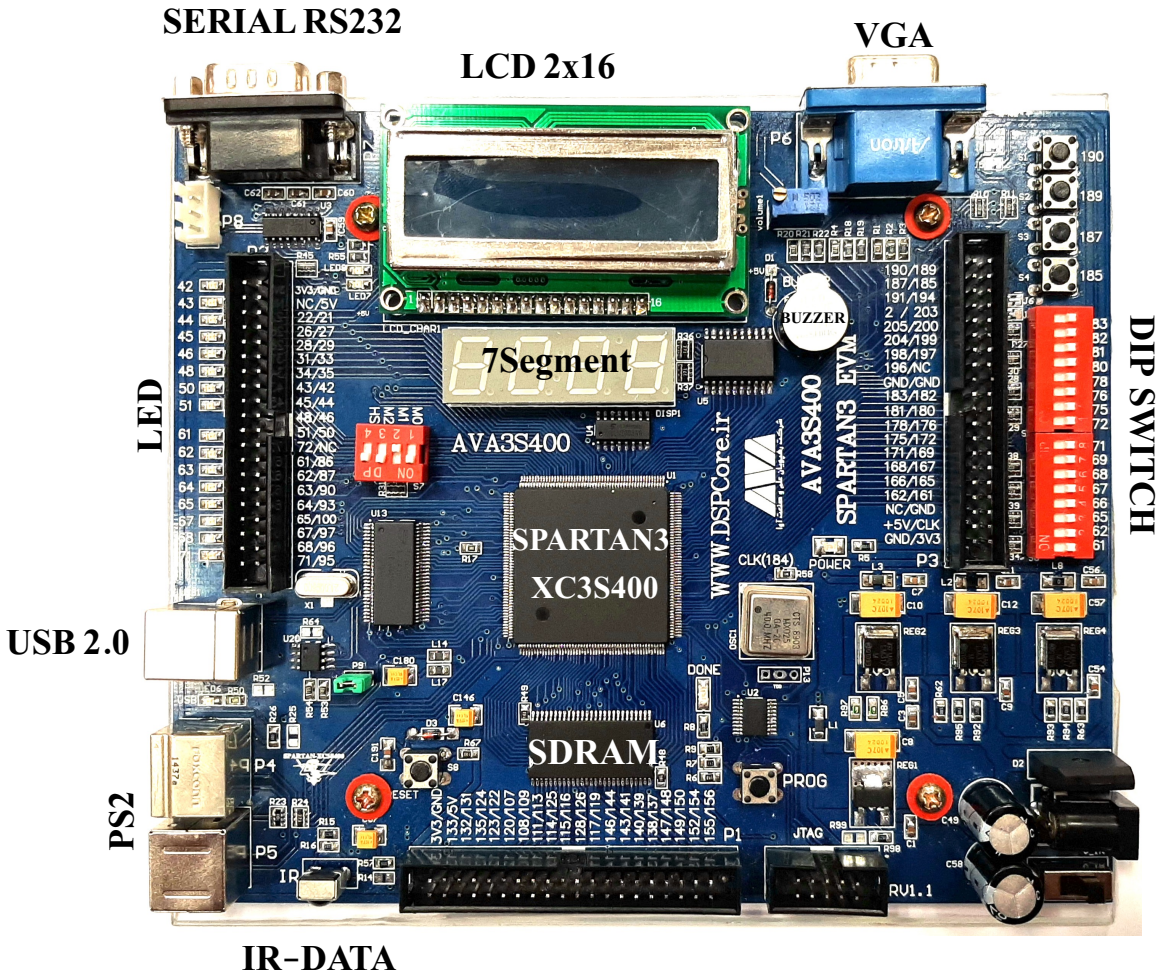
Start

Stop

Binary Output



Experiment



MM : SS

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THANK YOU

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