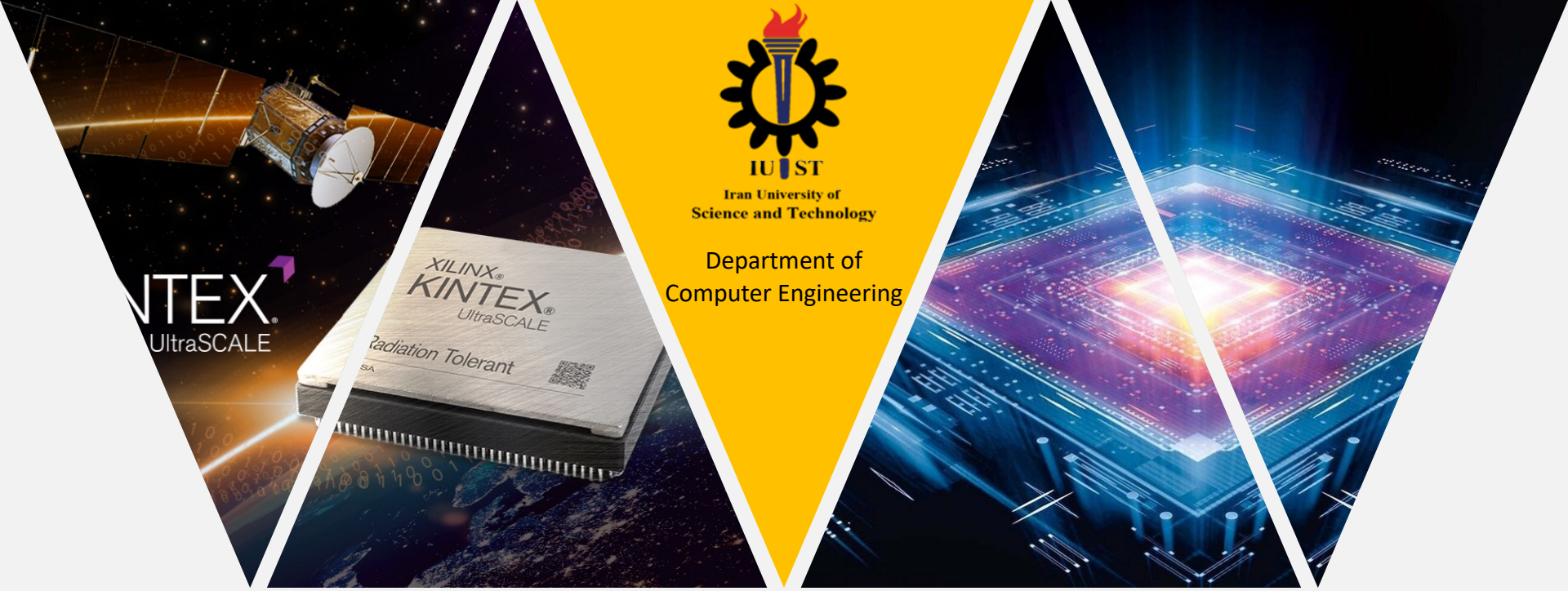


IUST
Iran University of
Science and Technology

Department of
Computer Engineering

Computer Architecture Laboratory

Digital Timer Implementation using 7 Segment Displays

Lecturer: Ali Javadi

Javadi_ali@comp.iust.ac.ir

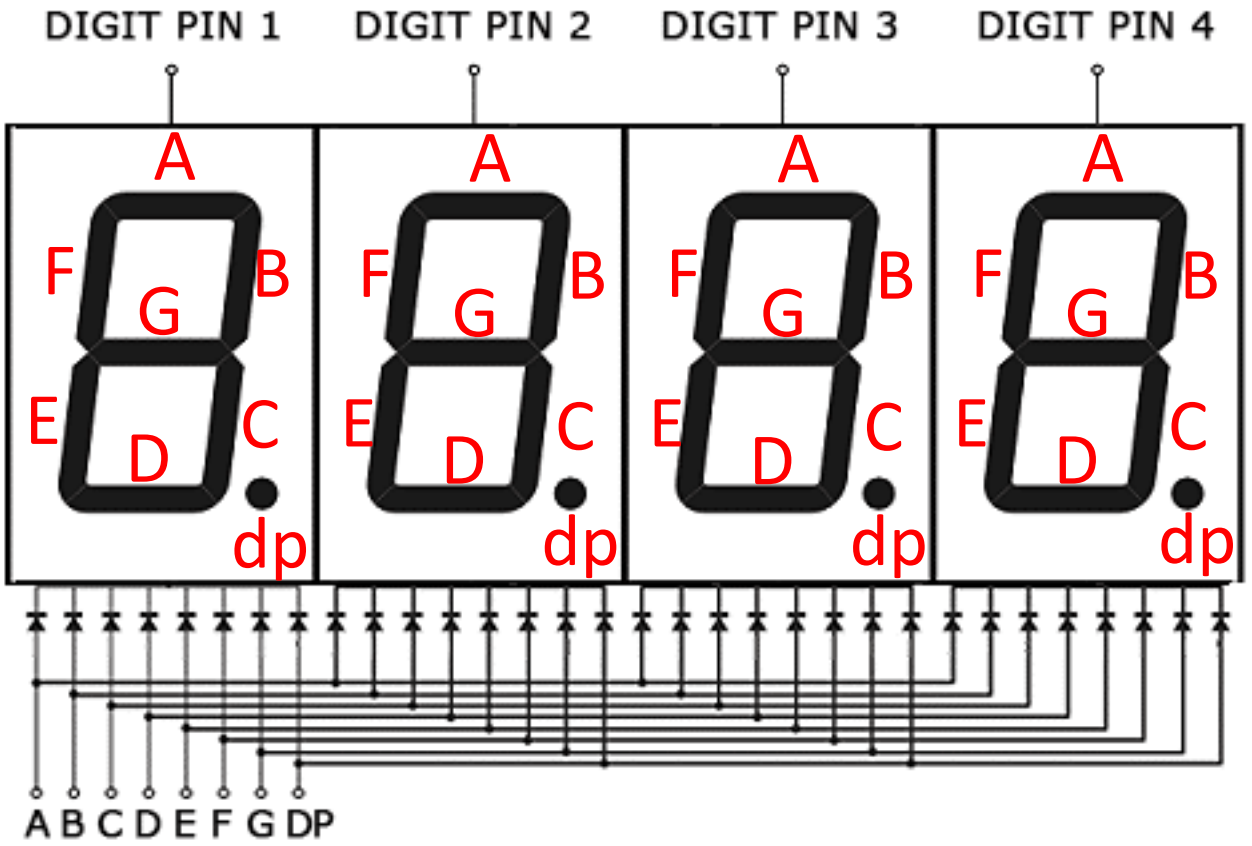
3rd session

CPS LAB
IUST
Cyber-Physical Systems Laboratory

Overview

- Parts and Wiring
- How to Set up a 7-Segment Display (Refreshing)
- How to Synthesize the Required Delay?
- Experiment

7-Segment
Parts and Wiring



How to Set up a 7-Segment Display (Refreshing)

```
process(CLK10MS)
variable RefreshSEG : integer range 0 to 4 :=0;

begin
    if (rising_edge(CLK10MS)) then
        if RefreshSEG < 4 then
        RefreshSEG := RefreshSEG + 1 ;
        else RefreshSEG := 0;
        end if;
        case RefreshSEG is
            when 0 =>
                SEG_SEL(4) <='0';
                SEG_SEL(0) <='1';
                SEG_DATA <= SEG_DATA_reg1;
            when 1 =>
```

How to Set up a 7-Segment Display (Refreshing)

```
when 1 =>
    SEG_SEL(0) <='0';
    SEG_SEL(1) <='1';
    SEG_DATA <= SEG_DATA_reg2;
when 2 =>
    SEG_SEL(1) <='0';
    SEG_SEL(2) <='1';
    SEG_DATA <= SEG_DATA_reg3;
when 3 =>
    SEG_SEL(2) <='0';
    SEG_SEL(3) <='1';
    SEG_DATA <= SEG_DATA_reg4;
when 4 =>
    SEG_SEL(3) <='0';
    SEG_SEL(4) <='1';
```

How to Set up a 7-Segment Display (Refreshing)

```
            SEG_SEL(2) <='1';
            SEG_DATA <= SEG_DATA_reg3;
        when 3 =>
            SEG_SEL(2) <='0';
            SEG_SEL(3) <='1';
            SEG_DATA <= SEG_DATA_reg4;
        when 4 =>
            SEG_SEL(3) <='0';
            SEG_SEL(4) <='1';
            SEG_DATA <= "0000000";
        when others => null;
    end case;
  end if;
end process;
```

How to Synthesize Required Delay

```
process(GCLK)
variable count_div : integer range 0 to 100000 :=0;
begin
    if (rising_edge(GCLK)) then
        if count_div < 80000 then
            count_div := count_div + 1 ;
        else
            count_div := 0;
            CLK10MS <= not CLK10MS;
        end if;
    end if;
end process;
```

Experiment
7-Segment Timer

CPS LAB

Cyber-Physical Systems Laboratory

THANK YOU

Cyber-Physical Systems Laboratory

cps.iust.ac.ir

+98 (21) 73225350

Javadi_ali@comp.iust.ac.ir

Room 120, Department of Computer Engineering, Iran University of Science and Technology, University Road, Hengam Street, Resalat Square, Narmak, Tehran, IRAN 16846-13114.