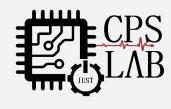


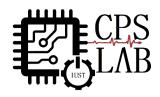
Computer Architecture Laboratory Time to Complete Previous Experiments

Lecturer: Ali Javadi

Javadi ali@comp.iust.ac.ir

7th session





Overview

Full Adder & BCD to 7-Seg

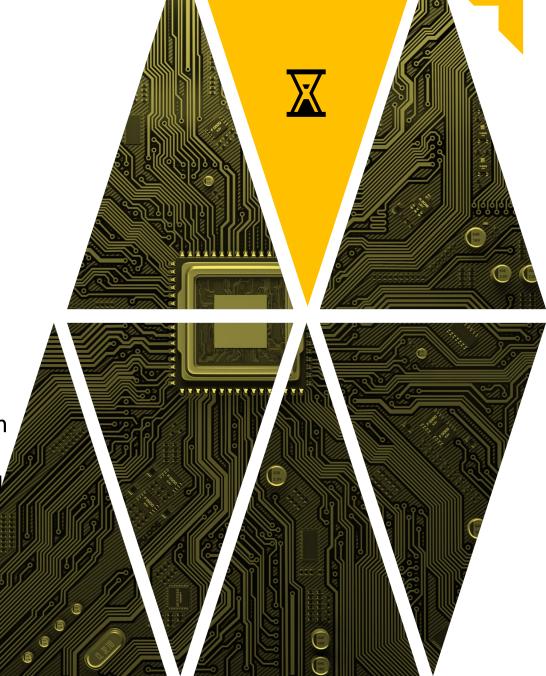
• Digital Timer

Advanced Digital Timer

• UART Serial Communication

Basic Calculations and Send

via UART





THANK YOU

Cyber-Physical Systems Laboratory



cps.iust.ac.ir



+98 (21) 73225350



Javadi_ali@comp.iust.ac.ir



Room 120, Department of Computer Engineering, Iran University of Science and Technology, University Road, Hengam Street, Resalat Square, Narmak, Tehran, IRAN 16846-13114.