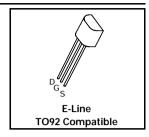
P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP2110A

ISSUE 2 - MARCH 94

FEATURES

- * 100 Volt V_{DS}
- * $R_{DS(on)} = 8\Omega$



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V _{DS}	-100	V
Continuous Drain Current at T _{amb} =25°C	I _D	-230	mA
Pulsed Drain Current	I _{DM}	-3	Α
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T _{amb} =25°C	P _{tot}	700	mW
Operating and Storage Temperature Range	T _j :T _{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

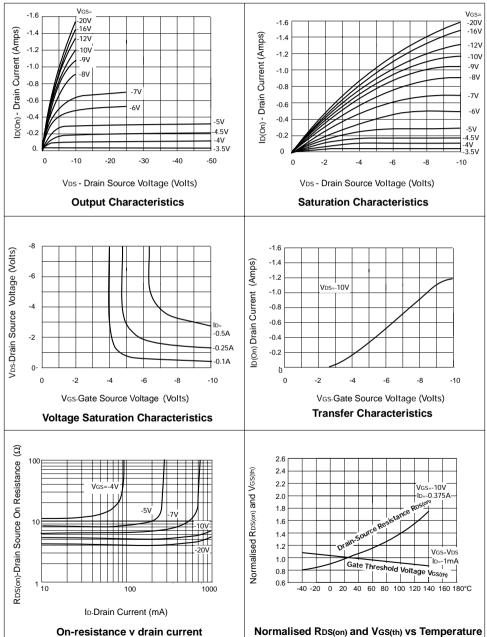
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.	
Drain-Source Breakdown Voltage	BV _{DSS}	-100		V	I _D =-1mA, V _{GS} =0V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	ID=-1mA, V _{DS} = V _{GS}	
Gate-Body Leakage	I _{GSS}		20	nA	V _{GS} =± 20V, V _{DS} =0V	
Zero Gate Voltage Drain Current	I _{DSS}		-1 -100	μ Α μ Α	V _{DS} =-100 V, V _{GS} =0 V _{DS} =-80 V, V _{GS} =0V, T=125°C(2)	
On-State Drain Current(1)	I _{D(on)}	-750		mA	V _{DS} =-25 V, V _{GS} =-10V	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}		8	Ω	V _{GS} =-10V,I _D =-375mA	
Forward Transconductance (1)(2)	g _{fs}	125		mS	V _{DS} =-25V,I _D =-375mA	
Input Capacitance (2)	C _{iss}		100	pF	V _{DS} =-25V, V _{GS} =0V, f=1MHz	
Common Source Output Capacitance (2)	C _{oss}		35	pF		
Reverse Transfer Capacitance (2)	C _{rss}		10	pF		
Turn-On Delay Time (2)(3)	t _{d(on)}		7	ns	V _{DD} ≈-25V, I _D =-375mA	
Rise Time (2)(3)	t _r		15	ns		
Turn-Off Delay Time (2)(3)	t _{d(off)}		12	ns		
Fall Time (2)(3)	t _f		15	ns		

⁽¹⁾ Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%

⁽²⁾ Sample test.

ZVP2110A

TYPICAL CHARACTERISTICS



ZVP2110A

TYPICAL CHARACTERISTICS

