

**Department of Electronics and Communication Engineering**

LOW POWER 3-BIT ENCODER DESIGN USING MEMRISTOR

**Batch: BB1**

**Abstract:**

The power consumption is a very critical parameter in electronic digital circuits. In this project, power dissipation is reduced in digital circuits using memristors. The use of memristors in the design of digital logic gates presents an alternative approach to current integrated circuit (IC) design and is a promising development in computing architecture. The manufacturing process for memristor-based gates is straightforward, as memristors can be designed on top of the polysilicon gate of NMOS transistors. This can lead to an increase in transistor density on a chip. Additionally, lower power consumption is achieved by tweaking the memristor's Ron, Roff, and Rint values. The memristor-based design can be utilised to model various combinational logic circuits, and the primary objective of this project is to analyse and design a 3-bit encoder with different logics using LTspice software.

**Name of the Guide**: Mr. C. Leela Mohan, Asst. Professor

**Project Associates:**

SD. JAVEED (19711A04A9),

M.N. ROHITH (19711A0473),

M. VENKATA SUBBAIAH (19711A0470),

SK. MASTHAN (19711A04A1)

**Signature of the Guide Signature of the HOD**