A Project Report on

**LOW POWER MEMRISTOR-BASED**

**3-BIT ENCODER DESIGN**

*is submitted in partial fulfillment of the requirement for the award of**the Degree of* ***Bachelor of Technology***

*to*



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTHAPURAMU**

**By**

**SD. JAVEED**

**(19711A04A9)**

**M.N. ROHITH M. VENKATA SUBBAIAH**

**(19711A0473) (19711A0470)**

**SK. MASTHAN**

**(19711A04A1)**

**Under the Guidance of**

**Mr. C. LEELA MOHAN,** M.Tech

**Associate Professor**

****

Department of Electronics and Communication Engineering****

**MAY 2023**

****

**Department of Electronics and Communication Engineering**

**CERTIFICATE**

This is to certify that the project report entitled **“LOW POWER MEMRISTOR-BASED 3-BIT ENCODER DESIGN”** being submitted by **SD. JAVEED (19711A04A9), M.N. ROHITH (19711A0473), M. VENKATA SUBBAIAH (19711A0470), SK. MASTHAN (19711A04A1)** in partial fulfillment for the award of the Degree ofBachelor of Technology in Electronics & Communication Engineering Department to the Jawaharlal Nehru Technological University Anantapur, Ananthapuramu is a record of bonafied work carried out by them under my guidance and supervision.

The results embodied in this project report have not been submitted to any other University or Institute for the award of any Degree or Diploma.

Mr. C. LEELA MOHAN, M.Tech Dr.K.MURALI, M.Tech., Ph.D

Associate Professor Professor & HOD

Project Supervisor Department of ECE

Date of Viva-Voce\_\_\_\_\_\_\_\_\_\_\_

INTERNAL EXAMINER EXTERNAL EXAMINER

**ACKNOWLEDGEMENT**

We are extremely grateful to **Dr. P. NARAYANA, Ph.D. Founder,** Narayana Educational Institutions, Andhra Pradesh for the kind blessings. We are extremely thankful to **Mr. R. Sambasiva Rao B.Tech, Registrar** Narayana Engineering, Nellore.

We are much obliged to **Dr. A.V.S Prasad, Ph.D. Director,** Narayana Engineering & Pharmacy Colleges, for the continuous encouragement and support. We owe indebtedness to our **Principal Dr. G. Srinivasulu Reddy, M.Tech., Ph.D.,** Narayana Engineering College, Nellore for providing us the required facilities.

We express our deep sense of gratitude and sincere thanks to **Dr. K. Murali, M.Tech, Ph.D, Professor & HOD,** Department of Electronics and Communication Engineering, Narayana Engineering College, Nellore for providing the necessary facilities and encouragement towards the project work.

We thank our project guide, **Mr. C. Leela Mohan, M.Tech, Associate Professor, Department of Electronics and Communication Engineering** for his guidance, valuable suggestions and support in the completion of the project.

We gratefully acknowledge and express our thanks to teaching and non-teaching staff of E.C.E Department. We would like to express our love and affection to our parents for their encouragement throughout this project.

**Project Associates**

SD. JAVEED (19711A04A9)

M.N. ROHITH (19711A0473)

M. VENAKATA SUBBAIAH (19711A0470)

SK. MASTHAN (19711A04A1)

**ABSTRACT**

In this project, power dissipation is reduced in digital circuits using memristors. The use of memristors in the design of digital logic gates presents an alternative approach to current integrated circuit (IC) design and is a promising development in computing architecture. The manufacturing process for memristor-based gates is straightforward, as memristors can be designed on top of the polysilicon gate of NMOS transistors. This can lead to an increase in transistor density on a chip. Additionally, to achieve even lower power consumption, we are tweaking the memristor's Ron, Roff, and Rint values in this project. The memristor-based design can be utilised to model various combinational logic circuits, and the primary objective of this paper is to analyse and design a 3-bit encoder with different logics using LTspice.

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