
ACTIVITY 0
CONTROL AND ANALYSIS OF ELECTRICAL
SYSTEMS DOMINATED BY POWER
ELECTRONICS

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Javier Muñoz Sáez
- UPC -

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1 CLARKE TRANSFORM

By opening the file ‘Script Clarke 3D Base.m’ in matlab, the following concepts were studied.

1.1 Understanding the time domain

The perfect three phase balanced sinusoidal signals are presented in figure Figure 1, each signal represents the voltage of each phase a,b c.

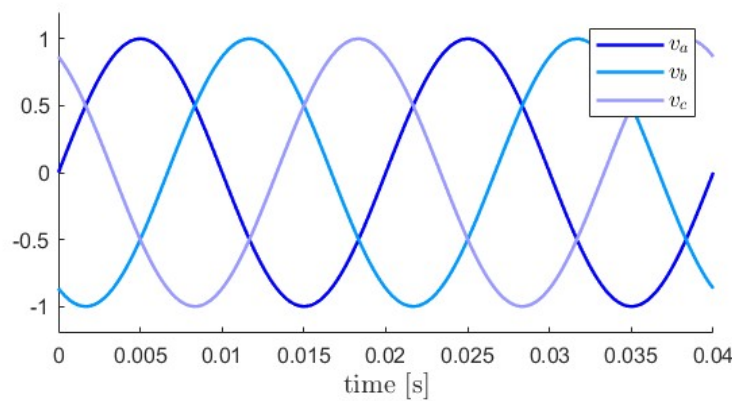


Figure 1: V(abc) over time

The motivation behind the usage of the Clarke or transformation (Figure 2), is to eliminate cross-coupled terms in v(abc) obtaining an orthogonal space reference v(alpha beta zero). No information is lost (isomorphism) after this transformation, and it simplifies a lot the equations describing the system and consequently the control.

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$$

Figure 2: V(alpha beta zero) Clarke transformed from V(abc)

Once the Clark transformation is applied to V(abc) the following signals are obtained (Figure 3), as our example grid is completely balanced (no harmonics) $V_{zero} = 0$ and $|V_{\alpha}| = |V_{\beta}|$

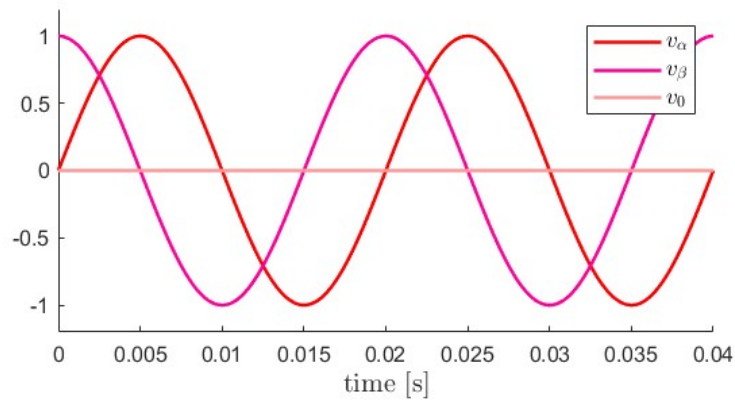


Figure 3: $V(\alpha\beta 0)$ over time

1.2 Understanding the 3D cubic representation

The Figure 4 shows the original reference V_{abc} in black, the transformed reference alpha beta zero in pink, and lastly the revolving voltage points represented in alpha beta zero references (red circle).

The red circle is contained in the plane alpha beta because no harmonics are used in the representation (yet).

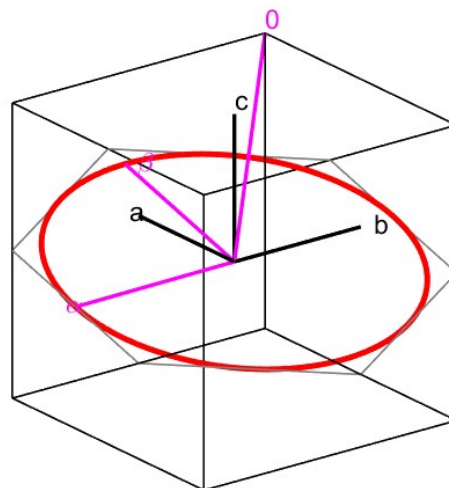


Figure 4: 3D representation of Clarke transformation and projections

1.3 Adding harmonics

Sometimes, in order to increase the DCbus utilization at expense of increased voltage THD , a 3rd Harmonic is added to our fundamental signal Figure 5, it could also represent a non-linear load.

```

harmonic_amplitude=0.1;
harmonic_number=3;
va = sin(w*t) + harmonic_amplitude*sin(harmonic_number*(w*t));
vb = sin(w*t - 2*pi/3) + harmonic_amplitude*sin(harmonic_number*(w*t - 2*pi/3));
vc = sin(w*t + 2*pi/3) + harmonic_amplitude*sin(harmonic_number*(w*t + 2*pi/3));

```

Figure 5: Matlab formulas for 3rd harmonic injection 10%

The resulting Vabc signals are deformed as seen in Figure 8, as expected of any 3n harmonic it affects the Vzzero component.

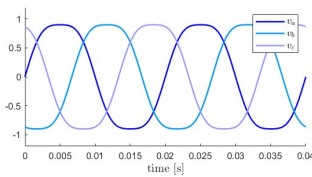


Figure 6: V(abc) with 3rd harmonic

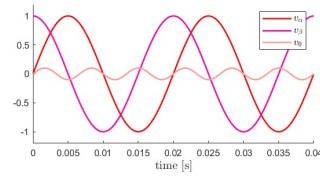


Figure 7: V(alpha beta zero) with 3rd harmonic

Vzero is not 0 anymore, our previously perfect red circle is not contained in the alpha-beta plane anymore, now is pringle-chip shaped. Even with the Vzzero component not equal to zero the system would still be considered simetric and balanced, both Valpha and Vbeta are still equal and usable in a PLL.

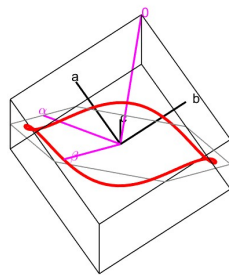


Figure 8: 3D representation with 3rd harmonic

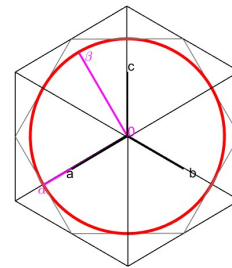


Figure 9: Same plot but seen from top

Now trying with 4th and 5th harmonics, there is no multiple of 3 harmonic so no V_{zero} component, these two examples are instead distorting the V_{α} and V_{β} components (the red circle projection is not a circle anymore), they cannot be as easily filter out as in the previous case, this will bring problems if we are to feed this to a PLL.

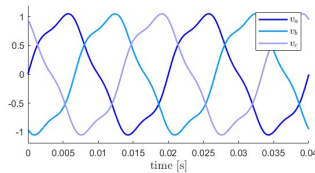


Figure 10: vabc with 4rd harmonic

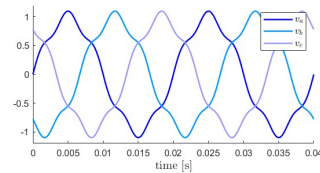


Figure 11: vabc with 5th harmonic

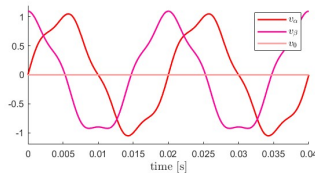


Figure 12: V(alpha beta zero) with 4rd harmonic

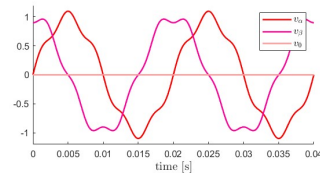


Figure 13: V(alpha beta zero) with 5th harmonic

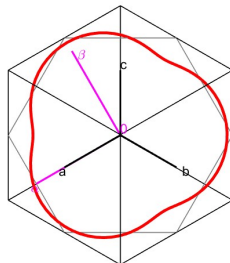


Figure 14: top view of 3D representation with 4rd harmonic

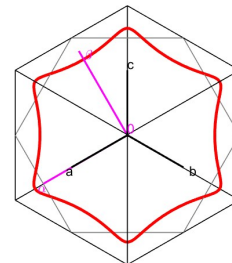


Figure 15: top view of 3D representation with 5th harmonic

2 PWM FROM A GRID CONNECTED CONVERTER

Opening "Model0 PWM Base.slx" in simulink and discussing the following aspects

2.1 Understanding how the modulation is implemented

The model Figure 16, conceptually consists in a converter voltage source (circled in yellow), and a grid voltage source (circled in orange).

The converter voltage source phase relative to the grid is meant to be changed (blue blocks) in order to demonstrate active power transfer to or from the grid.

The PWM signals are created with a triangular carrier signal and some compare blocks. There are also some blocks to measure the obtained voltage and currents of our converter and grid.

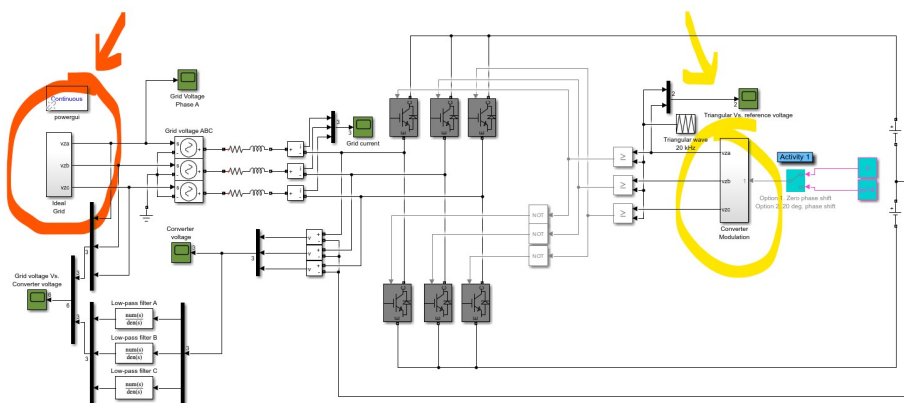


Figure 16: simulink model of the converter

2.2 voltages applied to the converter

After the comparator blocks, the sinusoidal signal used as reference by the converter is transformed in Figure 17 pwm signals.

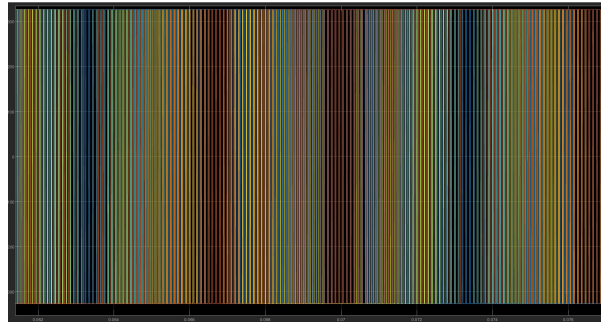


Figure 17: PWM signals of the converter full bridge

When filtered Figure 18, the pwm signals show back the same sinusoidal signals.

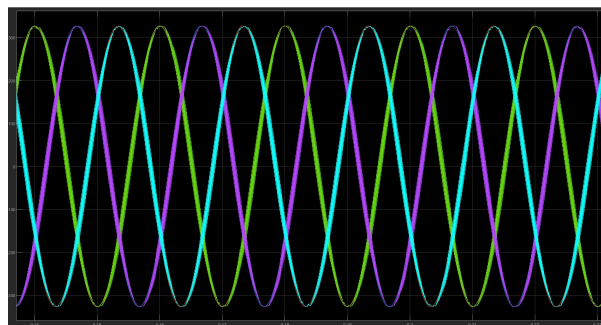


Figure 18: filtered PWMs from previous plot

Residual small currents flowing from the grid to the converter Figure 19, they could be considered noise from the model and the PWM harmonics.

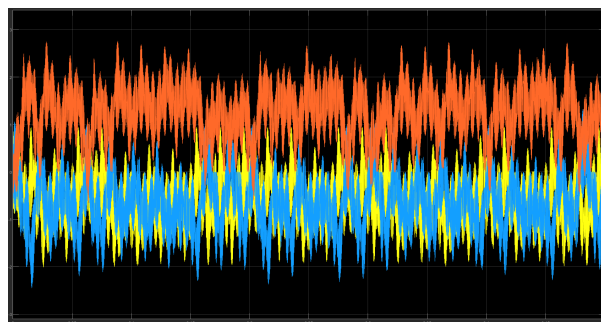


Figure 19: currents from the grid

2.3 Consequences of modifying phase differences

When applying a small phase difference of $\pi/18$ Figure 20 , the current flowing from the grid to our converter increases, as our VSC is immitating an ideal load, all current waveforms are almost perfect sinusoidals (still some noise from the pwm) Figure 21.

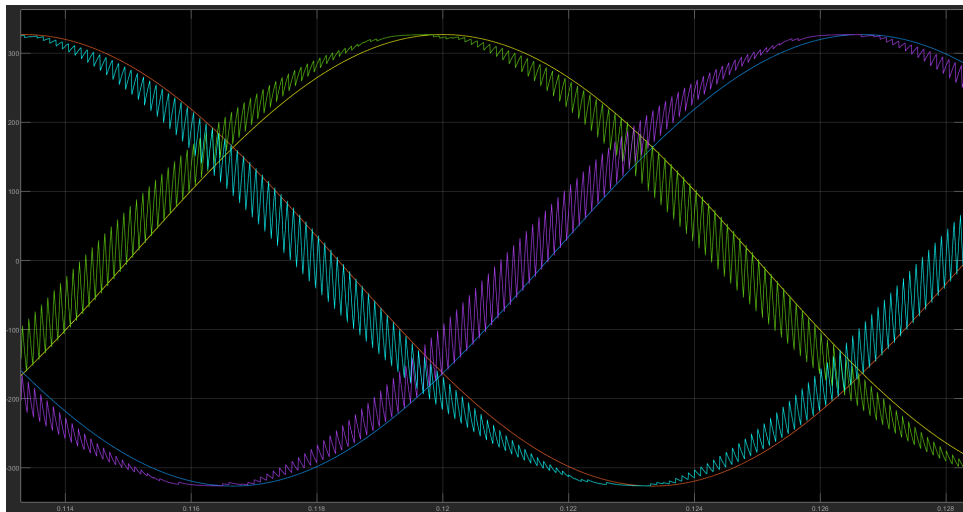


Figure 20: voltages from the grid and from the converter(filtered)

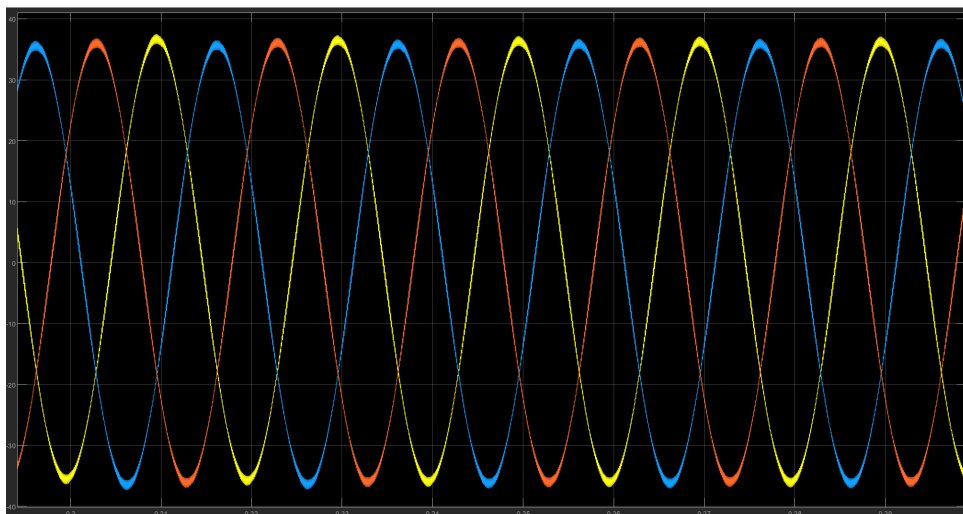


Figure 21: current from the converter to the grid

3 CLARKE AND PARK TRANSFORMATIONS

Opening "Model1 Clarke Park.slx" in simulink and discussing the following aspects

3.1 Understanding Clarke transformation in time domain

When the reference phase angle theta is set to 0 in Figure 22, it means our transformation reference is fixed to theta 0, we obtain the clarke transform alpha beta sine waves. Figure 23.

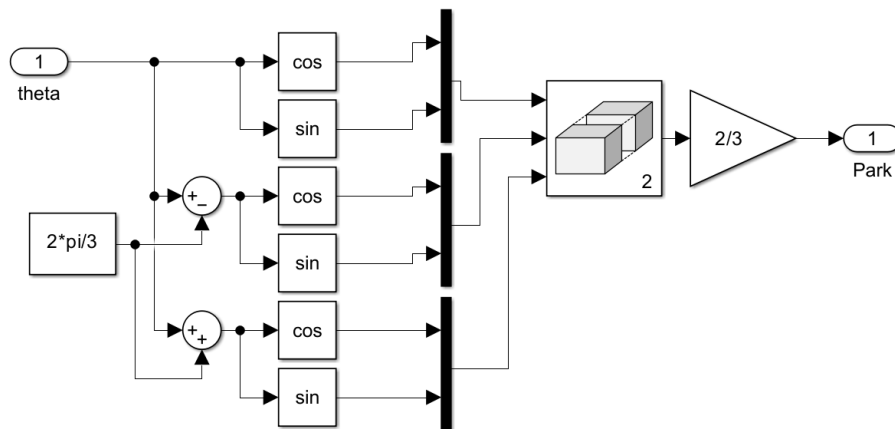


Figure 22: Clark or Park transform block

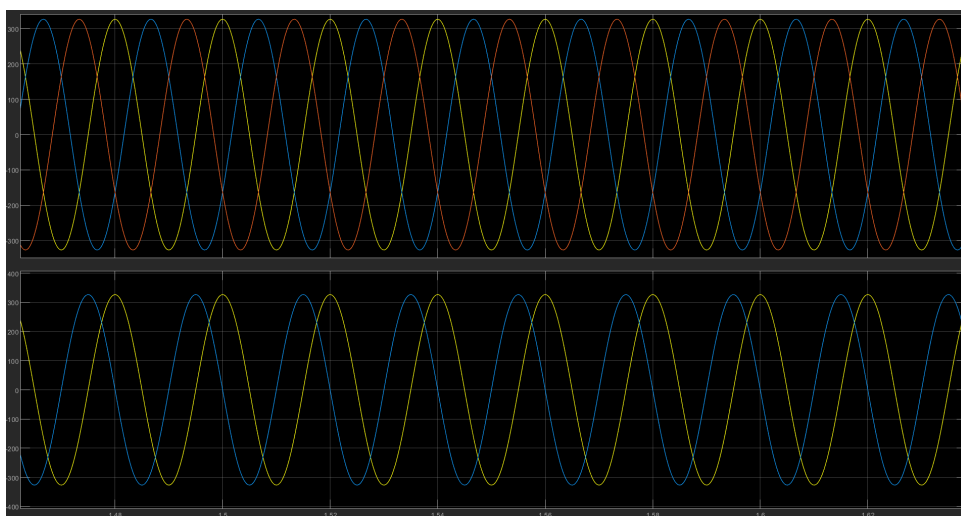


Figure 23: Vabc and Valphabeta

3.2 Understanding Park transformation in time domain

If θ is perfectly following the angle from the grid, our reference model spins matching the spin of the network voltage vectors, this situation creates V_d and V_q which are not sinusoidal but constant. Figure 24.

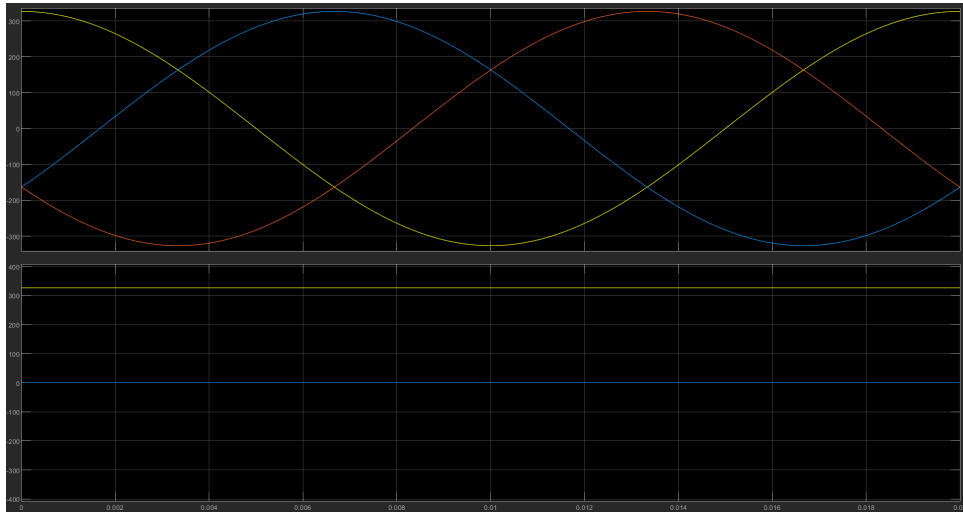


Figure 24: vabc and vdq park transform

If we add 5th harmonic to the voltage but only use the fundamental angle to calculate the park transformation, the harmonic noise is translated down to V_d and V_q , they stop being constant. Figure 25.

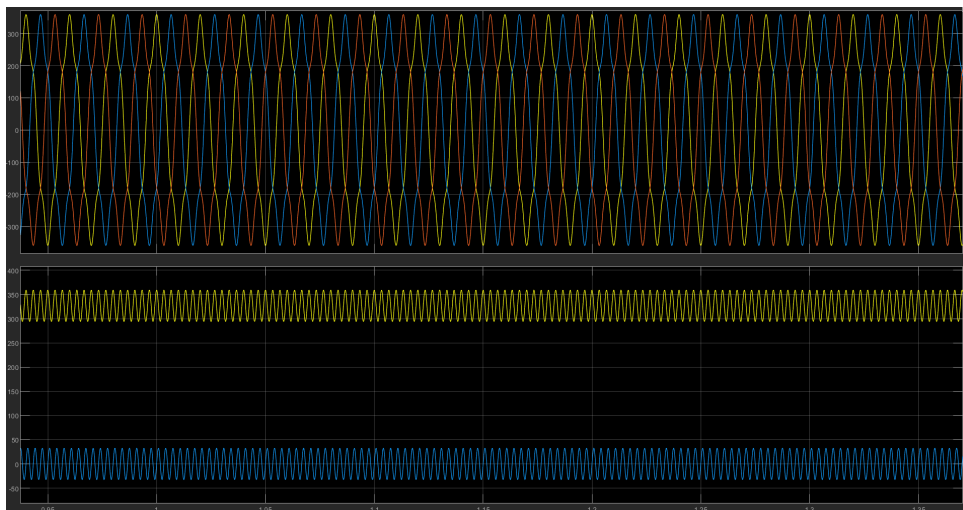


Figure 25: vabc and vdq park transform with a 5th harmonic

3.3 Consequences of applying phase shift

As the clarke transformation doesn't use the angle θ for anything, the transformation remains as accurate as before. But when we feed an angle with a constant error to the Park transform, as the frequency still matches but the phase is off, V_{α} and V_{β} would be constant but not correct.

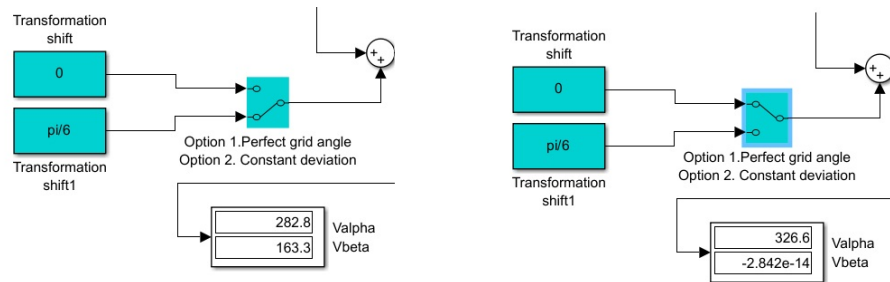


Figure 26: results for park whit and without phase error

4 PLL CONTROL

Opening "Model2 PLL.slx" in simulink and discussing the following aspects.

4.1 Fiddling with the phase and amplitudes of the grid voltage

Because of the PLL and the simulated grid start both with phase 0, the PLL is already working in steady state, phase error=0. When we double the Grid voltage amplitude at mid simulation, the PLL is still locked in so V_d is still 0 (blue), V_q doubles in value as expected (yellow). Figure 27.

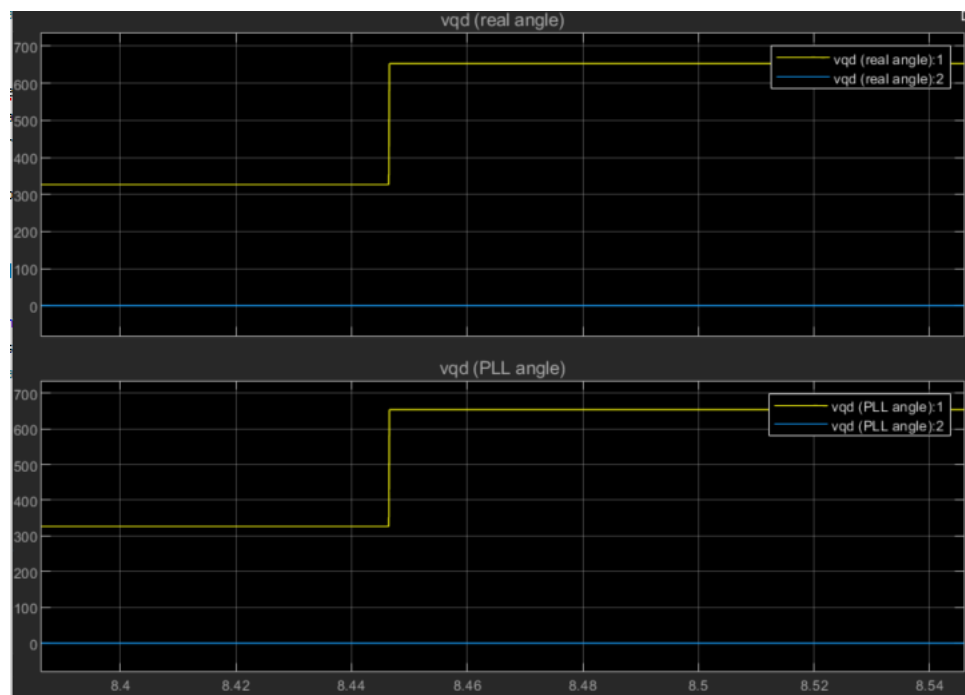


Figure 27: real and estimated Vdq voltages

When a phase of $\pi/9$ is introduced at mid simulation, the PLL control loop is put to work, the estimated angle disturbance clears in less than 1 milisecond. Figure 28.

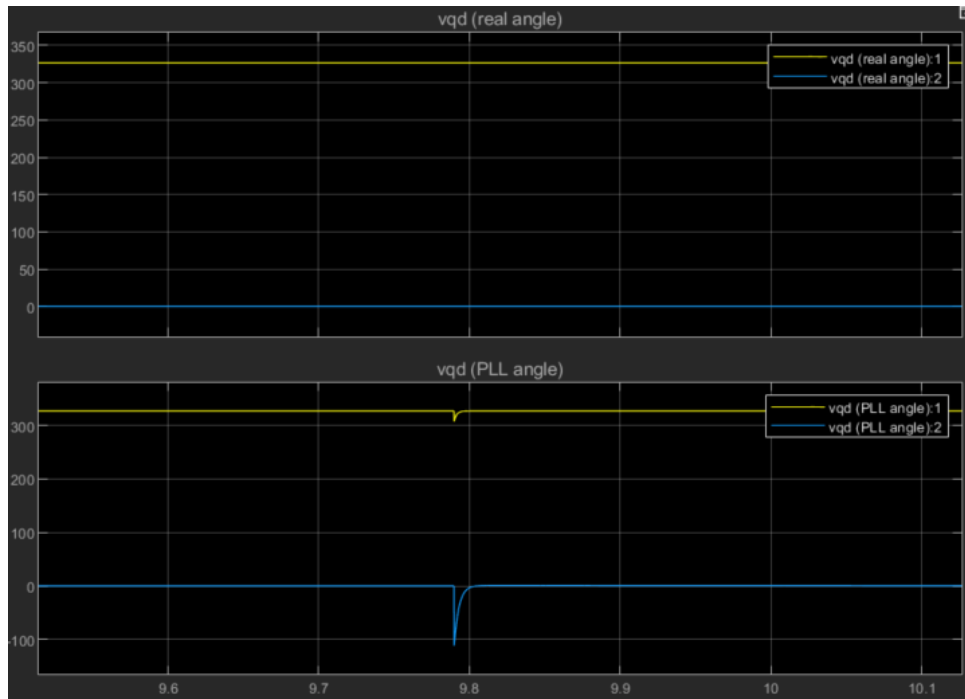


Figure 28: real and estimated Vdq voltages

4.2 Observing behaviour of the PLL after changes in K_p and K_i

Increasing the K_p from the PLL control block results in faster response to perturbations. Figure 29.

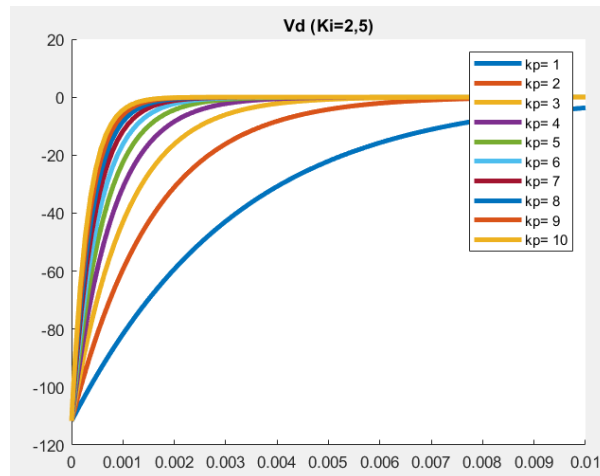


Figure 29: V_d for different k_p values

Increasing the K_i doesn't have noticeable effect in the time response (slightly slower for higher K_i) but our PLL will reduce quicker the static error when the PLL has locked the phase. Figure 30.

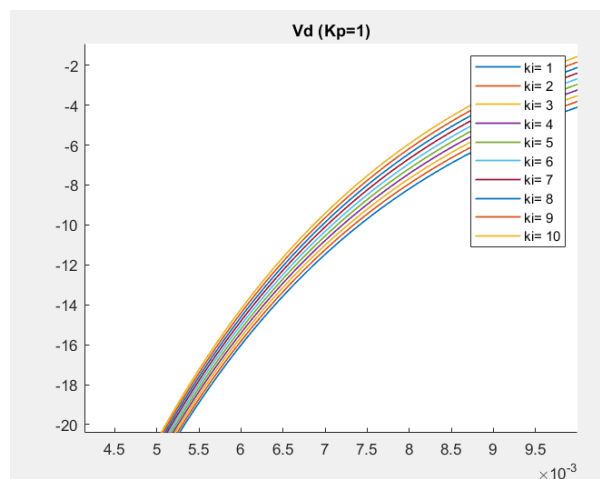


Figure 30: V_d for different k_i values

4.3 Amplitude single phase disturbance in Vdq0

By adding a 1.2 disturbance mid simulation, the Grid suddenly has a negative sequence component, this component's nature makes the grid angle to oscillate 50Hz up and down. Figure 31. That oscillation is followed and not filtered by the PLL which is just doing its job, this noise will mess with our control and the quality of our delivered power.

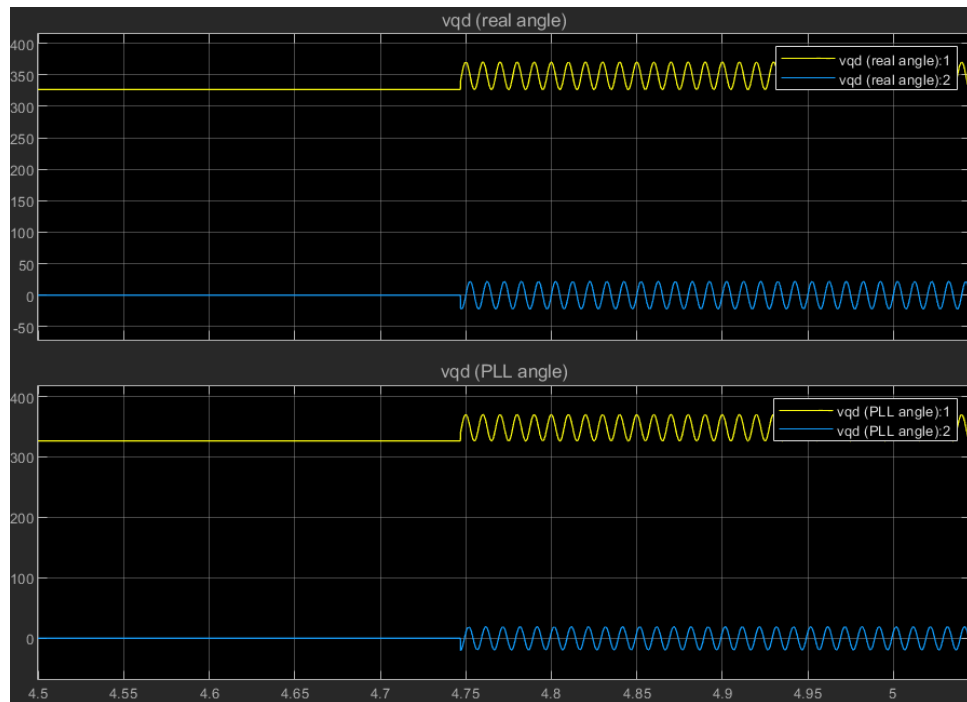


Figure 31: real and estimated angles with $V_a=1.2$ disturbance

5 CURRENT LOOP

Opening "Model3 CurrentLoop.slx" in simulink and discussing the following aspects.

5.1 Operation of the current control loop

This specific control loop uses variables in dq0 domain, this means right before and after this block there are clarke-park transforms happening, in charge of translating from and to abc domain. Figure 32. There is also no PLL involved in the simulation, the instantaneous angle theta is just taken from the simulink block synthesising the grid voltages itself.

$$\begin{bmatrix} v_{zq} \\ v_{zd} \end{bmatrix} - \begin{bmatrix} v_{lq} \\ v_{ld} \end{bmatrix} = \begin{bmatrix} r_l & l_l \omega_e \\ -l_l \omega_e & r_l \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} l_l & 0 \\ 0 & l_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_q \\ i_d \end{bmatrix}$$

Figure 32: current controller equations, coupling terms in blue

There are two separate PI control blocks one for d (direct) and another for q (quadrature) components of current and voltage. Figure 33.

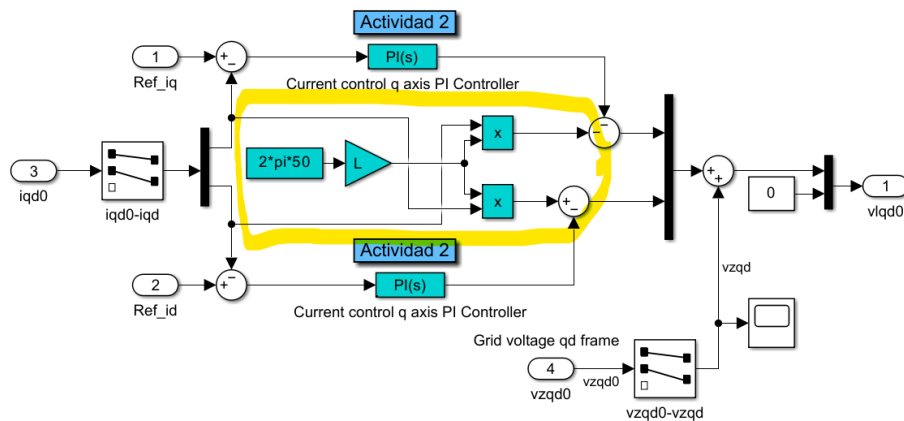


Figure 33: current control entirely in dq0, coupling blocks in yellow

5.2 Modifying the dq disturbances

Using a 3Hz sawtooth signal as reference for i_q (Figure 34), we start to notice the limitations of our control, the PIs are not tuned for quick and wide I_d/I_q changes, the PIs are tuned for reasonable and slow current flows to and from the grid, if this current control was needed for motor control instead of grid following a PI re-tuning should be made.

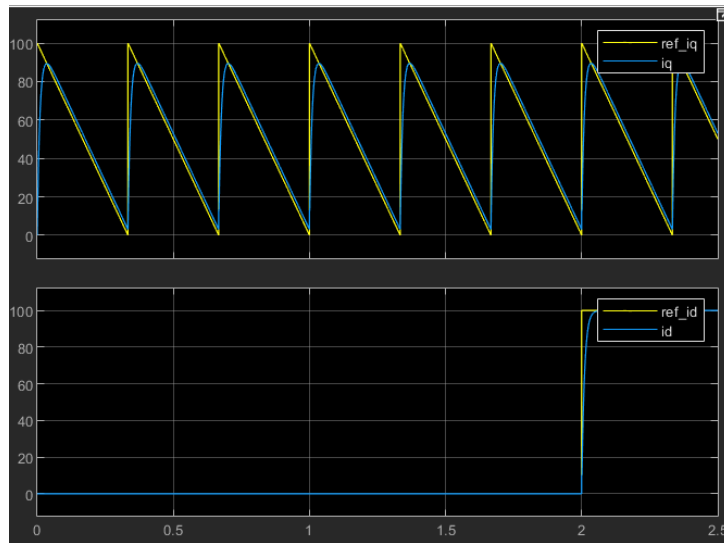


Figure 34: Idq sawtooth signal

5.3 Messing with the PI values

If both PI (K_p and k_i) values are left as they are, the step response looks like Figure 35, both PIs have a neat no overshoot setting time of 10ms with an static error of less than 0.005%.



Figure 35: Idq references and real values

If the K_i is multiplied by 2, suddenly appears an overshoot of 3%, the setting time decreases down to 6ms and the static error drops to near 0.00006%. Figure 36

By increasing K_p 10 times, the setting time decreases down to 1ms, and we observe the error has also multiplied by 10, the integral part is having issues eliminating that 10x error reaching the steady state much slower showing that weird elbow shape seen in Figure 37.

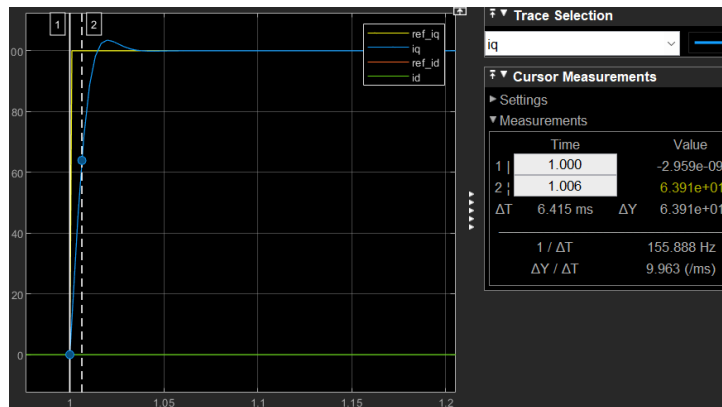


Figure 36: Id reference and real value with $K_i \cdot 2$

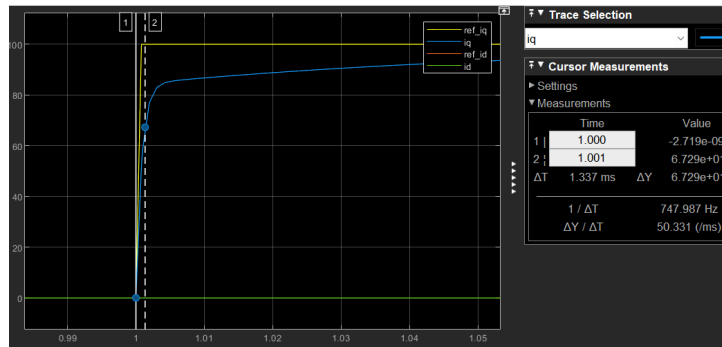


Figure 37: Id reference and real value with $K_p \cdot 10$

5.4 Coupling effect in current

When the plant is correctly inverted inside the current control loop including both coupling terms, we obtain a sharp clean 1st order response for both Id and Iq references. Figure 38.

If both coupling branches are disconnected in the control block, our PI is not well tuned anymore, it shows a 2nd order overshoot against perturbances.

Now when setting a reference value in one of the currents, a disturbance (due to badly identified plant) appears in the other. Figure 39.

Sometimes, in order to simplify the design of the control, the coupling effect is removed entirely leaving it for the PI to deal with the disturbances.

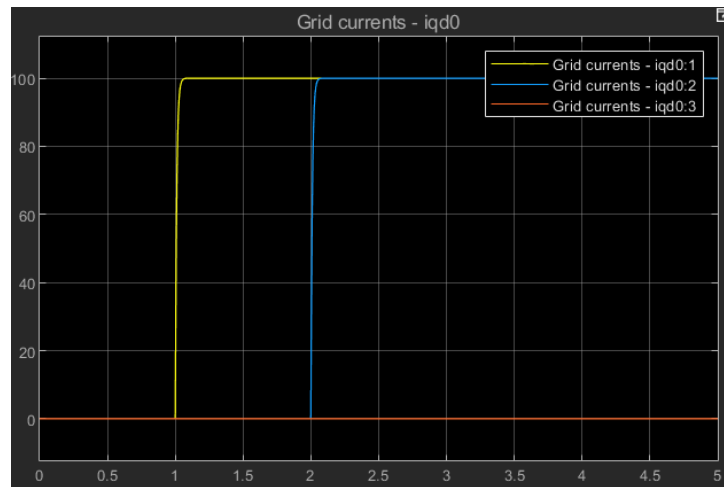


Figure 38: Idq0 with coupling blocks in place

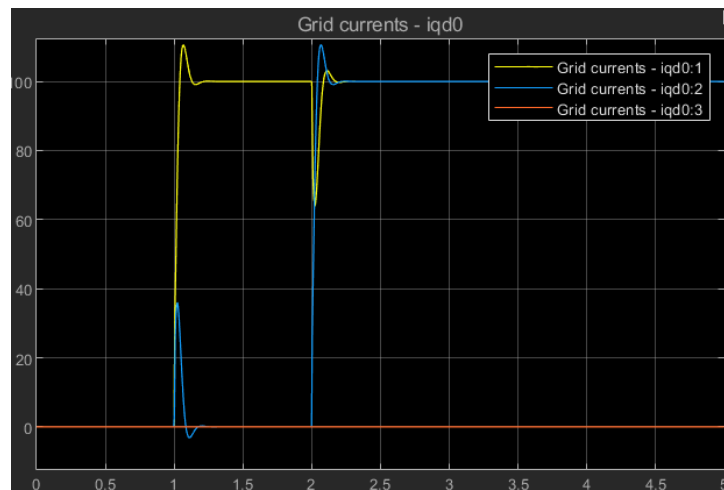


Figure 39: Idq0 without coupling blocks

6 ACTIVE AND REACTIVE POWER TRANSFER

Opening "Model4 Refcalculation1.slx" and "Model4 Refcalculation2.slx" in simulink and discussing the following aspects.

6.1 Changing P and Q setpoints

The main difference between both simulink models is the PQ control loop, in "Model4 Refcalculation1.slx" there is no feedback, on the other hand in "Model4 Refcalculation2.slx" there is a PI in each P and Q closed loops. Figure 40.

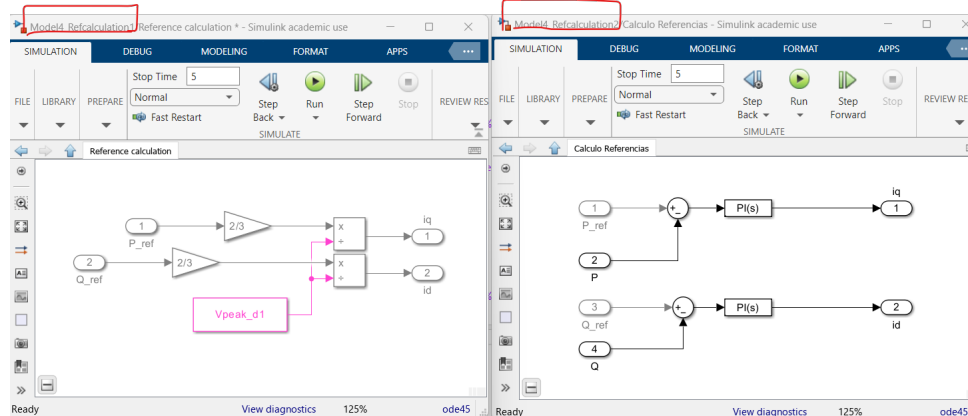


Figure 40: Both models PQ reference to Idq simulink blocks

By not including a PI control for the power setpoints in "Model4 Refcalculation1.slx", we cannot design nor control the desired dynamic response, specially against disturbances and/or system stationary errors.

When punishing our simulation by introducing thermal losses Figure 41 in the converter, the power setpoint has now an error, as there is no feedback in place, the controller would continue to happily deliver the wrong P and Q. Figure 42

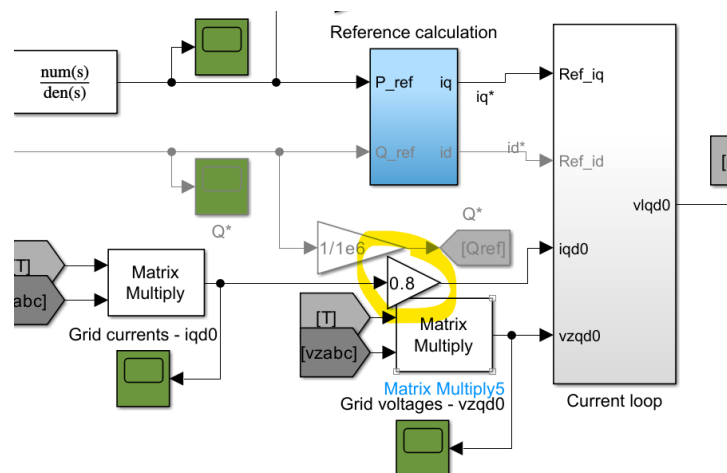


Figure 41: Introducing error in Idq0 feedback

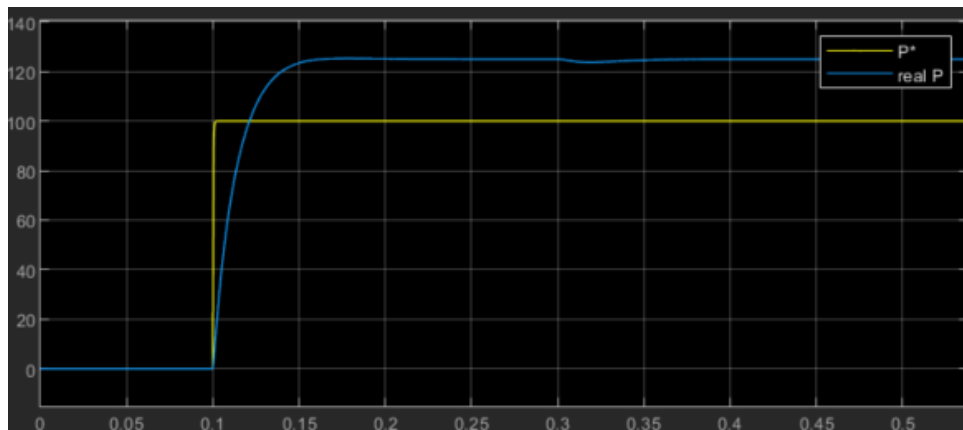


Figure 42: P and P* no PI control

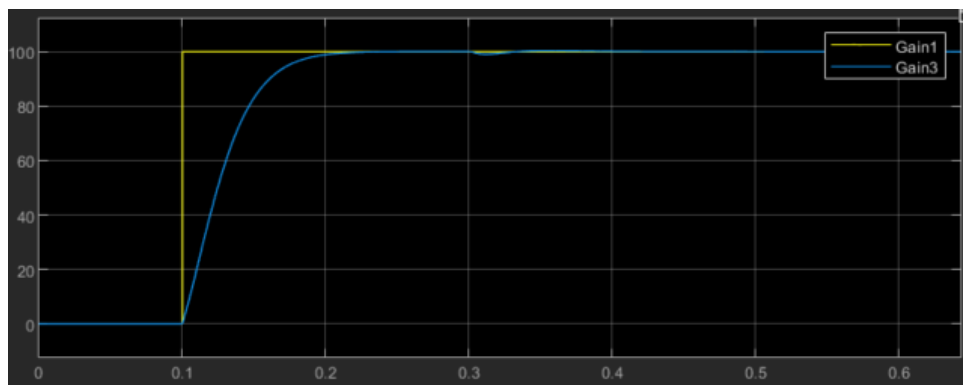


Figure 43: P and P* with PI control

If the same thermal losses are included in "Model4 Refcalculation2.slx", the PI deals with the error, and after a short transient, the intended P and Q setpoints are reached. Figure 43. Modifying K_p and K_i we could tailor the system dynamic response to suit our needs.

7 COMPLETE MODEL

7.1 Overview

Created using the blocks from previous simulations, they all fit together to create a fully functional power converter. Figure 44.

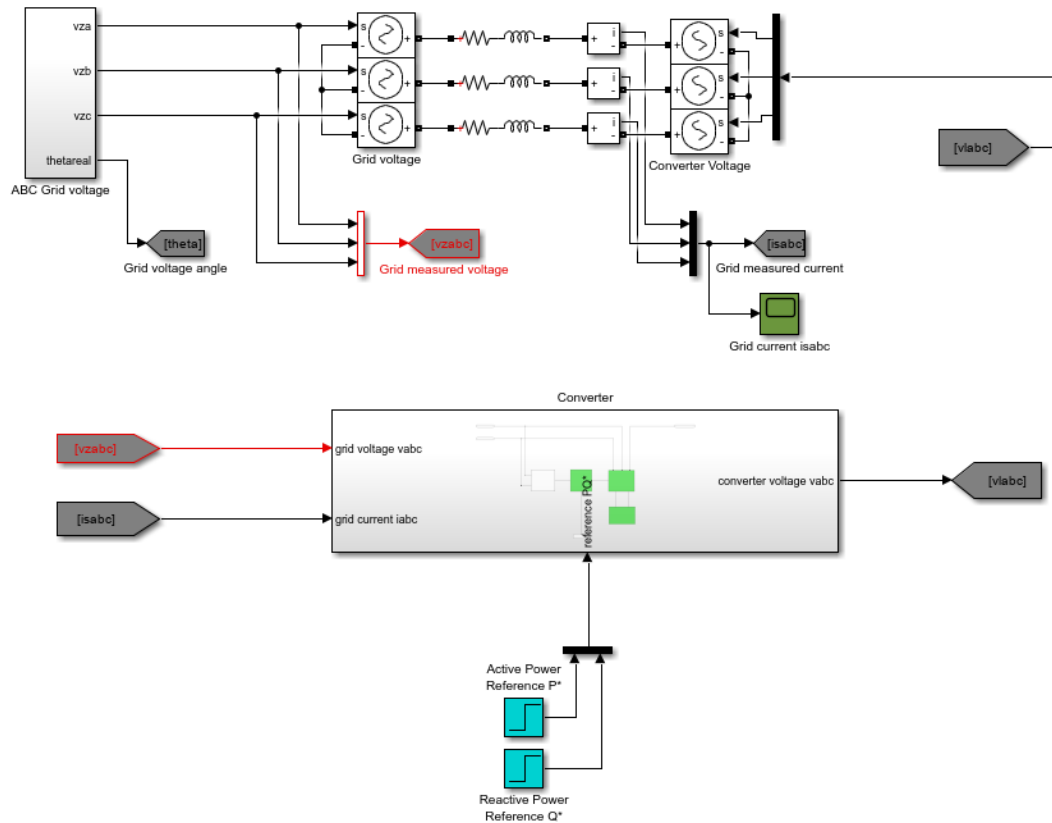


Figure 44: full model with current control and PQ control loops

Our converter uses grid voltages and currents in abc format as inputs. From those inputs the converter estimates the grid angle and power transfer. It also has voltage as the output, with this voltage phase and amplitude it controls the power transfer between itself and the grid.

All clarke and park transforms are contained when needed within each subsystem block.

- The power references PQ.
- The current loop in Idq.
- The phase locked loop (PLL) block.

The diagram illustrates a control system for a three-phase inverter, consisting of the following main blocks and signal flows:

- Inputs:**
 - grid voltage vabc** and **grid current iabc**: These signals are fed into the **from VI to PQ translator** block.
 - reference PQ***: This signal is fed into the **Power to current control loop** block.
- from VI to PQ translator**: This block converts the grid voltage and current signals into **grid PQ** (active power) and **grid Q** (reactive power) signals.
- Power to current control loop**: This block takes the **grid PQ** and **reference PQ*** as inputs and outputs a **reference i_{dq}^*** signal.
- Current control loop**: This block receives the **reference i_{dq}^*** and the **grid vabc** signal. It also receives feedback signals: **iabc** (grid current) and **vabc** (grid voltage). It outputs the **estimated grid voltage angle** and a **reference i_{dq}^*** signal to the PLL block.
- PLL (Phase-Locked Loop)**: This block receives the **estimated grid voltage angle** and outputs the **grid v $_{dq0}$** signal.
- Feedback and Control Signals:**
 - The **grid v $_{dq0}$** signal is fed back into the **Current control loop**.
 - The **grid v $_{dq0}$** signal is also fed into the **Power to current control loop**.

Figure 45: detail f the converter subsystem

When applying the same reference steps we have been using in the last simulations, we observe the response from the converter to be of first order with no overshoot and about 50ms rise time. Figure 46

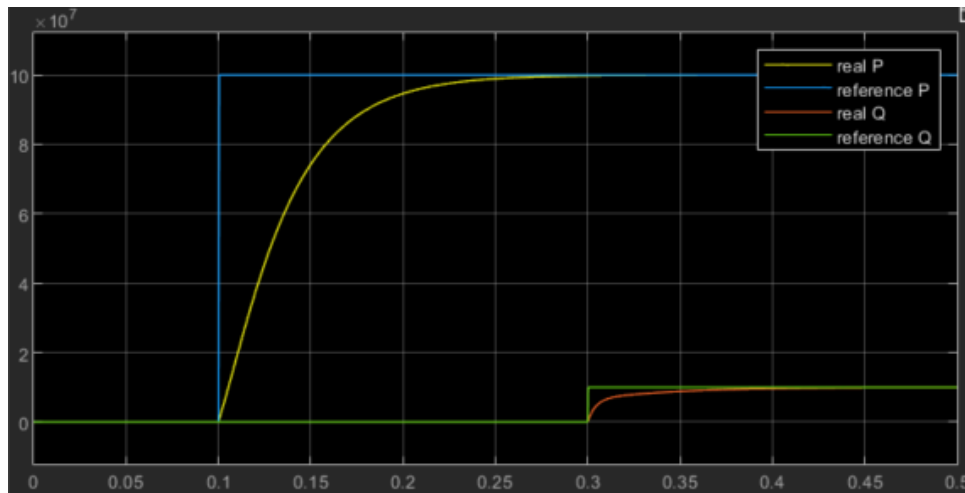


Figure 46: P and Q references and real measurements

Those PQ steps result in the following current references: Figure 47. Also first order with a similar rise time.

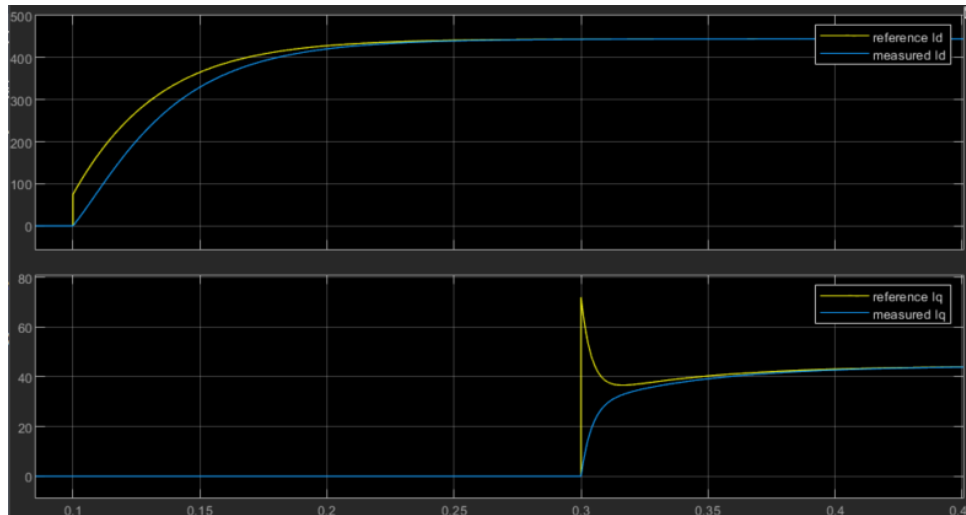


Figure 47: detail f the converter subsystem

The resulting current waves flowing from the converter to the grid in a b c format look correct as well Figure 48

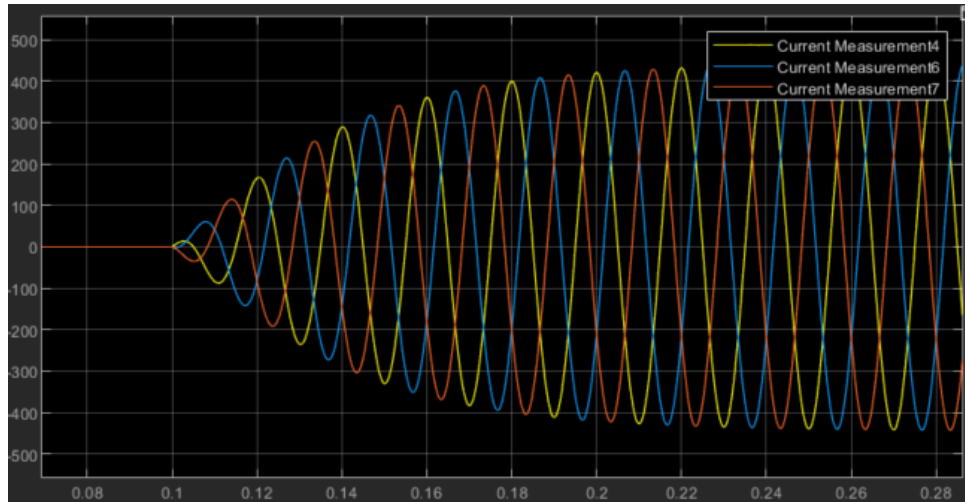


Figure 48: detail f the converter subsystem

8 CODE

Code available in **this Github repo**