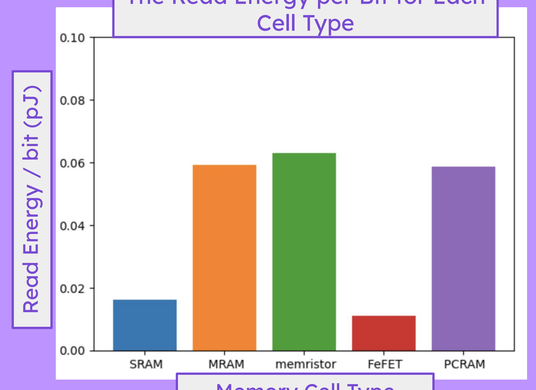
Compare your Memory Technologies with NVMExplorer: Story Mode

Javier Gutierrez Bach '26
Professor Pentecost

Method & Tools:

This framework is used to visualize outputs from NVMExplorer. It is based on Jupyter Notebook and works with the Python libraries pandas, numpy, ipywidgets and matplotlib. It provides toggles for the users to customize the data being displayed.

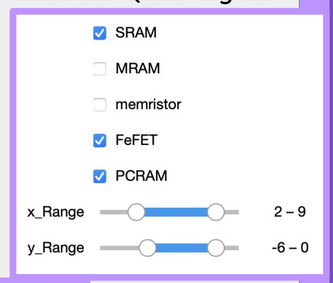
The Read Energy per Bit for Each Cell Type

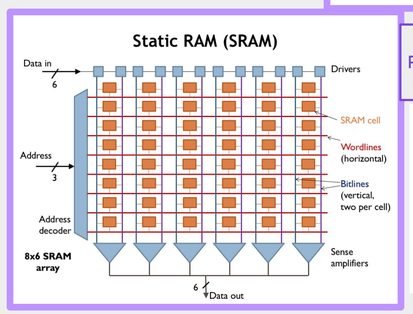


This metric shows us how much energy is required to access and read a single bit from a given memory technology.

Utilization:

User would replace the sample file with their own results in a csv format. They can replace variable names on desired graph to plot your data, or copy the sample code to plot at unrepresented variable. Then, you can analyze patterns by toggling on different memory technologies. There are also range features to change the graph view to focus on specific data points. The Story Mode Framework comes in a three chapter cross-stack narrative: technology specific information (see figure above), array level statistics under generic workload, and a comparison between common traffic patterns (graph processing, DNNs and spec).





NVMExplorer Repository with Source Code and Story Mode

Background:

What are eNVMs?

Embedded Non-Volatile Memories: Memory technologies on the chip that will retain information after they are turned off. Proposed to overcome SRAM and DRAM limitations on storage density, latency and energy efficiency.

NVMExplorer?

Open source design space exploration framework which simulates eNVM behavior and provides data on their performance in latency, power, endurance when used for different traffic patterns (read/write accesses).

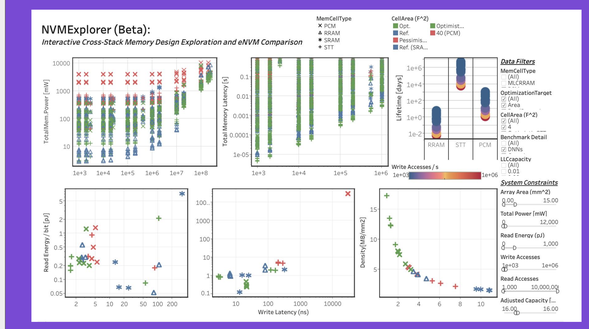
Terminal Output for NVMExplorer

```
Retrieved Array-Level Results;
Reported Results; Evaluation C
Experiment Name: default
Read Latency (ns): 0.659354
Read BW (GB/s): 22.125000
Write Latency (ns): 150.381000
Write BW (GB/s): 0.051987
Read Energy (pJ): 3.756000
Write Energy (pJ): 8.981000
Leakage Power (mW): 21.368000
Area (mm^2): 0.177607
Area Efficiency (percent): 43.
Retrieved Array-Level Results;
Reported Results; Evaluation C
```

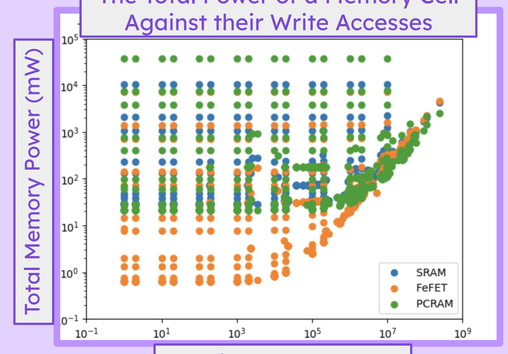
Motivation:

NVMExplorer data is displayed on the terminal in a cluttered manner and a Tableau interface with no guidance. Tutorial materials are needed to have visualizations be more user-friendly, so a visualization framework allowing for easy interpretation of the data was needed. This project provides a platform to guide users through data analysis to identify efficient memory solutions.

Tableau Desktop Interface



The Total Power of a Memory Cell Against their Write Accesses

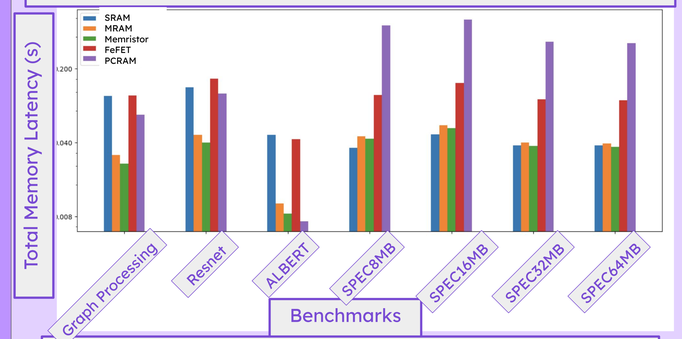


The power refers to how much energy per second is used by a cell. Write accesses are when the computer overwrites the value of a bit in a memory cell.

Evaluation:

The story order is imperative on understanding the data, and the real time graph options allow the viewer to lend focus to specific data ranges. This tool becomes a facilitator for system designers to answer their own research questions regarding memory cell performance in various applications.

The Total Memory Latency for Different Benchmarks (Traffic Patterns)



Each benchmark represents a common type of workload. Resnet does image classification, ALBERT is a language model, SPEC is common scientific computations, and finally graph processing. The latency is how long the software is waiting for all required bit reads and writes to occur.

A disadvantage of this tool is that sometimes it requires additional software development to customize the visualizations to new data; moreover, in the future I want to make the program a bit more flexible and user friendly. Now, it is YOUR turn to find out which memory technology is best suited for your projects by visualizing your NVMExplorer data.

References:

[1] X. Dong, C. Xu, Y. Xie, and N. P. Jouppi, "Nvsim: A circuit-level performance, energy, and area model for emerging nonvolatile memory," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,

[2] L. Pentecost, A. Hankin, M. Donato, M. Hempstead, G.-Y. Wei, and D. Brooks, "Nvmexplorer: A framework for cross-stack comparisons of embedded non-volatile memories," in 2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)

[3] C. Terman, *Static RAM*. M.I.T. Department of Electrical Engineering and Computer Science , 2017.