Binary and decimal counter

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Laboratory exercise number:

Lab. 05

Laboratory exercise name:

Binary and Decimal counter

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| Names: | Roll Number | Date |
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Lab description:

The purpose of this laboratory is to learn how program an FPGA using VHDL with the architecture “dataflow” using the skills learnt in class. Recycling the code from previous labs, the implementation of the clocks using the one inside the FPGA the project must be a counter from 0 to F or 0 to 9 depending of the desired selection.

The material used was:

Nexys 3 by Digilent for the FPGA

ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

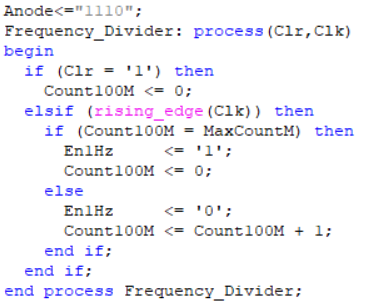
Schematics, block diagrams and/or timing diagrams:

The following table shows the behavior of the counter, Q being the counter. The enable is just set to 1 every time the 100MHz clock reach it’s limit. Every time Q reach 9 or F depending of the base (user selects the base with a switch), it will reset to 0.

|  |  |  |  |
| --- | --- | --- | --- |
| Clk100MHz | Enable | Rst | Q |
| X | X | 1 | 0 |
| 0 | 0 | 0 | Q |
| ↑ | 0 | 0 | Q |
| ↑ | 1 | 0 | Q+1 |

The code is shown in the following images:

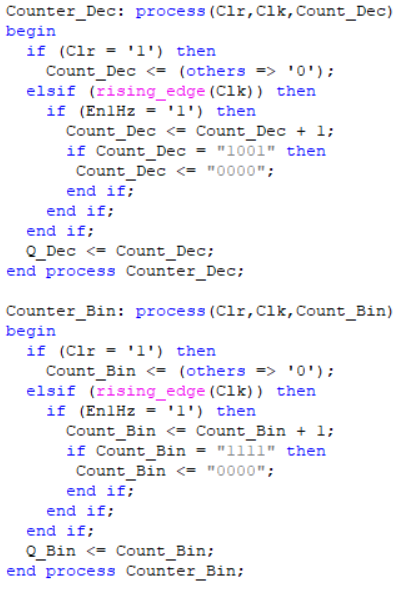
Image 1.1



Frequency divider

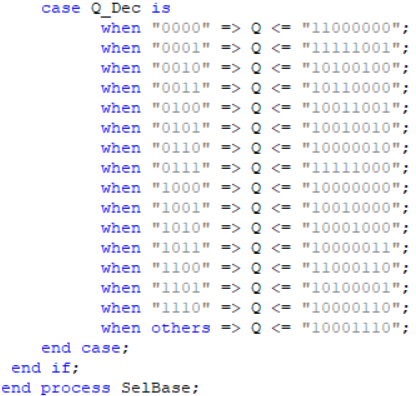
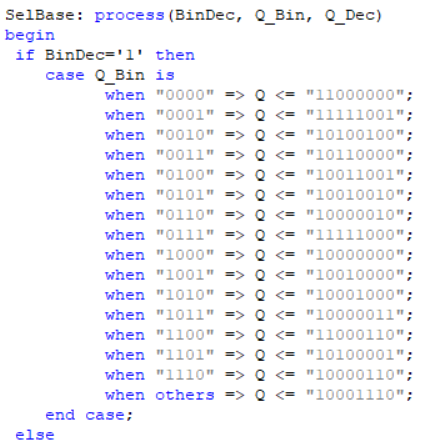
Code for counting when the clock reaches its limit

Image 1.2



Hexadecimal and Decimal counter

Image 1.3



Selector and display output

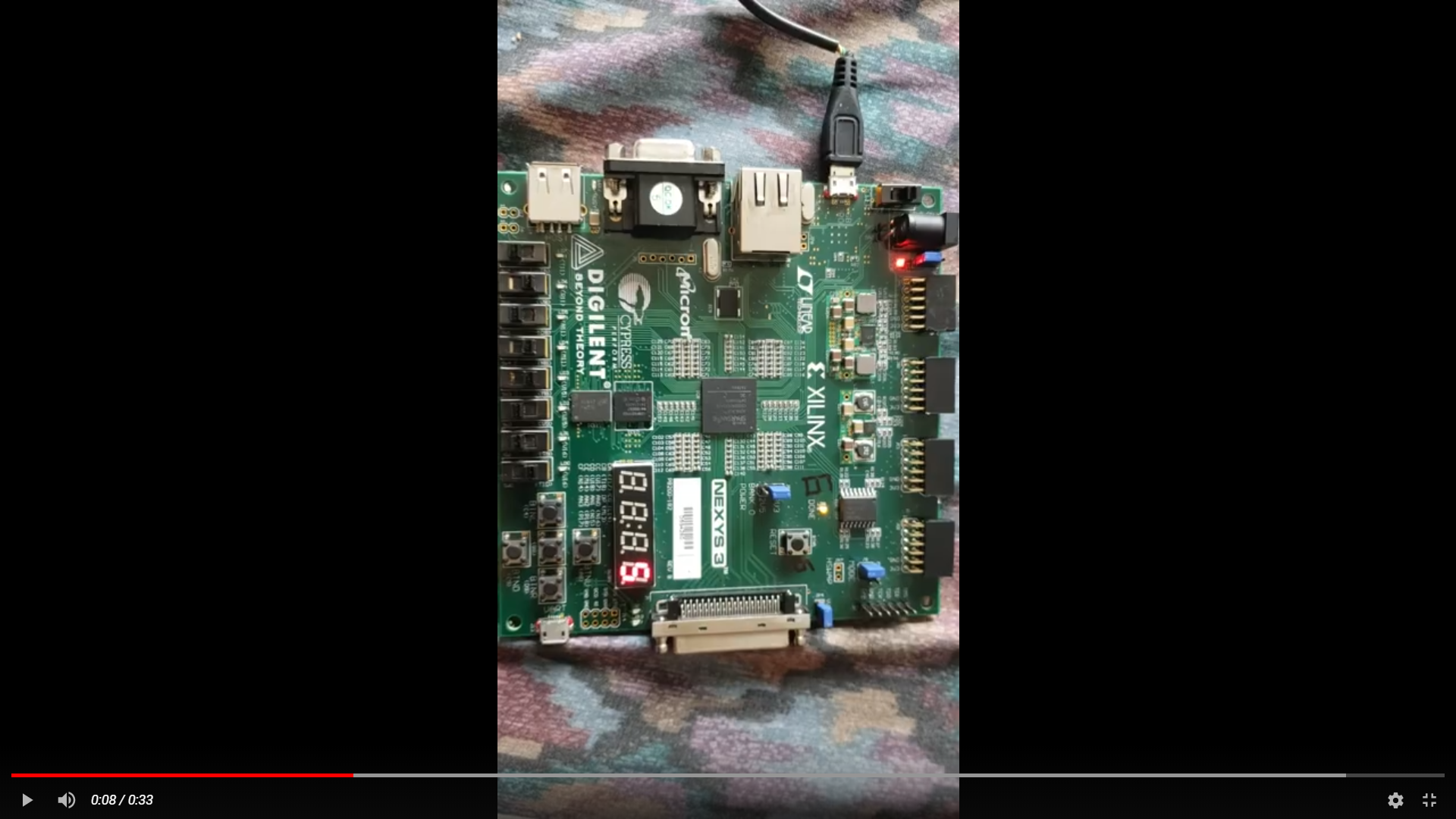
Results obtained:

The result was a successful counter from hexadecimal and decimal to digital displayed in the FPGA using 7 segment display as output and a switch for the base.

Evidence:

Video: https://youtu.be/mSbyxkPR0gw

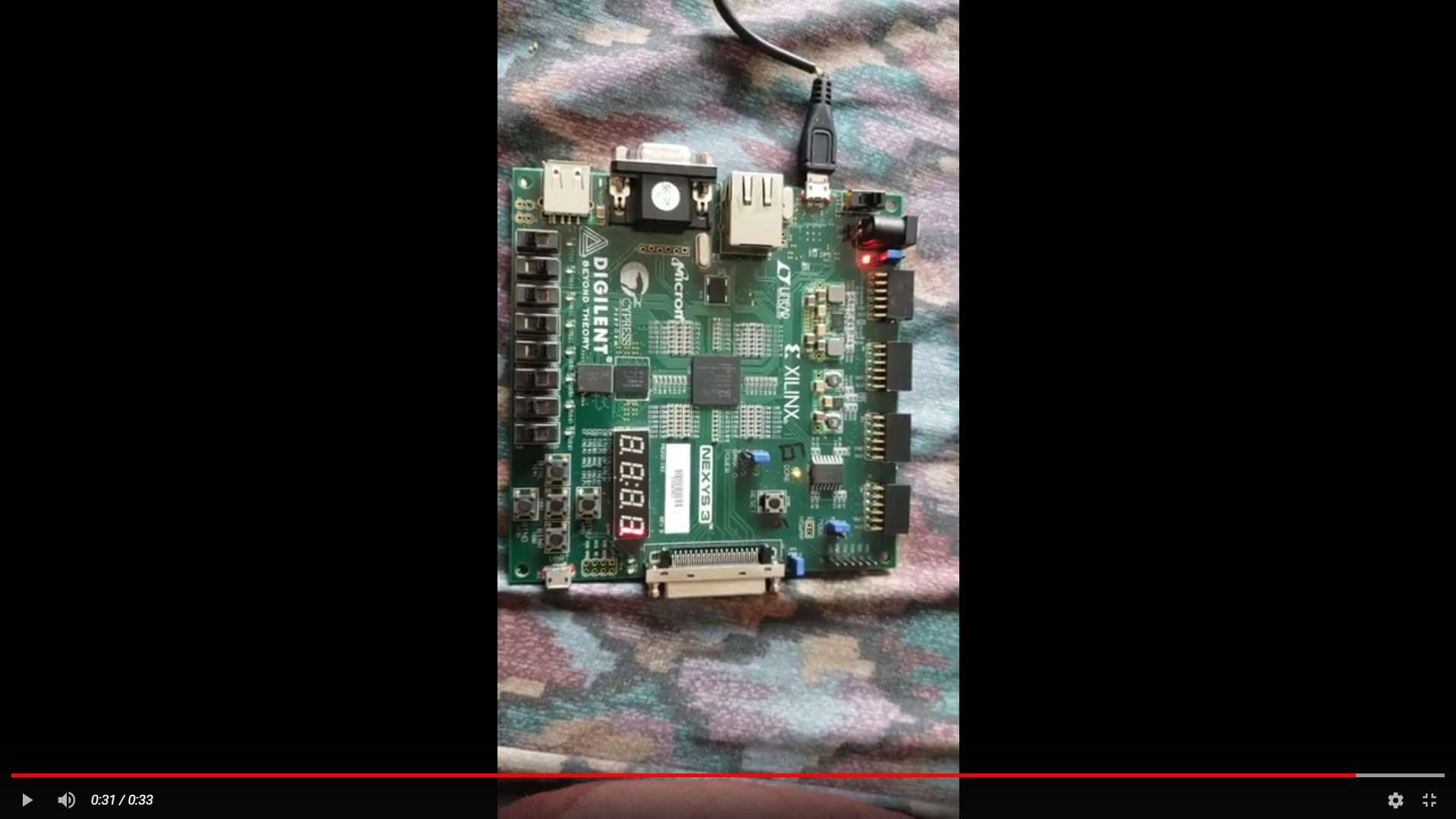
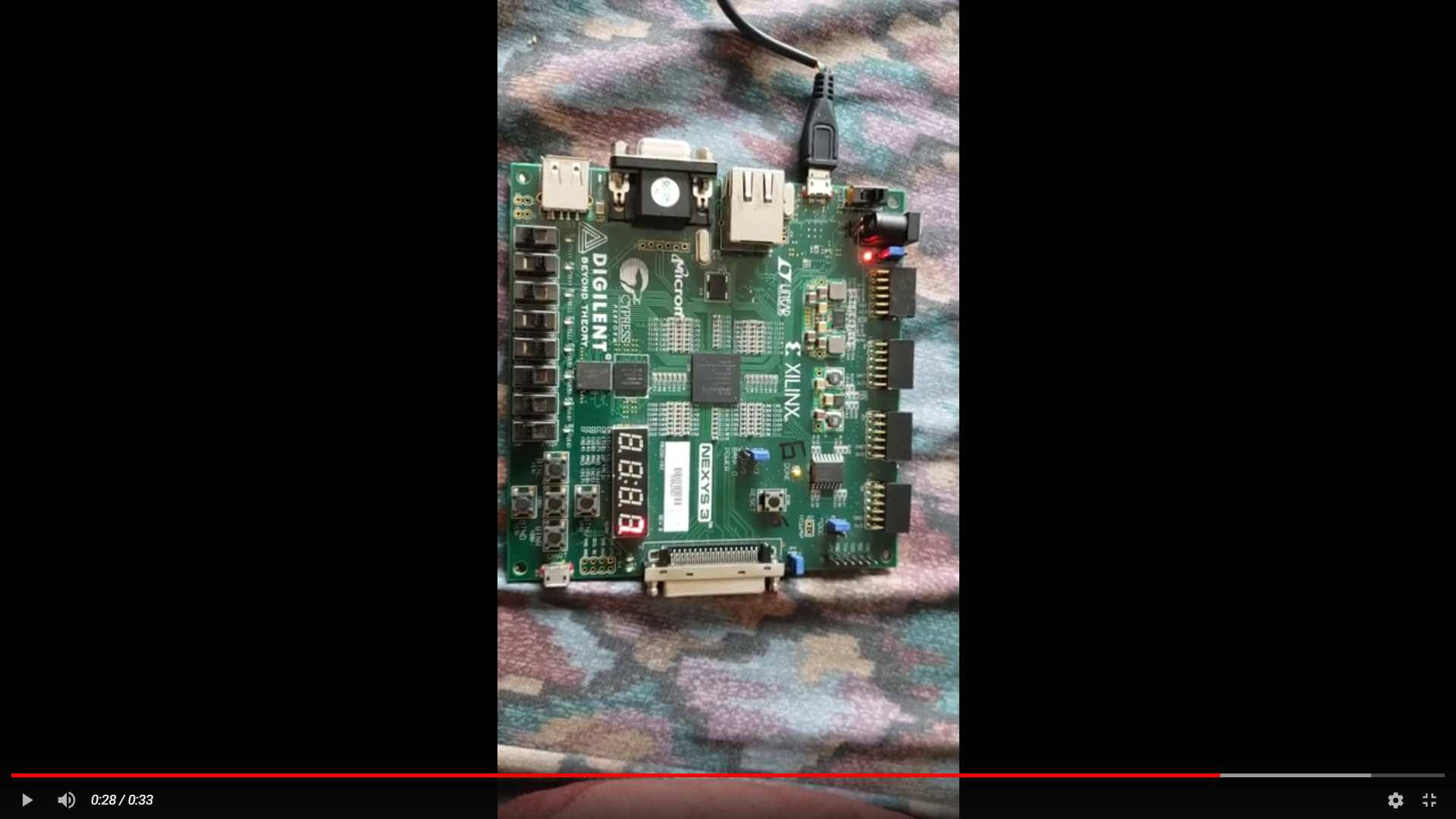
Case 1: Case 2:



Case 3: Case 4:



Case 5: Case 6:



Conclusions:

The counter, divider and selector are a great example to show that is better to make the code by parts with different process. Also, the Nexys has a lot of tools to test circuits to know if your logic is right before making the final circuit.

Problems encountered:

The clock is not displayed in the board and you have to look for the reference manual and the syntax may be confusing for the counters.