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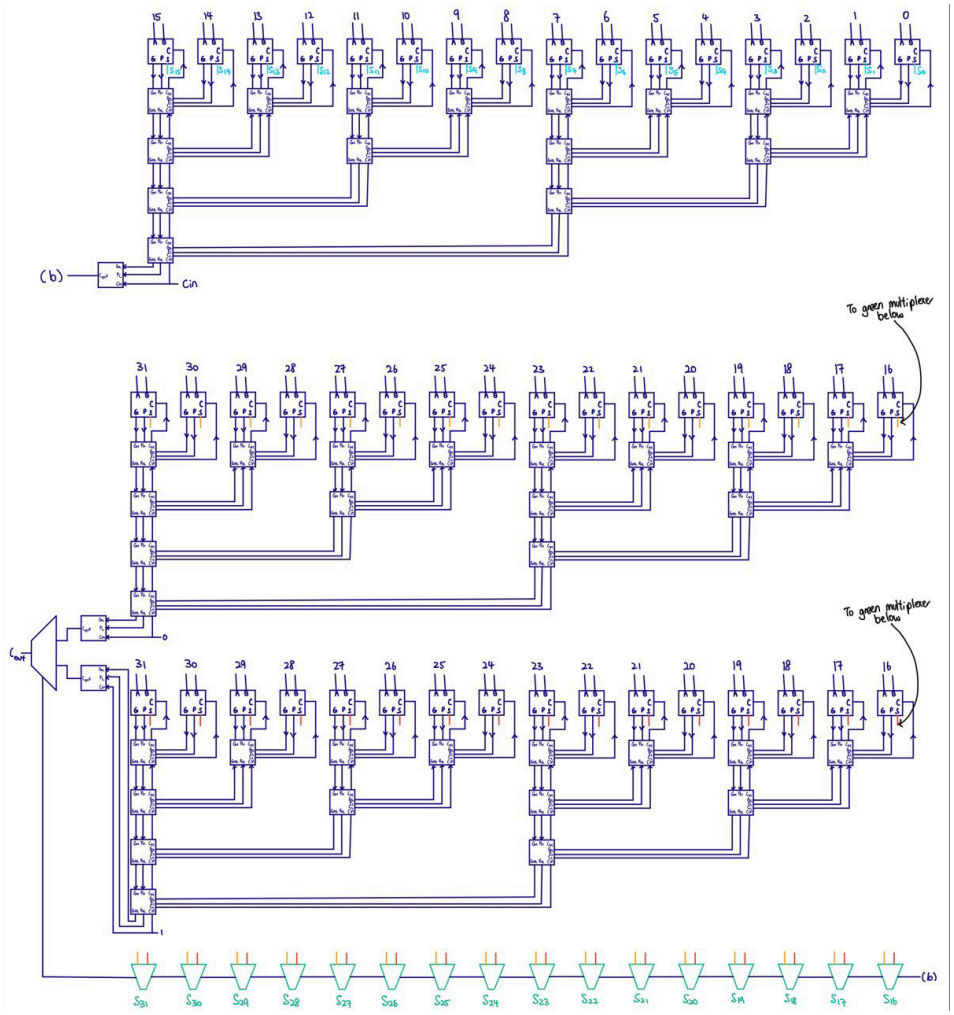
The structure of the adder that we adopted is a combination of the variable carry select adder, as well as the carry lookahead adder. Within our JSIM file we utilized recursion to create the subcircuits for the G, P and C outputs of each “block”, as we noticed a reoccurring pattern of logic devices within our design. Furthermore, buffers were utilized to minimize the load-dependent delays. The diagram of our optimized 32-bit adder is as shown below:



Our group chose the **16th-bit output for the CNF**, aand the fastest timing that our adder can pass is 3ns, with it being at **2.795ns**.