



A review of recent MOSFET threshold voltage extraction methods

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Abstract

The threshold voltage value, which is the most important electrical parameter in modeling MOSFETs, can be extracted from either measured drain current or capacitance characteristics, using a single or more transistors. Practical circuits based on some of the most common methods are available to automatically and quickly measure the threshold voltage. This article reviews and assesses several of the extraction methods currently used to determine the value of threshold voltage from the measured drain current versus gate voltage transfer characteristics. The assessment focuses specially on single-crystal bulk MOSFETs. It includes 11 different methods that use the transfer characteristics measured under linear regime operation conditions. Additionally two methods for threshold voltage extraction under saturation conditions and one specifically suitable for non-crystalline thin film MOSFETs are also included. Practical implementation of the several methods presented is illustrated and their performances are compared under the same challenging conditions: the measured characteristics of an enhancement-mode n-channel single-crystal silicon bulk MOSFET with state-of-the-art short-channel length, and an experimental n-channel a-Si:H thin film MOSFET. © 2002 Elsevier Science Ltd. All rights reserved.

1. Introduction

The threshold voltage (V_T) is a fundamental parameter for MOSFET modeling and characterization [1–6]. This parameter, which represents the onset of significant drain current flow, has been given several definitions [7–9], but it may be essentially understood as the gate voltage value at which the transition between weak and strong inversion takes place in the MOSFET channel.

There exist numerous methods to extract the value of threshold voltage [10–41] and various extractor circuits have also been proposed [42–44] to automatically measure this parameter. Recently three books [1–3] and three articles [4–6] have reviewed and scrutinized different available methods.

The greater part of the procedures available to determine V_T are based on the measurement of the static transfer drain current versus gate voltage (I_D-V_g) characteristics [10–35] of a single transistor. Most of these I_D-V_g methods use the strong inversion region [10–27], while only a few consider the weak inversion region [28–31]. Extraction is mostly done using low drain voltages so that the device operates in the linear region [10–33]. However, V_T extraction with the device operating in saturation is also frequently carried out [34,35].

A common feature present of most V_T extraction methods based on the I_D-V_g transfer characteristics is

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the strong influence of the source and drain parasitic series resistances and the channel mobility degradation on the resulting value of the extracted V_T . This situation is highly undesirable because the correct value of the extracted V_T should not depend on parasitic components nor mobility degradation. In order to eliminate the influence of these unwanted effects **some methods have been proposed which are based on measuring capacitance as a function of voltage** [36,37]. However **these C-V methods have the disadvantage of requiring elaborate high-resolution equipment to measure the small capacitances present in MOSFETs**, particularly in very small geometry state-of-art devices. Other approaches to eliminate the influence of parasitic series resistances are based on measuring the I_D-V_g transfer characteristics of various devices having different mask channel lengths [38,39], or on measuring several devices connected together [40,41]. Although such multi-device approaches offer interesting solutions to this problem, they require additional work and the availability of several supplementary special devices. Another recently proposed method that requires repeated measurements is **based on a proportional difference operator** [26,27].

The extraction of V_T in non-crystalline MOSFETs is **more conveniently performed using the drain current in saturation**, considering that these devices present much smaller currents than single-crystalline devices. Amorphous and polycrystalline thin film transistors (TFTs) introduce the additional difficulty that the saturation drain current in strong inversion is usually modeled by a power law with an exponent which can differ from 2 [45,46]. Because of this behavior, using conventional V_T extraction methods developed for single-crystal devices will generally produce values of V_T that are unacceptable or at least not very accurate. Therefore the extraction method must be capable of extracting the value of the unknown power-law exponent parameter and take it into consideration in the extraction process. To that end, methods have been proposed that are specific for non-crystalline thin MOSFET TFTs [45,46] and thus allow to extract their threshold voltage correctly.

This article will review and scrutinize the following existing I_D-V_g methods for extracting V_T in single-crystal MOSFETs, biased in the *linear region*: (1) **constant-current (CC) method**, which defines V_T as the gate voltage corresponding to a certain predefined practical constant drain current [1–6,10,11]; (2) **extrapolation in the linear region (ELR) method**, which finds the gate voltage axis intercept of the linear extrapolation of the I_D-V_g characteristics at its maximum first derivative (slope) point [1–6]; (3) **transconductance linear extrapolation (GMLE) method**, which finds the gate voltage axis intercept of the linear extrapolation of the g_m-V_g characteristics at its maximum first derivative (slope) point [19,20]; (4) **second derivative (SD) method**, which determines V_T at the maximum of the SD of I_D with

respect to V_g [12]; (5) **ratio method (RM)**, which finds the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance [13–18]; (6) **transition method** [33]; (7) **integral method** [32]; (8) **Corsi function method** [21]; and (9) **second derivative logarithmic (SDL) method**, which determines V_T at the minimum of the SD of $\log(I_D-V_g)$ [31]; (10) **linear cofactor difference operator (LCDO) method**, and (11) **non-linear optimization** [23,24].

This article will also review the following two methods to extract the V_T of single-crystalline MOSFETs, operating in the *saturation region*: (1) extrapolation in the saturation region (ESR) method, which finds the gate voltage axis intercept of the linear extrapolation of the $I_D^{0.5}-V_g$ characteristics at its maximum first derivative (slope) point [1,2]; and (2) G_1 function extraction method [34,35].

Finally, we will review and discuss some amorphous TFT specific procedures which have been recently proposed to extract the threshold voltage of these non-crystalline devices [45,46].

2. Extraction from the I_D-V_g curve of MOSFETs biased in the linear region

In order to critically assess and compare the different linear region extraction methods reviewed here, we will apply them all to extract the value of the threshold voltage from the measured transfer characteristics of a state-of-the-art bulk single-crystal silicon enhancement-mode n-channel MOSFET with a 5 μm mask channel width, a 0.18 μm mask channel length, and a 32A gate oxide thickness. For this group of methods the device is biased to operate in the linear regime by applying a drain voltage of 10 mV. Fig. 1 presents the output characteristics of this device for general reference purposes.

2.1. Constant-current method

The CC method [1–6] **evaluates the threshold voltage as the value of the gate voltage, V_g , corresponding to a given arbitrary constant drain current, I_D , and $V_d < 100 \text{ mV}$** . A typical value [20] for this arbitrary constant drain current is $(W_m/L_m) \times 10^{-7}$, where W_m and L_m are the mask channel width and length, respectively. This method is widely used in industry because of its simplicity. The **threshold voltage can be determined quickly with only one voltage measurement**, as shown in Fig. 2. In spite of its simplicity, this method has the severe **disadvantage of being totally dependent of the arbitrarily chosen value of the drain current level**. This is evident by the results in Fig. 2, where different gate voltages can be taken at different drain current values to represent the threshold voltages.

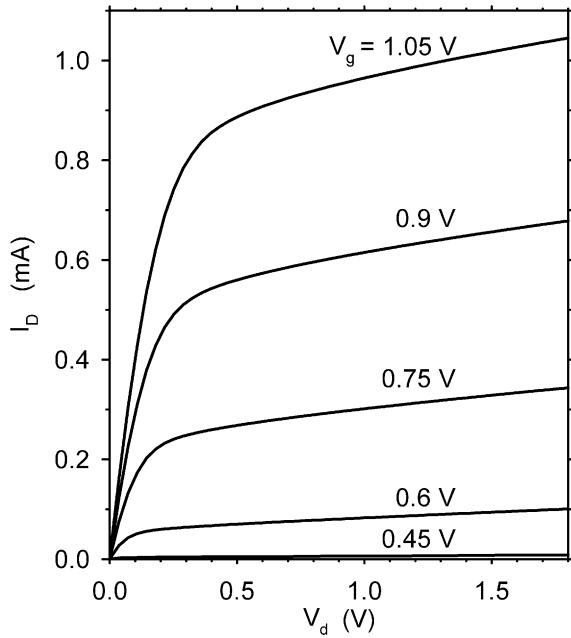


Fig. 1. Measured I_D - V_d output characteristics at five values of gate bias for the test bulk single-crystal n-channel MOSFET with 5 μm mask channel width and 0.18 μm mask channel length.

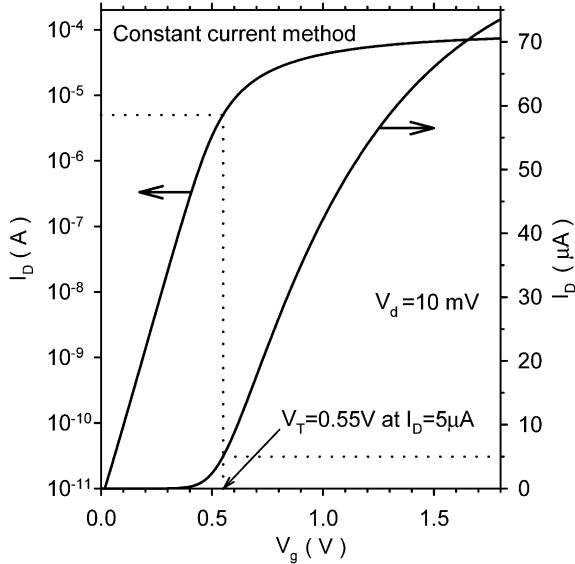


Fig. 2. CC method implemented on the I_D - V_g transfer characteristics of the test bulk device measured at $V_d = 10$ mV. This method evaluates the threshold voltage as the value of the gate voltage corresponding to a given arbitrary constant drain current.

Recently Zhou and his group have proposed [10,11] an improvement to the CC method. It consists on de-

fining the previously arbitrary drain current level used to define the threshold voltage at the drain current where $d^2 I_D / dV_g^2$ presents a maximum. This amounts to a combination of the CC method and the second-derivative method, which will be presented latter.

2.2. Extrapolation in the linear region method

The ELR method [1–6] is perhaps the most popular threshold-voltage extraction method. It consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the linear extrapolation of the I_D - V_g curve at its maximum first derivative (slope) point (i.e. the point of maximum transconductance, g_m), as illustrated in Fig. 3. The value of V_T is calculated by adding $V_d/2$ to the resulting gate-voltage axis intercept, which for the device at hand happens to be 0.51 V. The main drawback of this otherwise useful method is that the maximum slope point might be uncertain, because the I_D - V_g characteristics can deviate from ideal straight line behavior at gate voltages even slightly above V_T , due to mobility degradation effects and to the presence of significant source and drain series parasitic resistances [2]. Therefore, the threshold voltage value extracted using this method, often referred to as the extrapolated V_T , can be strongly influenced by

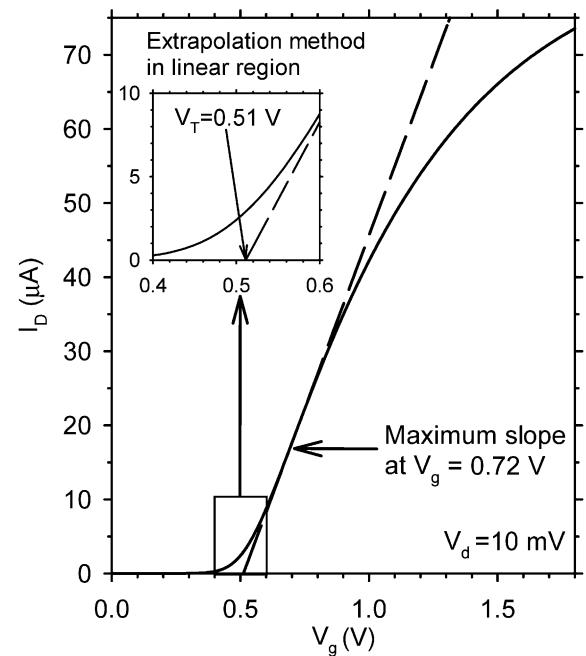


Fig. 3. ELR method implemented on the I_D - V_g characteristics of the test bulk device measured at $V_d = 10$ mV. This method consists of finding the gate-voltage axis intercept (i.e., $I_D = 0$) of the linear extrapolation of the I_D - V_g curve at its maximum slope point.

parasitic series resistances and mobility degradation effects.

2.3. Transconductance extrapolation method in the linear region

A seldom used method is the transconductance extrapolation method in the linear region (GMLE) which was proposed in 1998 [19,20]. This method suggests that the threshold voltage corresponds to the gate voltage axis intercept of the linear extrapolation of the $g_m - V_g$ characteristics at its maximum first derivative (slope) point. This method is based on the following arguments when the device is biased in the linear region. (1) In weak inversion, the transconductance depends exponentially on gate bias; (2) For strong inversion, if the series resistance and mobility degradation are negligible, the transconductance tends to a constant value; (3) The transconductance decreases slightly with gate bias due to the series resistance and mobility degradation; (4) In the transition region between weak and strong inversion, the transconductance depends linearly on gate bias. Fig. 4 presents the application of this method to the $g_m - V_g$ characteristics producing an apparent value for V_T of only 0.44 V. The following method also based on the

maximum slope of the $g_m - V_g$ characteristics offers a better description of V_T .

2.4. Second-derivative method

The SD method [12], developed to avoid the dependence on the series resistances, determines V_T as the gate voltage at which the derivative of the transconductance (i.e., $dg_m/dV_g = d^2I_D/dV_g^2$) is maximum. The origin of this method can be understood by analyzing the following ideal case of a MOSFET modeled with a simple level = 1 SPICE model, where $I_D = 0$ for $V_g < V_T$ and I_D is proportional to V_g for $V_g > V_T$. Using the previous simplifying assumption, dI_D/dV_g becomes a step function, which is zero for $V_g < V_T$ and has a positive constant value for $V_g > V_T$. Therefore, d^2I_D/dV_g^2 will tend to infinity at $V_g = V_T$. Since for a real device such simplifying assumptions are obviously not exactly true, d^2I_D/dV_g^2 will of course not become infinite, but will instead exhibit a maximum at $V_g = V_T$.

As Fig. 5 indicates, the implementation of this method is highly sensitive to measurement error and noise, because the use of the SD amounts to applying a high-pass filter in the measurement. Notice in this figure that the maximum value of d^2I_D/dV_g^2 occurs at about $V_g = 0.54$ V due to the measurement noise present;

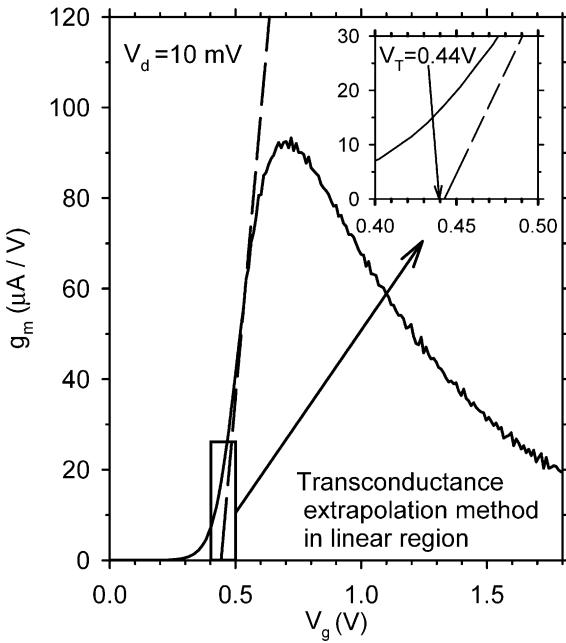


Fig. 4. Transconductance extrapolation method (GMLE) implemented on the $g_m = dI_D/dV_g$ versus V_g characteristics of the test bulk device measured at $V_d = 10$ mV. This method suggests that the threshold voltage corresponds to the gate voltage axis intercept of the linear extrapolation of the $g_m - V_g$ characteristics at its maximum slope point.

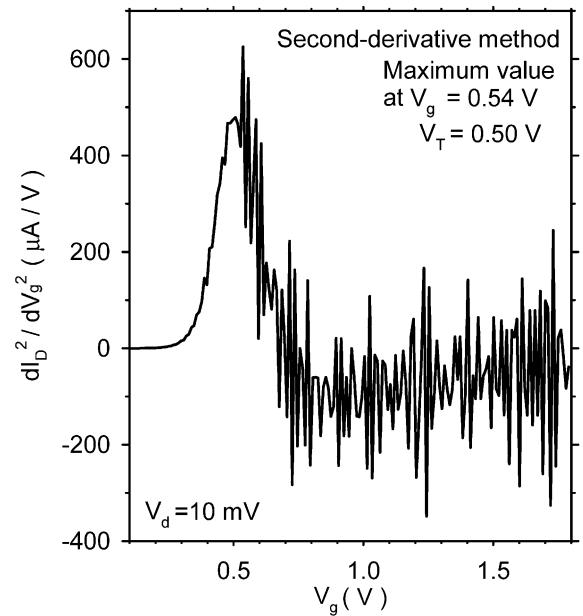


Fig. 5. SD method implemented on the plot of d^2I_D/dV_g^2 versus V_g of the test bulk device measured at $V_d = 10$ mV. This method consists of finding the gate-voltage at which d^2I_D/dV_g^2 exhibits a maximum value.

whereas if the noise is suppressed the maximum appears to be around $V_g = 0.50$ V.

2.5. Ratio method

The RM [13–18], developed to avoid the dependence of the extracted V_T value on mobility degradation and parasitic series resistance, proposes that the ratio of the drain current to the square root of the transconductance ($I_D/g_m^{0.5}$) behaves as a linear function of gate bias, whose intercept with the gate-voltage axis will equal the threshold voltage. This method was originally published independently in 1988 by Jain [13] and by Ghibaudo [14]. Jain demonstrated that if the mobility degradation were negligible, the function $I_D/g_m^{0.5}$ would be independent of parasitic series resistance [13]. On the other hand, Ghibaudo showed that if the parasitic series resistance were negligible, the function $I_D/g_m^{0.5}$ would not depend on mobility degradation [14]. In 1995, Fikry and his coworkers proved [15] that the function $I_D/g_m^{0.5}$ is independent of mobility degradation, parasitic series resistance and velocity saturation effects. The RM was further improved in 2000 [18] to account for a more general mobility degradation model.

Summarizing the RM developments, the drain current I_D in the linear region can be expressed as [1–3]

$$I_D = \frac{W}{L_{\text{eff}}} \mu C_o (V_{GS} - V_T) V_{DS}, \quad (1)$$

where W is the channel width, C_o is the oxide capacitance per unit area, μ is the effective free-carrier mobility, and V_{GS} and V_{DS} are the intrinsic gate-source and drain-source voltages, respectively. The intrinsic voltages can be related to the external gate-source and drain-source voltages (V_g and V_d) by

$$V_{GS} = V_g - I_D R_D \quad (2)$$

and

$$V_{DS} = V_d - I_D (R_S + R_D). \quad (3)$$

Here R_D and R_S represent the drain and source parasitic series resistances, respectively. According to Fikry et al. [15], the velocity saturation effect is imbedded in the following free-carrier mobility model:

$$\mu = \frac{\mu_0}{(1 + \theta(V_g - V_T)) \left(1 + \frac{\mu_0 V_d}{L_{\text{eff}} v_{\text{sat}}} \right)}, \quad (4)$$

where μ_0 is the low-field mobility, θ is the mobility degradation factor due to the vertical field, and v_{sat} is the saturation velocity of the carriers. Using (1)–(4) and the approximation $V_g = V_{GS}$, it can be proved that

$$\frac{I_D}{g_m^{1/2}} = s^{-1/2} (V_g - V_T), \quad (5)$$

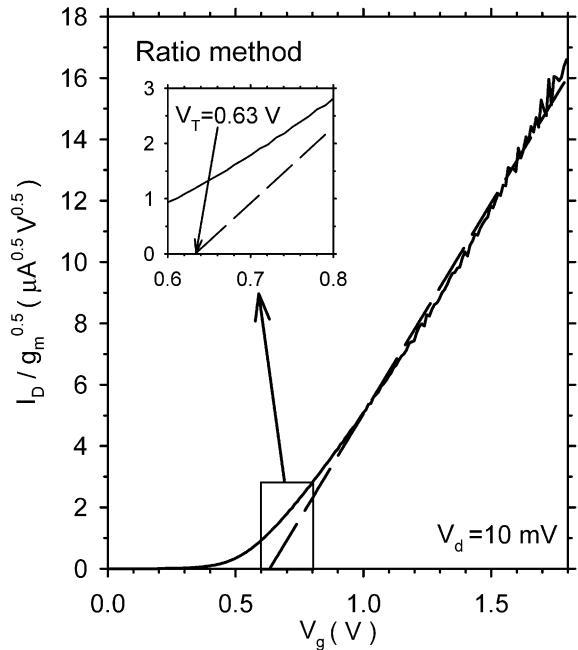


Fig. 6. RM implemented on the plot of the ratio of the drain current to the square root of the transconductance ($I_D/g_m^{0.5}$) versus V_g of the test bulk device measured at $V_d = 10$ mV. This method evaluates V_T from the intercept to the lateral axis of its straight line fit.

where g_m is the transconductance and

$$s = \frac{L_{\text{eff}} - \left(\Delta L_{\text{eff}} - \frac{\mu_0 V_d}{v_{\text{sat}}} \right)}{W \mu_0 C_o V_d}. \quad (6)$$

Then, by plotting the $I_D/g_m^{1/2}$ versus V_g curve the values of V_T and s can be extracted from the intercept and the slope of its straight line fit. Fig. 6 shows the results of applying this method to the present test device. As can be observed, in the present case it is not clear where to do the linear approximation to be extrapolated to the V_g axis to extract the value of V_T . The $I_D/g_m^{1/2}$ versus V_g curve for the present test device shown in Fig. 6 does not appear to totally fulfill this method's assumptions, since it does not clearly behave in the linear manner expected. Therefore, the linear fit shown is just a guess, amidst the evident non-linearity and the noise present, significantly enhanced by dividing the current by the square root of its first derivative (g_m).

2.6. Transition method

This method uses the sub-threshold-to-strong inversion transition region of the MOSFET's transfer characteristics to extract the threshold voltage. It is based on

an auxiliary operator that involves integration of the drain current as a function of gate voltage.

In order to extract V_T , the drain current is measured versus V_g below and above threshold with zero body bias and a small constant value of drain voltage. Next the following function G_1 is numerically calculated from measured data [33]:

$$G_1(V_g, I_D) = V_g - 2 \frac{\int_{V_{gb}}^{V_{ga}} I_D(V_g) dV_g}{I_D}, \quad (7)$$

where V_{gb} and V_{ga} are the lower and upper limits of integration corresponding to gate voltages below and above threshold, respectively.

A plot of G_1 versus $\ln I_D$ should result in a straight line below threshold, where the current is dominated by diffusion and consequently it is predominantly exponential. As soon as $V_g = V_T$ function G_1 should drop abruptly. This is what is observed with the present test device, as revealed in Fig. 7. It can be shown that the maximum value of G_1 corresponds to the threshold voltage of the device [33], which for this case happens to be 0.49 V. It should be noted that parasitic resistance and mobility degradation effects influence the shape of the above-threshold G_1 , but not significantly its maximum value, unless those effects are highly pronounced.

2.7. Integral method

The integral method was developed in [32] to be insensitive to the effect of drain and source parasitic series resistances. It was demonstrated that substituting the

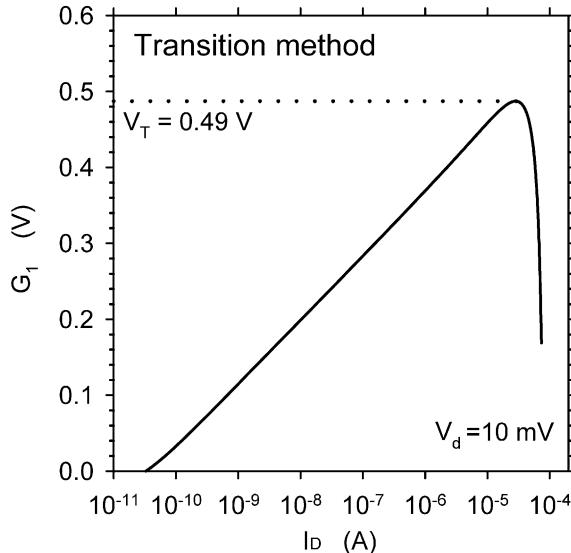


Fig. 7. Transition method implemented on the plot of function G_1 versus I_D of the test bulk device. This method evaluates the threshold voltage from the maximum value of G_1 .

necessary values of voltage and current in an integral function D defined as

$$D(x, y) = \int_0^{y_0} x dy - \int_0^{x_0} y dx, \quad (8)$$

and after substituting and performing algebraic manipulations the following function can be obtained:

$$D_1(V_{gb}, R_m V_{gb}) = \frac{2V_{gb}}{K} + \frac{V_{gb}}{K(V_{max} - V_{gb} - V_T)} + \frac{2(V_{max} - V_T)}{K} \ln \left[1 - \frac{V_{gb}}{V_{max} - V_T} \right], \quad (9)$$

where $V_{gb} = V_{max} - V_g$ and V_{max} is a constant parameter equal to the maximum gate voltage under consideration.

When D_1 is plotted versus V_{gb} , the value of V_T is obtained using a procedure similar to extracting the ideality factor and saturation current of a junction diode, as explained in [47,48]. Fig. 8 illustrates the application of this method to the test device producing a V_T value of 0.51 V. Notice that D_1 also permits the extraction of parameter K . Although this method gives accurate results, is it quite cumbersome to implement.

2.8. Corsi function method

Corsi and coworkers have proposed [21] a method based on the following function:

$$\text{Beta} = \frac{I_D}{V_g - V_p}, \quad (10)$$

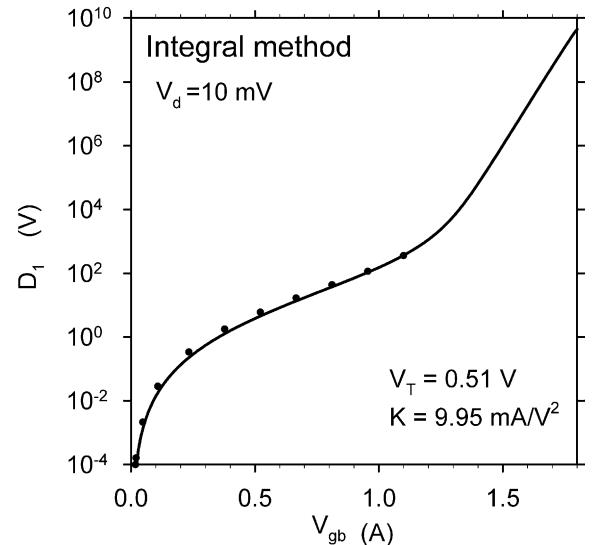


Fig. 8. Integral method implemented on the plot of function D_1 versus V_{gb} of the test bulk device. This method evaluates the threshold voltage by doing a curve fitting of function D_1 .

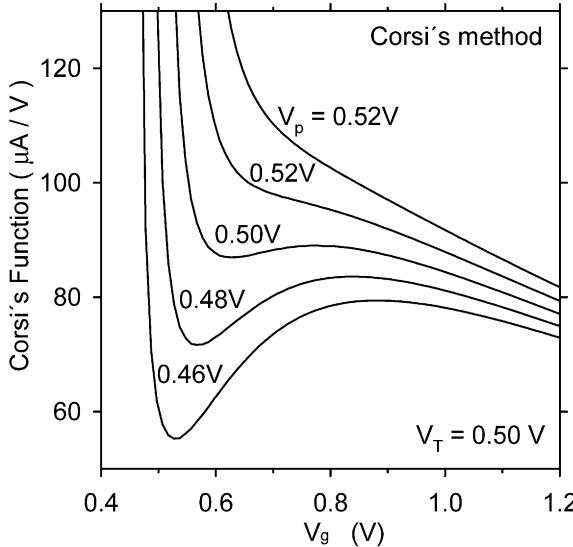


Fig. 9. Corsi function method implemented on the plot of the Corsi function versus V_g of the test bulk device for several arbitrary values of V_p . This method evaluates the threshold voltage by finding the plot for which the minimum just disappears and for this particular case $V_p = V_T$.

where $V_g > V_p$ and V_p is a parameter chosen in the region of expected values of V_T . Fig. 9 shows plots of this function versus V_g , for several values of V_p , as derived from the experimental transconductance characteristics of the test device. The minimum is related to a value of $V_g = V_T + (\alpha/2)V_d$, where α is a parameter dependent on small channel effects and the body effect. It can be demonstrated that the minimum disappears when $V_p = V_T$. In practice this method appears not to be very precise for determining the value of V_T and in our opinion it offers no particular advantages.

2.9. Second derivative logarithmic method

The SDL method was proposed by Aoyama in 1995 [31]. The threshold voltage is determined as the gate voltage at which the second difference of the logarithm of the drain current takes on a minimum value. It corresponds to the gate voltage at which drift and diffusion drain currents are equal to each other. The authors claim that this definition of V_T overcomes the disadvantages of the CC method, which requires measuring the effective channel length, and that it is more accurate than ELR, which can be applied only to the low drain voltage region, or than the already described transconductance method. However, similarly to other methods based on taking SDs, this method is highly sensitive to experimental measurement noise and error. Fig. 10 shows the implementation of this method for the present test device. It produces a reasonable value for V_T of

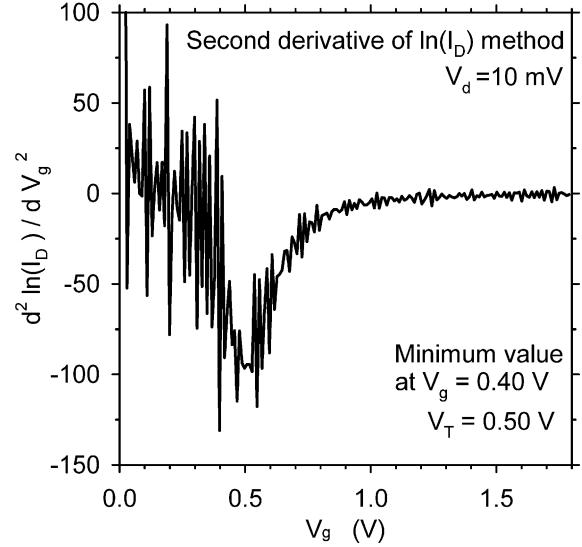


Fig. 10. SDL method implemented on the plot of $d^2 \ln(I_D) / dV_g^2$ versus V_g of the test bulk device measured at $V_d = 10$ mV. This method consists of finding the gate-voltage at which $d^2 I_D / dV_g^2$ exhibits a minimum value.

about 0.5 V, if measurement noise and error are suppressed.

2.10. Linear cofactor difference operator method

This method (LCDO), recently developed by He and co-workers to avoid the dependence of the extracted V_T value on mobility degradation, proposes to use the following auxiliary function [22]:

$$\Delta I_D \equiv G_x V_g - I_D, \quad (11)$$

where G_x is an arbitrary constant. The drain current, neglecting parasitic series resistance, is modeled by

$$I_D = \frac{G_d(V_g - V_T)}{1 + \theta(V_g - V_T)}, \quad (12)$$

where $G_d \equiv (W/L_{\text{eff}})\mu C_o V_d$ is a constant of the device with units of conductance, θ is the mobility reduction factor due to the vertical electric field in the channel, and other parameters have their usual meaning. Substituting (12) into (11) and taking the first derivative, it can be proved that ΔI_D will present a minimum value located at $V_g = V_{gp}$ and $\Delta I_D = \Delta I_{DP}$. The evaluation of this minimum value allows to extract V_T and θ by using:

$$V_T = \frac{\Delta I_{DP}}{(G_x G_d)^{1/2}} + \left[1 - \left(\frac{G_x}{G_d} \right)^{1/2} \right] V_{gp} \quad (13)$$

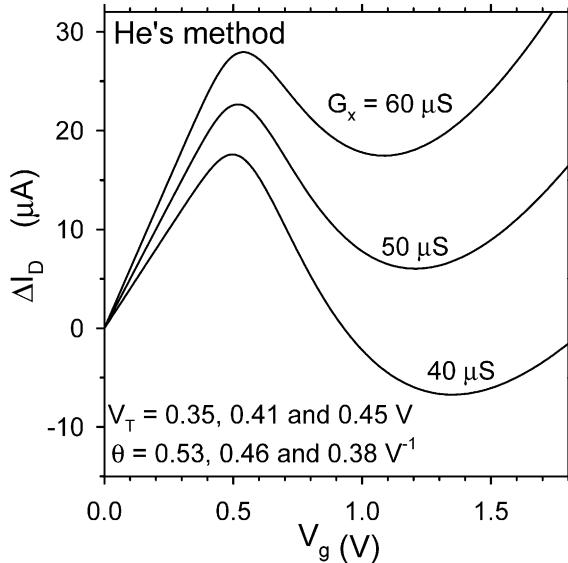


Fig. 11. LCDO method implemented on the plot of function ΔI_D versus V_g of the test bulk device measured at $V_d = 10$ mV.

and

$$\theta = \frac{G_d^{1/2} - G_x^{1/2}}{G_x^{1/2}(V_{gp} - V_T)}. \quad (14)$$

Fig. 11 shows the results of applying this method to the present test device. As can be observed, the location of the minimum value changes for different G_x . According to this method, the values of V_T and θ should be independent on the selected value of G_x . In contrast to this assumption, our results indicate that for variations of G_x from 40 to 60 μ S, V_T changes from 0.35 to 0.45 V and θ goes from 0.53 to 0.38 V^{-1} . Therefore this method does not seem to be very appropriate for short-channel devices.

2.11. Non-linear optimization method

The non-linear optimization method [23,24] extracts V_T based on optimization techniques applied to the MOSFET current–voltage characteristics. It has two main advantages: (1) the consistent determination of all the model parameters because of the simultaneous extraction; and (2) the reduction of the effects of the noise on the experimental data due to the optimization techniques. There are two main disadvantages, however: (1) non-physical parameter values can be obtained because of the pure fitting scheme, and (2) the requirement of a long computational process.

The development of this method, proposed by Karlsson and Jeppson [24], is as follows: The drain current for the MOSFET is expressed as

$$I_D = \frac{\beta(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}}{1 + \theta(V_{GS} - V_T)}, \quad (15)$$

where $\beta = (W/L_{\text{eff}})\mu C_o$ is the transconductance parameter, θ is the mobility reduction factor due to the vertical electric field in the channel, and other parameters have their usual meaning. For the MOSFET biased in the strong inversion region with a small drain voltage, and assuming the voltage drop in the source and drain series resistances is small compared to the gate bias, the drain current can be rewritten as

$$I_D = a \frac{V_g - b}{V_g - c} V_d, \quad (16)$$

where

$$a = \frac{\beta}{\theta + \beta R_{DS}}, \quad (17)$$

$$b = V_T + \frac{V_d}{2} \approx V_T, \quad (18)$$

and

$$c = V_T - \frac{1}{\theta + \beta R_{DS}}. \quad (19)$$

Fig. 12 shows measured I_D versus V_g characteristics (solid lines) for $V_d = 10$ mV of the same test device previously described. The fit (closed circles) to the simulated results were obtained by using the optimized values of $a = 12.4$ mA/V, $b = V_T = 0.57$ V and $c = -0.24$ V such that the following parameter ε has the minimum value:

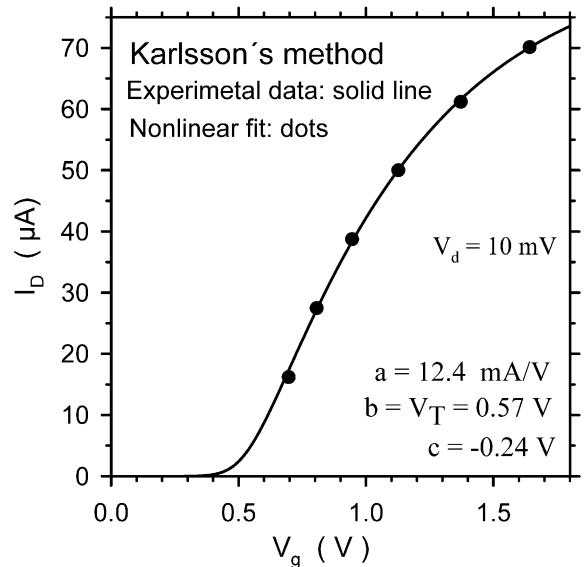


Fig. 12. Non-linear optimization method implemented on the measured I_D – V_g characteristics of the test bulk device measured at $V_d = 10$ mV.

$$\varepsilon \equiv \sum_{i=1}^N \left(I_D - a \frac{V_g - b}{V_g - c} V_d \right)^2. \quad (20)$$

Then, the following three parameters can be calculated from the values of a , b and c :

$$\beta = \frac{a}{b - c \frac{V_d}{2}}, \quad (21)$$

$$\theta + \beta R_{DS} = \frac{1}{b - c - \frac{V_d}{2}}, \quad (22)$$

$$\beta^{-1} = (\mu C_o)^{-1} \frac{(L_m - \Delta L_{eff})}{W}. \quad (23)$$

3. Extraction from the I_D – V_g curve of MOSFETs biased in the saturation region

To extract the saturation threshold voltage V_{Tsat} the drain current must be measured as a function of gate voltage with the drain connected to the gate, to guarantee that the device is operating in the saturation regime.

3.1. Extrapolation method in the saturation region

The ESR method, determines the threshold voltage from the gate voltage axis intercept of the $I_{Dsat}^{0.5}$ – V_g characteristics linearly extrapolated at its maximum first derivative (slope) point [1–3] as illustrated in Fig. 13. The value of V_{Tsat} calculated for the present device results to be 0.46 V.

3.2. G_1 function method

This method [34,35] considers that the device is operating in the saturation region and under strong inversion. The gate and drain terminals are connected together to ensure saturation operation. The saturation drain current may be expressed as [1–3]

$$I_{Dsat} = \frac{K}{2} (V_{GS} - V_T)^2, \quad (24)$$

where V_T is the threshold voltage,

$$V_{GS} = V_g - I_{Dsat} R_s \quad (25)$$

is the intrinsic gate–source voltage, V_g is the extrinsic gate–source voltage, R_s is the source series resistance, and

$$K = \frac{\beta}{1 + \theta(V_{GS} - V_T)}. \quad (26)$$

In the previous equation, θ is the mobility degradation parameter and $\beta = (W/L_{eff})\mu C_o$ is the transconductance parameter.

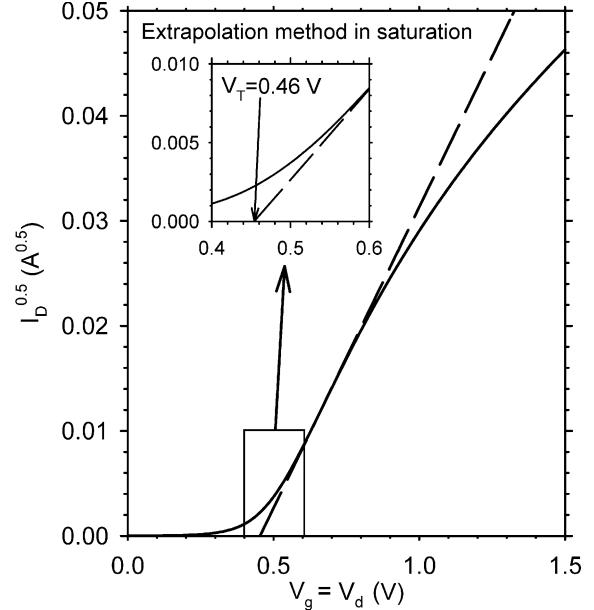


Fig. 13. Extrapolation method in the saturation region (ESR) implemented on the measured $I_{Dsat}^{0.5}$ – V_g characteristics of the test bulk device measured at $V_d = V_g$. This method consists of finding the gate-voltage axis intercept (i.e., $I_D^{0.5} = 0$) of the linear extrapolation of the $I_{Dsat}^{0.5}$ – V_g curve at its maximum slope point.

Substituting (25) and (26) into (24) and solving for V_g , we obtain:

$$V_g = V_T + R_t I_{Dsat} + \left(\frac{2I_{Dsat}}{K_o} + R_\theta^2 I_{Dsat}^2 \right)^{1/2}, \quad (27)$$

where

$$R_\theta \equiv \frac{\theta}{K_o} \quad (28)$$

is an effective resistance due to the free-carrier mobility degradation in the channel, and

$$R_t \equiv R_s + R_\theta \quad (29)$$

is the total effective resistance.

Using the approximation, $(2I_{Dsat}/K_o) \gg R_\theta^2 I_{Dsat}^2$, Eq. (27) is simplified to

$$V_g \approx V_T + R_t I_{Dsat} + \left(\frac{2}{K_o} \right)^{1/2} I_{Dsat}^{1/2}. \quad (30)$$

Based on an approach developed previously [47,48], we have proposed to use the following function to suppress the linear term of I_{Dsat} in (30):

$$G_1(V_g, I_{Dsat}) = V_g - \frac{2}{I_{Dsat}} \int_0^{V_g} I_{Dsat}(V_g) dV_g. \quad (31)$$

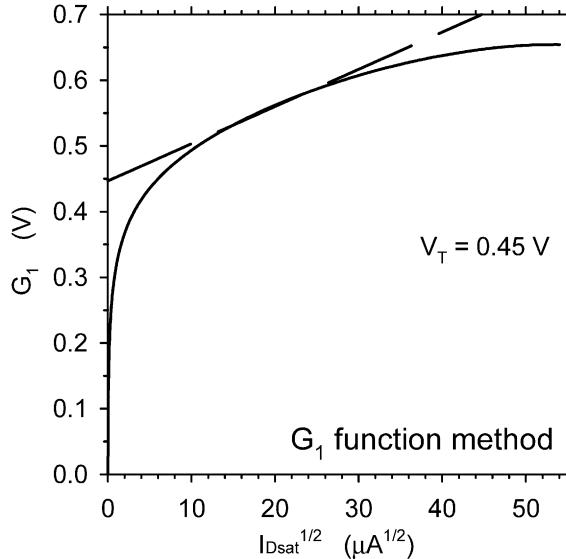


Fig. 14. G_1 function method in the saturation region implemented using the plot of the G_1 function versus $I_D^{0.5}$ of the test bulk device measured at $V_d = V_g$. This method consists of finding the gate-voltage axis intercept (i.e., $I_D^{0.5} = 0$) of the linear extrapolation of the $I_D^{0.5}$ – V_g curve.

The function defined in the previous equation, with units of V, can be numerically computed from the measured $I_{\text{Dsat}}(V_g)$ characteristics. It can be proved, after using integration by parts and doing algebraic manipulations, that (31) becomes

$$G_1(V_g, I_{\text{Dsat}}) = V_T + \frac{1}{3} \left(\frac{2}{K_o} \right)^{1/2} I_{\text{Dsat}}^{1/2}. \quad (32)$$

Therefore, the value of K_o can be obtained from the slope of G_1 versus $I_{\text{Dsat}}^{1/2}$ plot, and V_T can be determined from the intercept of the linear extrapolation of the G_1 curve to the y -axis.

The value of V_{Tsat} is extracted from the G_1 axis intercept of the linear fit of the calculated G_1 versus $I_{\text{Dsat}}^{0.5}$ curve, extrapolated in the region of the curve where the square root of the saturation current has a linear dependence on the gate voltage. That region is clearly shown in Fig. 13 around the maximum slope point. The result of applying this method to the present test device is presented in Fig. 14, indicating a value of V_{Tsat} close to 0.45 V.

4. Extraction from the I_D – V_g curve of non-crystalline MOSFETs biased in the saturation region

The extraction of V_T in non-crystalline MOSFETs is more conveniently performed from the drain current in saturation, considering that these devices present much

smaller drain currents than conventional single-crystal bulk devices. Amorphous TFTs introduce the following additional difficulties for V_T extraction: First, the saturation drain current in strong inversion is usually modeled by an equation of the form [49]

$$I_{\text{Dsat}} = K(V_{\text{GS}} - V_T)^m, \quad (33)$$

where K is a conductance parameter with units of A V^{−m} and m an empirical parameter which can be different from 2, the value used in conventional MOSFET models. Second, the value of parameter m cannot be easily extracted from a simple plot of $\log(I_{\text{Dsat}})$ versus $\log(V_g)$ because practical operation values of V_g are usually not large enough to validate the approximation: $(V_{\text{GS}} - V_T) \approx V_g$. Third, it is not clear at what point the I_{Dsat} versus V_g plot could be linearly extrapolated, since the curve does not present an inflection point because the mobility of these devices raises as V_g is increased.

A method to extract the threshold voltage of amorphous thin film MOSFETs, that circumvents some of these difficulties, is based on the following function which can be numerically computed from the measured $I_{\text{Dsat}}(V_g)$ characteristics:

$$H(V_g) = \frac{\int_0^{V_g} I_{\text{Dsat}}(V_g) dV_g}{I_{\text{Dsat}}}, \quad (34)$$

where the upper limit of integration is any suitable value greater than the threshold voltage.

The integral in (34) is negligible for values of V_g such that the device is operating in the strong inversion region. Thus, $H(V_g)$ may be approximated by

$$H(V_g) \approx \frac{\int_{V_T}^{V_g} I_{\text{Dsat}}(V_g) dV_g}{I_{\text{Dsat}}}. \quad (35)$$

After substitution of (33) into (35), and assuming that the variation of K with respect to V_g is insignificant, we obtain:

$$H(V_g) = \frac{(V_g - V_T)}{m + 1}, \quad (36)$$

which means that $H(V_g)$ behaves linearly in the strong inversion region. Therefore, a plot of function H versus V_g has a slope that defines the value of m and a V_g axis intercept which gives the sought after value of V_T . Because of the low-pass filter nature of integration, this method offers the additional advantage of inherently reducing the effects of experimental errors.

After having found m and V_T , the remaining parameter in (33), K , may be easily evaluated from

$$K = \frac{I_{\text{Dsat}}}{(V_g - V_T)^m}. \quad (37)$$

This extraction procedure will be applied to an experimental n-channel a-Si:H thin film MOSFET having: a

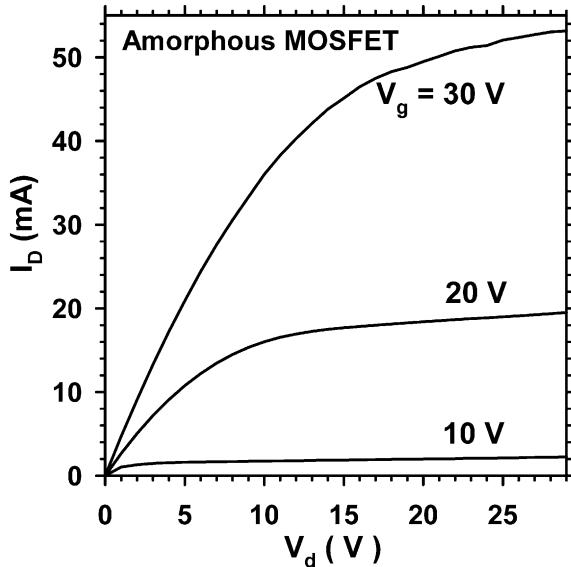


Fig. 15. Measured I_D - V_d characteristics at three values of gate bias for the experimental n-channel amorphous TFT.

gate oxide thickness of 0.3 μm ; an intrinsic a-Si:H layer thickness of 0.3 μm ; 0.1 μm thick n⁺ drain and source regions with impurity concentrations of 10^{18} cm^{-3} ; channel width of 600 μm and channel length of 40 μm . The measured I_D versus V_d output characteristics for several values of V_g are presented in Fig. 15. Examination of this figure indicates that the threshold voltage must be smaller than 10 V, since it shows that there is a reasonable drain current flowing already at $V_g = 10$ V.

Fig. 16 presents the measured $I_{D\text{sat}}$ versus V_g transfer characteristics with linear and logarithmic scales for the vertical axis. The drain current was measured using 0.5 V gate-to-source voltage steps, with the drain connected to the gate to insure operation in the saturation regime. Fig. 16 also presents the results of simulating the device using (33) with the values of parameters that will be extracted by the present method. It is clear from this figure that the plot of $I_{D\text{sat}}$ does not show evidence of any inflection point and, thus, a plot of $g_{\text{msat}} = dI_{D\text{sat}}/dV_g$ will always rise as V_g is increased. If we were to apply the commonly used so-called “constant current definition” for threshold voltage as being the gate bias corresponding to an arbitrary value of drain current, for instance 0.1 μA , we would obtain $V_T = 6$ V, a value which is far from being correct, as we shall see. Likewise, using the plot of $\log(I_{D\text{sat}})$ versus V_g would give the false impression that the transition from weak to strong inversion occurs at about 8 V, a value that is an even worse estimation of the threshold voltage.

Fig. 17 shows a plot of the numerical calculation of $H(V_g)$ according to (34). For strong inversion the curve is seen to behave approximately as a straight line with a

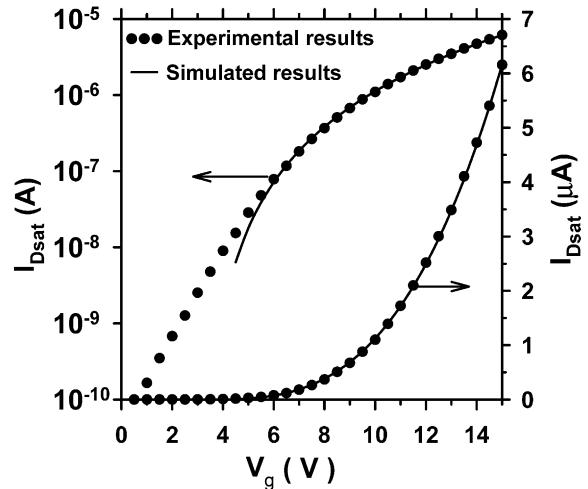


Fig. 16. Measured $I_{D\text{sat}}$ (symbols) versus gate bias for the experimental n-channel amorphous TFT. A 0.5 V gate-to-source voltage step was used with the drain connected to the gate. Also shown (continuous line) are the simulated results using the extracted set of parameter values: $m = 3.07$, $V_T = 3.25$ V and $K = 3.2 \text{ nA V}^{-m}$.

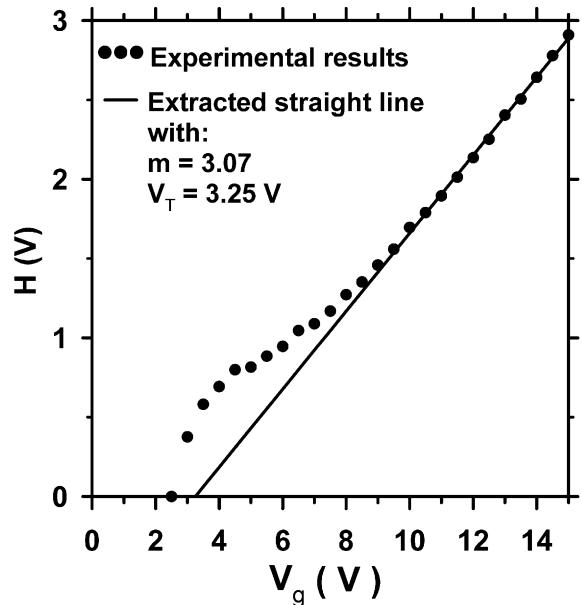


Fig. 17. Function $H(V_g)$ of the experimental n-channel amorphous TFT calculated from the I_D - V_g characteristics presented in the previous figure. The slope of the straight line for strong inversion is 0.246, which according to (5) implies $m = 3.07$. The intercept of the straight line to the gate bias axis is 3.25 V, which implies $V_T = 3.25$ V.

slope of 0.246 and a V_g axis intercept (threshold voltage) of 3.25 V. Furthermore, according to (36), this slope implies a power-law empirical exponent $m = 3.07$. It is

worth noting here that an alternate but laborious way to extract m for the strong inversion region would be to find, through trial and error, the value of m which produces the maximum linearity of $I_{D_{sat}}^{1/m}$, evaluated through a linear regression coefficient. Such procedure was applied and it yields $m = 3.06$, with a linear regression coefficient of 0.999797, which matches very well the value previously extracted through the present procedure and thus confirms its accuracy.

Synthetic $I_{D_{sat}}$ curves were simulated using (33) with the extracted parameter values: $m = 3.07$, $V_T = 3.25$ V and $K = 3.2$ nA V $^{-m}$. They are presented in Fig. 16 together with the original experimental data. The excellent match obtained between the resulting characteristics for strong inversion, simulated using the extracted parameters, and the measured data clearly validates the procedure.

5. Conclusions

We have presented, reviewed and critically compared several extraction methods currently used to determine the threshold voltage value of bulk single-crystal and non-crystalline thin film MOSFETs from their drain current versus gate voltage transfer characteristics measured either in linear or saturation operation regimes. The relative performance of the presented methods was illustrated and compared under the same conditions by applying them to the measured characteristics of two real test devices: (a) an enhancement-mode n-channel single-crystal silicon bulk MOSFET with state-of-the-art 0.18 μ m channel length, and (b) an experimental n-channel a-Si:H thin film MOSFET. Eleven methods that use the transfer characteristics under linear regime operation conditions were applied to the single-crystal bulk device. Table 1 presents the resulting different threshold voltage

Table 1

Threshold voltage values obtained from 11 extraction methods for a short-channel single-crystal bulk device ($L_m = 0.18$ μ m) biased in the linear region

Method	Threshold voltage (V)
CC (5 μ A)	0.55
ELR	0.51
GMLE	0.44
SD	0.50
RM	0.63
Transition	0.49
Integral	0.51
Corsi	0.50
SDL	0.50
LCDO	0.35–0.45
Optimization	0.57

Table 2

Threshold voltage values obtained from two extraction methods for a short-channel single-crystal bulk device ($L_m = 0.18$ μ m) biased in the saturation region

Method	Threshold voltage (V)
ESR	0.46
G_1	0.45

values for this device. As can be observed in this table, seven out of the eleven methods presented to extract threshold voltage under linear region bias produce very similar results, of about 0.5 V.

Two additional methods were applied under saturation regime operation to the same single-crystal bulk device. The saturation threshold voltage values extracted by either method are very close, as shown in Table 2. Finally, we can also conclude that the results of applying the non-crystalline MOSFET specific method to an experimental n-channel a-Si:H TFT has revealed that this method is better suited for accurate threshold voltage extraction of this type of device than other more conventional methods.

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References

- [1] Schroeder DK. Semiconductor material and device characterization, 2nd ed. New York: Wiley; 1998.
- [2] Liou JJ, Ortiz-Conde A, García Sánchez FJ. Analysis and design of MOSFETs: modeling, simulation and parameter extraction. New York, USA: Kluwer Academic Publishers; 1998.
- [3] Haddara H. Characterization methods of submicron MOSFETs. New York, USA: Kluwer Academic Publishers; 1996.
- [4] Terada K, Nishiyama K, Hatanaka KI. Comparison of MOSFET-threshold-voltage extraction methods. Solid-State Electron 2001;45:35–40.
- [5] Liou JJ, Ortiz-Conde A, García Sánchez FJ. Extraction of the threshold voltage of MOSFETs: an overview (invited). In: Proceedings of IEEE HKEDM, Hong Kong, June 1997. p. 31–8.
- [6] Ortiz-Conde A, García Sánchez FJ, Liou JJ. An overview on parameter extraction in field effect transistors. Acta Científica Venezolana 2000;51:176–87.
- [7] Ortiz-Conde A, Rodríguez J, García Sánchez FJ, Liou JJ. An improved definition for modeling the threshold voltage of MOSFETs. Solid-State Electron 1998;42:1743–6.

- [8] Salcedo JA, Ortiz-Conde A, García Sánchez FJ, Muci J, Liou JJ, Yue Y. New approach for defining the threshold voltage of MOSFETs. *IEEE Trans Electron Dev* 2001;48:809–13.
- [9] Benson J, D'Hallewyn NV, Redman-White W, Easson CA, Uren MJ, Faynot O, Pelloie JL. A physically based relation between extracted threshold voltage and surface potential flat band voltage for MOSFET compact modeling. *IEEE Trans Electron Dev* 2001;48:1019–21.
- [10] Zhou X, Lim KY, Lim D. A simple and unambiguous definition of threshold voltage and its implications in deep-submicron MOS device modeling. *IEEE Trans Electron Dev* 1999;46:807–9.
- [11] Zhou X, Lim KY, Qian W. Threshold voltage definition and extraction for deep-submicron MOSFETs. *Solid-State Electron* 2001;45:507–10.
- [12] Wong HS, White MH, Krutsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's. *Solid-State Electron* 1987;30:953.
- [13] Jain S. Measurement of threshold voltage and channel length of submicron MOSFETs. *IEE Proc Cir Dev Syst* 1988;135:162.
- [14] Ghibaudo G. New method for the extraction of MOSFET parameters. *Electron Lett* 1988;24:543–5.
- [15] Fikry W, Ghibaudo G, Haddara H, Cristoloveanu S, Dutoit M. Method for extracting deep submicrometer MOSFET parameters. *Electron Lett* 1995;31:762–4.
- [16] Sasaki M, Ito H, Horiuchi T. A new method to determine effective channel length, series resistance and threshold voltage. In: Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS), 1996. p. 139–44.
- [17] Hardillier S, Mourrain C, Bouzid MJ, Ghibaudo G. New method for the parameter extraction in Si MOSFETs after hot carrier injection. In: Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS), 1997. p. 63–6.
- [18] Mourrain C, Cretu B, Ghibaudo G, Cottin P. New method for parameter extraction in deep submicrometer MOSFETs. In: Proceedings of the 2000 International Conference on Microelectronic Test Structures (ICMTS), 2000. p. 181–6.
- [19] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. Reliable threshold voltage determination for sub-0.1 μm gate length MOSFETs. In: Proceedings of Asia and South Pacific Conference, 1998. p. 111–6.
- [20] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. Physically-based threshold voltage determination for MOSFET's of all gate lengths. *IEEE Trans Electron Dev* 1999;46:1429–34.
- [21] Corsi F, Marzocca C, Portacci GV. New experimental technique for fast and accurate MOSFET threshold extraction. *Electron Lett* 1993;29:1358–60.
- [22] He J, Zhang X, Wang YY. Linear cofactor difference operator method and its application in extracting threshold voltage and mobility of MOSFETs. *IEEE Trans Electron Dev*, in press.
- [23] McAndrew CC, Layman PA. MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization. *IEEE Trans Electron Dev* 1992;ED-39:2298–311.
- [24] Karlsson PR, Jeppson KO. An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors. *IEEE Trans Semicond Manuf* 1996;9:215–22.
- [25] Katto H. Device parameter extraction in the linear region of MOSFET's. *IEEE Electron Dev Lett* 1997;18:408–10.
- [26] Wang J, Xu M, Tan C. An accurate relationship for determining the key parameters of MOSFETs by proportional difference operator meted. *Solid-State Electron* 2000;44:959–62.
- [27] Tan C, Xu M, Wang Z. Proportional difference operator method and its application in studying subthreshold behavior of MOSFETs. *Solid-State Electron* 2000;44:1059–67.
- [28] El-Kareh B, Tonti WR, Titcomb SL. A submicron MOSFET parameter extraction technique. *IBM J Res Develop* 1990;34:243–9.
- [29] Yan ZX, Deen MJ. Physically-based method for measuring the threshold voltage of MOSFETs. *IEE Proc Cir Dev Syst* 1991;138:351.
- [30] Dobrescu L, Petrov M, Dobrescu D, Ravariu C. Threshold voltage extraction methods for MOS transistors. In: Proc Int Sem Conf, 2000. p. 371–4.
- [31] Aoyama K. A method for extracting the threshold voltage of MOSFET based on current components. *Simul Semicond Dev Process* 1995;6:118–21.
- [32] Ortiz-Conde A, Gouveia E, Liou JJ, Hassan MR, García Sánchez FJ, De Mercato G, Wang W. A new approach to extract the threshold voltage of MOSFETs. *IEEE Trans Electron Dev* 1997;44:1523–8.
- [33] García Sánchez FJ, Ortiz-Conde A, Mercato GD, Salcedo JA, Liou JJ, Yue Y. New simple procedure to determine the threshold voltage of MOSFETs. *Solid-State Electron* 2000;44:673–5.
- [34] Ortiz-Conde A, García Sánchez FJ, Cerdeira A, Estrada M, Flandre D, Liou JJ. A procedure to extract mobility degradation, series resistance and threshold voltage of SOI MOSFETs in the saturation region. Sixth International Conference on Solid-State and Integrated-Circuit Technology, October 2001 Shanghai, China. p. 887–90.
- [35] García Sánchez FJ, Ortiz-Conde A, Cerdeira A, Estrada M, Flandre D, Liou JJ. A method to extract mobility degradation and total series resistance of fully-depleted SOI MOSFETs. *IEEE Trans Electron Dev* 2002;49:82–8.
- [36] Lau MM, Chiang CYT, Yeow YT, Yao ZQ. Measurement of V_T and I_{eff} using MOSFET gate-substrate capacitance. In: Proceedings of the 1999 International Conference on Microelectronic Test Structures, 1999. p. 152–5.
- [37] Lau MM, Chiang CYT, Yeow YT, Yao ZQ. A new method of threshold voltage extraction via MOSFET gate-to-substrate capacitance measurement. *IEEE Trans Electron Dev* 2001;48:1742–4.
- [38] Taur Y, Zicherman DS, Lombardi DR, Restle PJ, Hsu CH, Hanafi HY, Wordeman MR, Davari B, Shahidi GG. A new “shift and ratio” method for MOSFET channel-length extraction. *IEEE Electron Dev Lett* 1992;EDL-13:267–9.
- [39] Cretu B, Bouthachacha T, Ghibaudo G, Balestra F. New ratio method for effective channel length and threshold

- voltage extraction in MOS transistors. *Electron Lett* 2001;37:717–9.
- [40] Galup-Montoro C, Schneider MC, Koerich AL, Pinto RLO. MOSFET threshold extraction from voltage-only measurements. *Electron Lett* 1994;30:1458–9.
- [41] Tsay JH, Liu SI, Wu YP. A simple and accurate method to measure the threshold voltage of a MOSFET using MOS active attenuator. *Int J Electron* 1996;81:49–58.
- [42] Lee HG, Oh SY, Fuller G. A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFET. *IEEE Trans Electron Dev* 1982;29: 346–8.
- [43] Cilimgiroglu U, Hoon SK. An accurate self-bias threshold voltage extractor using differential difference feedback amplifier. In: *IEEE Int Symp Cir Syst*, 2000. p. V209–12.
- [44] Thomas F, Holman WT. MOSFET threshold voltage extractor circuits based on square-law behavior. In: Sample S, editor. *IEEE 42nd Midwest Symp Cir Syst*, vol 2, 2000. p. 1118–21.
- [45] Ortiz-Conde A, Cerdeira A, Estrada M, García Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. *Solid-State Electron* 2001;45:663–7.
- [46] Cerdeira A, Estrada M, García R, Ortiz-Conde A, García Sánchez FJ. New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions. *Solid-State Electron* 2001;45:1077–80.
- [47] García Sánchez FJ, Ortiz-Conde A, Liou JJ. A parasitic series resistance-independent method for device-model parameter extraction. *IEE Proc Cir Dev Syst* 1996;143:68.
- [48] García Sánchez FJ, Ortiz-Conde A, De Mercato G, Liou JJ, Recht L. Eliminating parasitic resistances in parameter extraction of semiconductor device models. *Proc of First IEEE Int Caracas Conf on Dev Cir and Syst*, Caracas, Venezuela, 1995. p. 298.
- [49] Merckel G, Rolland A. A compact CAD model for amorphous silicon thin film transistors simulation. I. D.C. analysis. *Solid-State Electron* 1996;39:1231–9.