```vhdl
-- Sumador completo BCD de 3 dígito


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;


entity sum_BCD_3dig is
port(
      A     : in std_logic_vector(11 downto 0);
      B     : in std_logic_vector(11 downto 0);
      Cin   : in std_logic;
      Cout  : buffer std_logic;
      S     : buffer std_logic_vector(11 downto 0)
);
end entity;

architecture estructural of sum_BCD_3dig is

      signal Ci:  std_logic_vector(1 downto 0);

begin

      DigitoU: entity Work.sum_BCD(rtl)
               port map(A => A(3 downto 0),
                    Cin => Cin,
                    B => B(3 downto 0),
                    S => S(3 downto 0),
                    Cout => Ci(0));

      DigitoD: entity Work.sum_BCD(rtl)
             port map(A => A(7 downto 4),
                    B => B(7 downto 4),
                    Cin => Ci(0),
                    S => S(7 downto 4),
                    Cout => Ci(1));


      DigitoC: entity Work.sum_BCD(rtl)
             port map(A => A(11 downto 8),
                    B => B(11 downto 8),
                    Cin => Ci(1),
                    S => S(11 downto 8),
                    Cout => Cout);

end estructural;
```

```vhdl
-- Test-bench sumador completo BCD de 1 digito


library ieee;
use ieee.std_logic_1164.all;
```

```vhdl
use ieee.std_logic_unsigned.all;

entity tb_sum_BCD_3dig is
end entity;

architecture test of tb_sum_BCD_3dig is

	signal A: std_logic_vector(11 downto 0);
	signal B: std_logic_vector(11 downto 0);
	signal Cout: std_logic;
	signal Cin : std_logic;
	signal S   : std_logic_vector(11 downto 0);

begin
dut: entity Work.sum_BCD_3dig(estructural)
port map(
	A => A,
	B => B,
	Cin => Cin,
	Cout => Cout,
	S => S
	);

process
begin


	A <= (others => '0');
	B <= (others => '0');
	Cin <= '0';
	wait for 100 ns;

	  A <= X"000";
  B <= X"987";
  wait for 100 ns;

  A <= X"654";
  B <= X"000";
  wait for 100 ns;

  A <= X"333";
  B <= X"666";
  wait for 100 ns;

  A <= X"547";
  B <= X"126";
  wait for 100 ns;

  A <= X"381";
  B <= X"245";
  wait for 100 ns;

  A <= X"999";
  B <= X"999";
  wait for 100 ns;
  wait;
end process;
```

```
end test;
```