```vhdl
-- Banco de 4 registros de 4 bits.


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity banco_de_reg is
port(
      clk,nrst    : in std_logic;
      peso_dig    : in std_logic_vector(1 downto 0);
      dir_dig           : in std_logic_vector(1 downto 0);
      we_dig            : in std_logic;
      digito            : in std_logic_vector(3 downto 0);
      digito_out  : buffer std_logic_vector(3 downto 0)
);
end entity;

architecture rtl of banco_de_reg is

      signal reg0,reg1,reg2,reg3 : std_logic_vector(3 downto 0);

begin

process(clk,nrst)
begin
   if nrst = '0' then
      reg0 <= (others => '0');
      reg1 <= (others => '0');
      reg2 <= (others => '0');
      reg3 <= (others => '0');
   elsif clk'event and clk = '1' then
      if we_dig = '1'   then
         case peso_dig is
            when "00" => reg0 <= digito;
            when "01" => reg1 <= digito;
            when "10" => reg2 <= digito;
            when "11" => reg3 <= digito;
            when others => null;
         end case;
      end if;
   end if;
end process;

digito_out <= reg0 when dir_dig = "00" else
              reg1 when dir_dig = "01" else
              reg2 when dir_dig = "10" else
              reg3;



end rtl;
```