```vhdl
-- Modelo estructural
library ieee;
use ieee.std_logic_1164.all;


entity conv_bcd_a_bin_sec is
port( digito: in std_logic_vector(3 downto 0);
      peso_dig: in std_logic_vector(1 downto 0);
      we_dig, start: in std_logic;
      clk,nrst: in std_logic;
      fin_op: buffer std_logic;
      resultado: buffer std_logic_vector(13 downto 0));
end entity;

architecture estructural of conv_bcd_a_bin_sec is

      signal digito_out: std_logic_vector(3 downto 0);
      signal rst_acum: std_logic;
      signal ena_acum: std_logic;
      signal dir_dig: std_logic_vector(1 downto 0);

begin

      U_BANCO: entity Work.banco_de_reg(rtl)
            port map( clk => clk,
                  nrst => nrst,
                  digito => digito,
                  dir_dig => dir_dig,
                  peso_dig => peso_dig,
                  we_dig => we_dig,
                  digito_out => digito_out);

      U_ACUM_SUMA_PROD: entity Work.acum_suma_prod(rtl)
            port map( clk => clk,
                  nRst => nrst,
                  acum_in => digito_out,
                  rst_acum => rst_acum,
                  ena_acum => ena_acum,
                  resultado => resultado);

      U_CONTROL: entity Work.control(rtl)
            port map( clk => clk,
                  nRst => nrst,
                  start => start,
                  rst_acum => rst_acum,
                  ena_acum => ena_acum,
                  fin_op => fin_op,
                  dir_digito => dir_dig);

end estructural;
```