```vhdl
-- Contador BCD con ena y modulo 94


library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;


entity cnt_BCD is
port(
      clk,nrst: in std_logic;
      ena   : in std_logic;
      rst   : buffer std_logic

);

end entity;

architecture rtl of cnt_BCD is

      signal cnt_uni: std_logic_vector(3 downto 0);
      signal cnt_dec: std_logic_vector(3 downto 0);
      signal cout: std_logic;

begin

-- Unidades
process(clk,nrst)
begin
   if nrst = '0' then
      cnt_uni <= (others => '0');
   elsif clk'event and clk = '1' then
      if rst = '1' then
         cnt_uni <= (others => '0');
      elsif ena = '1' then
         if cnt_uni = 9 then
            cnt_uni <= (others => '0');
         else
            cnt_uni <= cnt_uni + 1;
         end if;
      end if;
   end if;
end process;

cout <= '1' when cnt_uni = 9 and ena = '1' else '0';

-- Decenas

process(clk,nrst)
begin
   if nrst = '0' then
      cnt_dec <= (others => '0');
   elsif clk'event and clk = '1' then
      if rst = '1' then
         cnt_dec <= (others => '0');
      elsif cout = '1' then
         if cnt_dec = 9 then
```

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            cnt_dec <= (others => '0');
         else
            cnt_dec <= cnt_dec + 1;
         end if;
      end if;
   end if;
end process;

rst <= '1' when cnt_uni = 3 and cnt_dec = 9 and ena = '1' else '0';

end rtl;
```

```
-- Test-bench del contador BCD con ena y modulo 94


library ieee;
use ieee.std_logic_1164.all;

entity tb_cnt_BCD is
end entity;

architecture test of tb_cnt_BCD is

      signal clk, nrst: std_logic;
      signal ena: std_logic;
      signal rst: std_logic;

      constant T_CLK : time := 1 us;
      signal final: boolean := false;

begin

dut: entity Work.cnt_BCD(rtl)
port map(
      clk => clk,
      nrst => nrst,
      ena => ena,
      rst => rst
      );

process
begin

      clk <= '0';
      wait for T_CLK/2;
      clk <= '1';
      wait for T_CLK/2;
        if final then
           wait;
        end if;
end process;

process
begin
      -- Inicializacion asincrona
```

```
        nrst <= '0';
        wait until clk'event and clk = '1';
        ena <= '0';
        wait until clk'event and clk = '1';

        -- ENA = '0', por lo que no debe contar
        nrst <= '1';
        wait until clk'event and clk = '1';
        wait until clk'event and clk = '1';

        -- Inicializamos el ENA, debe contar
        ena <= '1';
        wait until clk'event and clk = '1';
        wait for 50*T_CLK;
        wait until clk'event and clk = '1';

        -- Volvemos a desactivar ENA y comprobamos que deja de contar
        ena <= '0';
        wait until clk'event and clk = '1';
        wait until clk'event and clk = '1';

        -- Activamos de nuevo ENA
        ena <= '1';
        wait until clk'event and clk = '1';
        wait for 100*T_CLK;
        wait until clk'event and clk = '1';


        final <= true;
        wait;

end process;
end test;
```