

# Design Heterogeneous ICs with Chiplets – A Power Perspective

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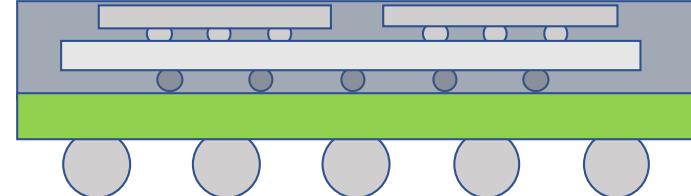
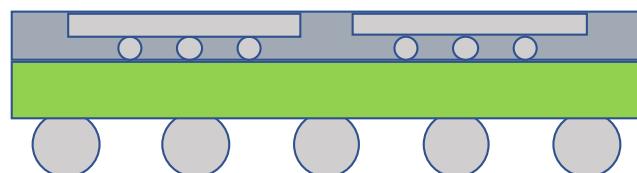
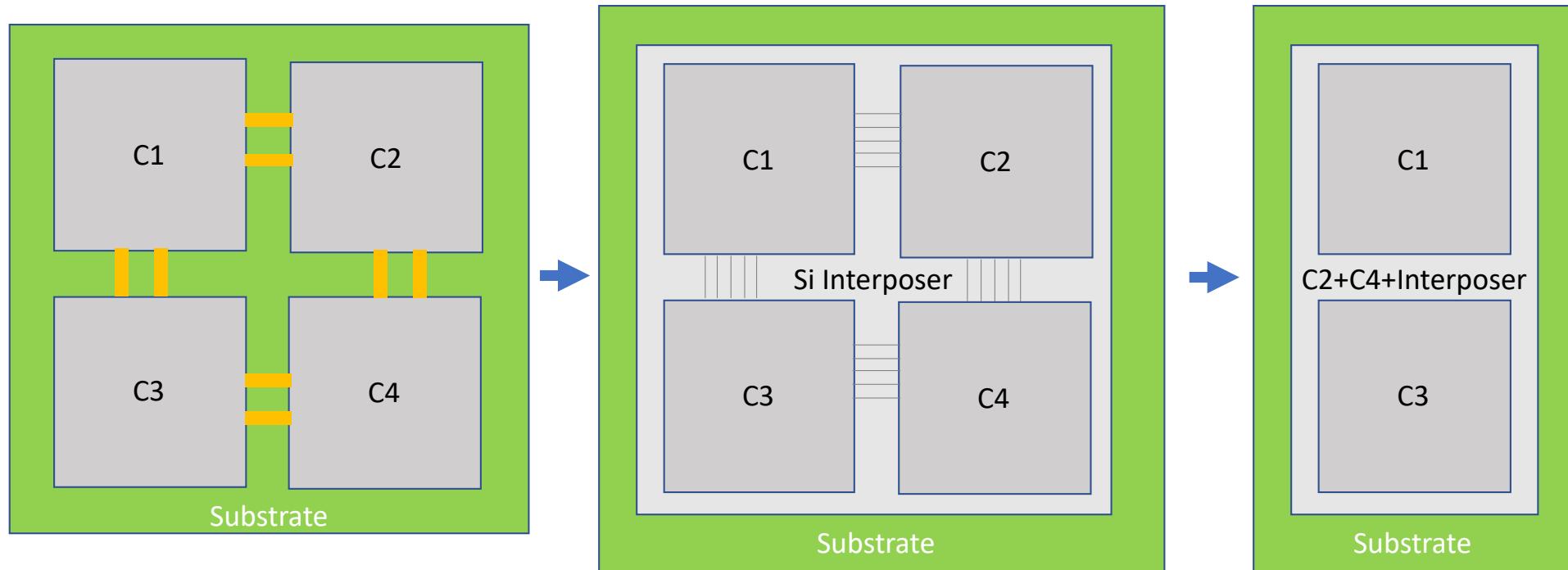
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<https://dac2020.pathable.co/organizations/aKPenY37tCNL9WMG5>

# Outline

1. BACKGROUND
  - Intro to Chiplet Based Designs—MCM, VSOC, Active Interposers
  - Power Planning and Modeling for MCM
  - Early Stage Power Modeling and Integration Choices
  - Power Modeling Basics Reminder
2. A POWER MODELING EXAMPLE
  - A Power Modeling Test Case (The Homework Assignment)
  - Power ZEF overview
  - Power Modeling Results for the Test Case
3. POWER MANAGEMENT IN ACTIVE SILICON INTERPOSERS
  - Active Silicon Interposers— zGlue as an example
  - Advanced power management with active silicon interposers
4. SUMMARY

# Multi Chiplet Modules



# “Power Is Everything”

Power Profile	$10^{-1}$ W	$10^0$ W	$10^1$ W	$10^2$ W	$10^3 - 10^5$ W	$10^6$ W
Applications	AIoT, Trackers, Wearables	Mobile	Laptops Pads	Servers	Racks	Data Centers
Energy Efficiency Challenge	✓	✓	✓	✓	✓	✓
Thermal Design Challenge		✓	✓	✓	✓	✓

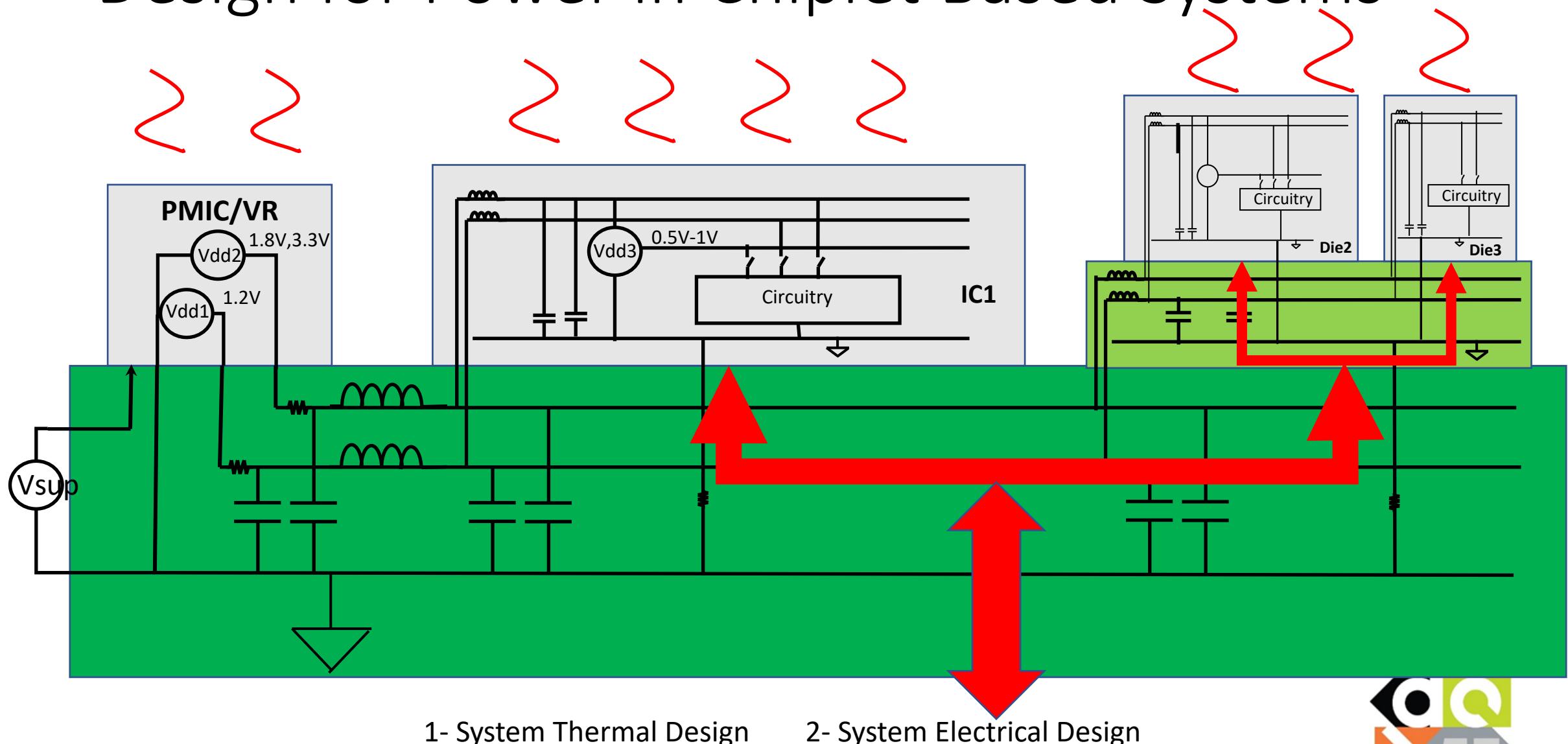
Chip Active Power Top Usage: IO/SerDes/Optical/RF, Compute, Storage

Chip Static Power Top Usage: Transistor Leakage, DC Biasing

Chip Thermal Design Range: 1mW-1000W



# Design for Power in Chiplet Based Systems



1- System Thermal Design

2- System Electrical Design



# Design Stages For Chiplet Integration

## Architecture and Early Design

Choose Multi-Die Technology  
Cost Analysis  
Performance Modeling  
**Early Power Estimation**  
Choose A Thermal Solution  
Design For Structural Integrity  
Design For Testing  
System Level Test Development

## Multi-Die Design Execution

Multi Die Design  
System Connectivity  
Power Delivery Integrity  
Signal Integrity  
Cross-Die Timing  
Noise Analysis  
EM/IR  
**Detailed Power Model**  
Thermal Analysis  
Structural Analysis  
Design Sign Off

## Manufacture: Bring Up and Reliability

Wafer Probe  
Organic Material Testing  
**Bring Up Testing**  
System Level Test  
Environment Reliability  
Later Life Failure Testing

# Power Modeling For Chiplet Integration

## Architecture and Early Design

- Early Power Estimation
- 1 - Understand Components
- 2- Understand Usecases
- 3- Rough Estimate of Scenarios
- 4- Normalize Data to a PVT condition
- 5- Table/Equation based summation
- 6- Early Power Estimate Ready
- 7- Validate against historical data, Thermal Solution
- 8- Iterate

## Multi-Die Design Execution

- Detailed Power Model
- 1- Create detailed UPM Models of All Components
- 2- Get detailed vector snippets
- 3- Simulate at transistor level where possible
- 4- Generate detailed power maps
- 5- Refine the power grid and thermal solution

## Manufacture: Bring Up and Reliability

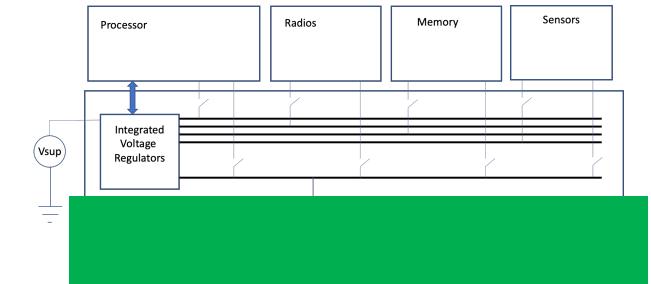
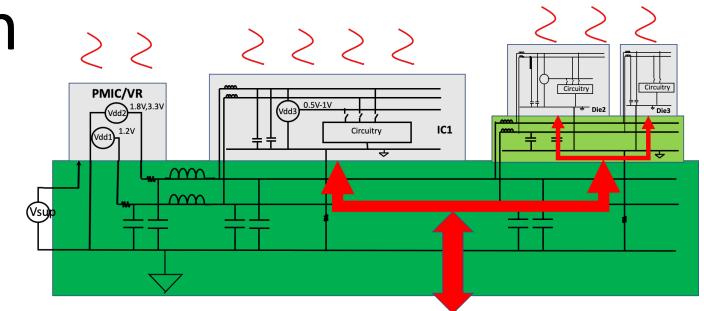
- Bring Up Testing
- 1- Validate power measurements against usecases
- 2- Little can be done at this stage if measurement are wildly off the simulation results. Design Iteration cycles are way too long.

Homework Exercise in the Folder Takes you through a simple exercise.



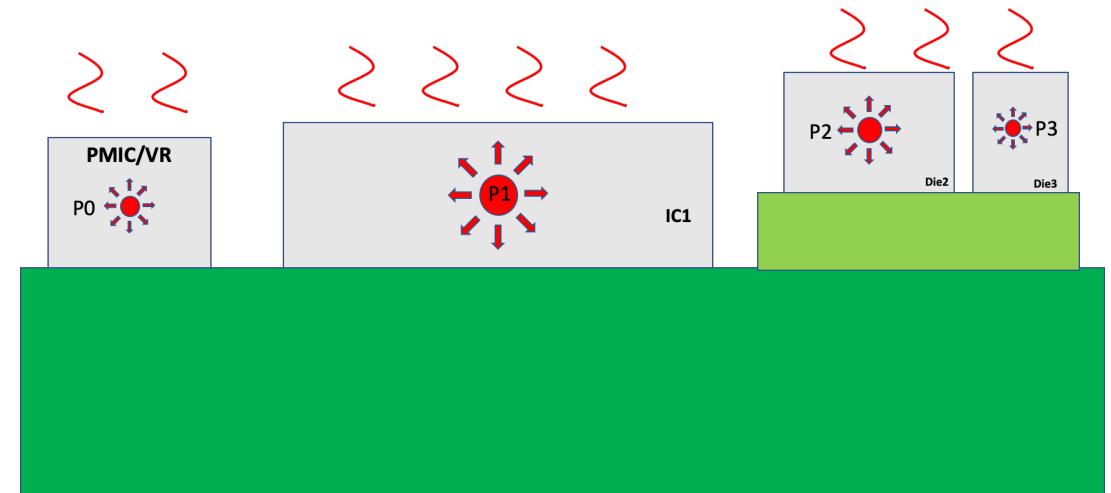
# Need for Early Power Modelling

- Side-by-Side Placement (Cheaper and Good-Enough Performance)
  - Easier Shrink of the System (Improves IO Power Dissipation somewhat)
  - Critical Dimensions Shrinking down to 2um line/space (driven by cost, not performance)
  - Somewhat helps on Time to Market
- Vertical Stacking (New Technologies Needed)
  - Vertical Interconnect (Significantly Improves performance and power )
  - Vertical Power Management (Significantly Improved Co-designed Power Management)



# Thermal Design—Power Consideration

- Thermal and Floor planning
  - Technology Selection
  - Vertical OR Side-by-Side Integration
- Power Dissipation Design
  - Heat Spreader, Heat Sink Design
  - Accurate power model is needed for accurate power model (recursive)  
(Leakage model depends on temperature which depends on accurate leakage model among others)



# CMOS Monolithic IC Power Modeling

$$P = P_{\text{dynamic}} + P_{\text{static}} + P_{\text{glitch}}$$

1-

$$P_{\text{dynamic\_rough}} = \text{Area} \times P_{\text{dyn\_density}}$$

$$P_{\text{dynamic\_accurate}} = a \times C \times V_{dd} \times V_{dd} \times \text{freq}$$

2-

$P_{\text{static}} = I_{\text{static}} \times V_{dd}$ , where  $I_{\text{static}}$  includes digital circuit leakage and analog circuit power draw

Accuracy	C	a	$I_{\text{static}}$
Rough	Circuit Area & Fab Tech Comparison	Mode of Operation	Transistor widths
Accurate	Extract Layout	Snippets of actual workload	Vector based dc simulations

Normalization of Power to same P, V, T, f is tedious but needed



# Chiplet-Based IC Early Power Modeling

$$P = P_{\text{dynamic}} + P_{\text{static}}$$

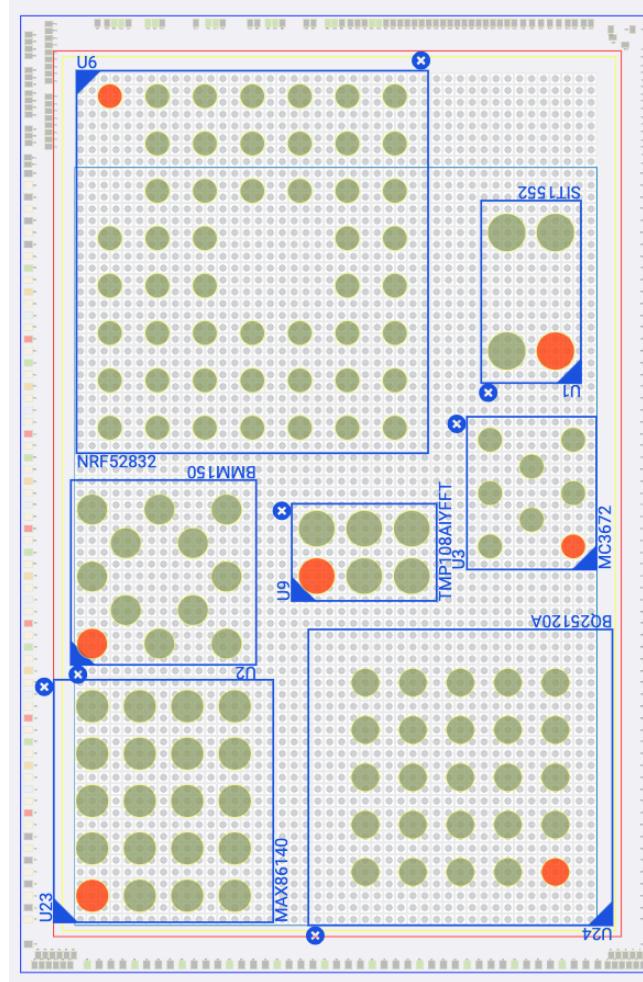
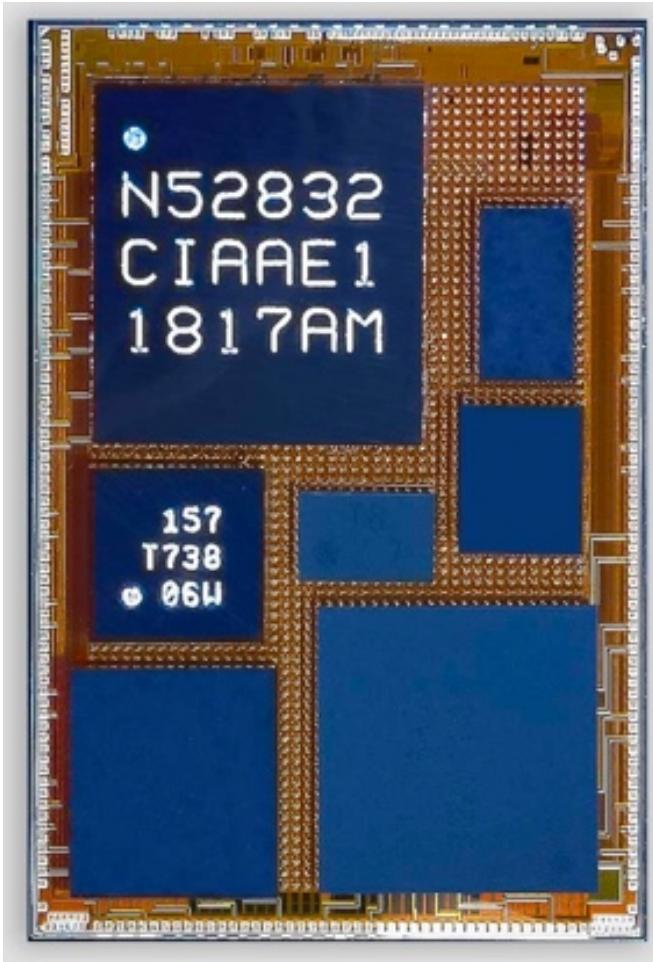
- Data Sheets Level Chiplet Power Models
- Convert System Level Power data to UPM
- IC Power Modelling tools can be reused
- Define System Usage Scenarios

Accuracy	C	a	I_static
Rough	Circuit Area & Fab Tech Comparison	Mode of Operation	Transistor widths
Accurate	Extract Layout	Snippets of actual workload	Vector-based dc simulations

Normalization of Power to same P, V, T, f is tedious but needed



# zGlue OmniChip—Power Test Case



## Chiplets Included

- CortexM4 MCU + BLE
- Temperature Sensing
- Vibration, Steps (Accelerometer)
- Roll and Pitch (Compass)
- Battery Recharging
- Heart Rate Sensor

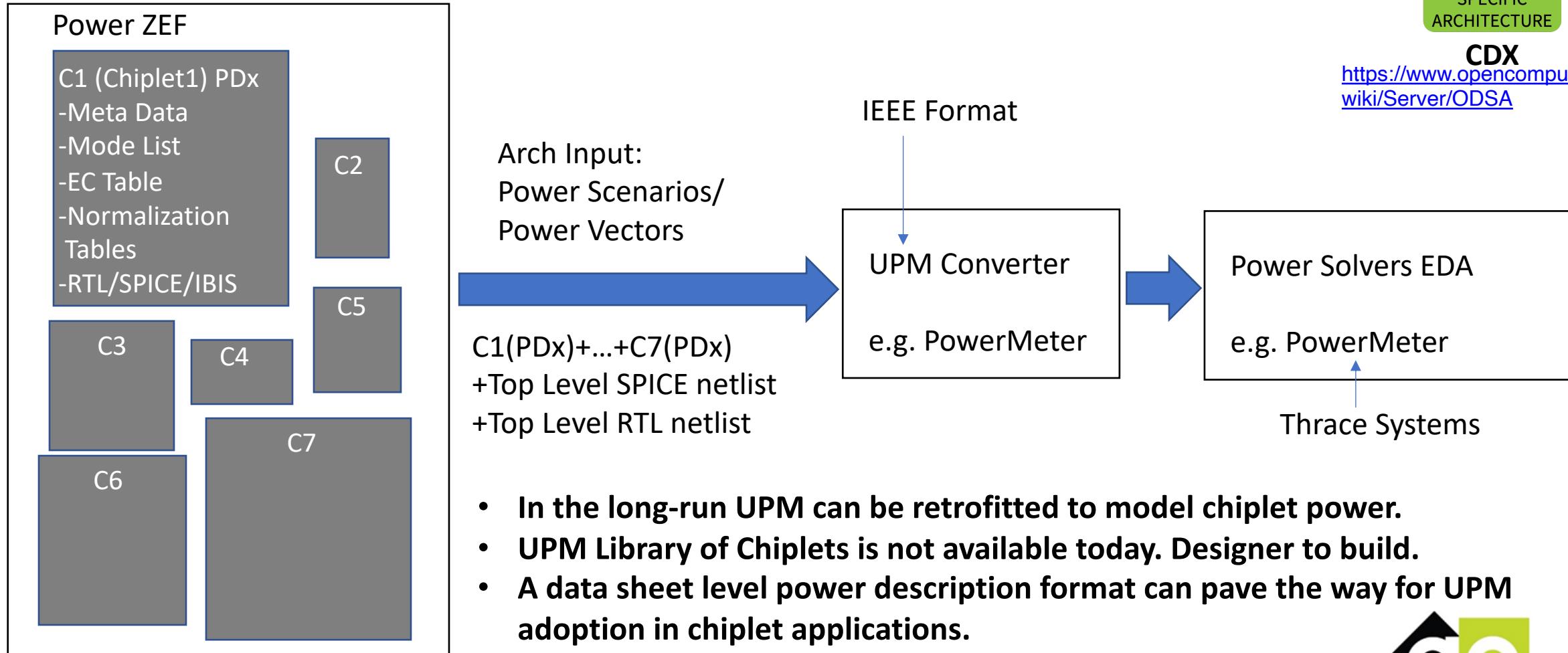
# Chiplet Power Description (Power ZEF)



OPEN DOMAIN  
SPECIFIC  
ARCHITECTURE

CDX

[https://www.opencompute.org/  
wiki/Server/ODSA](https://www.opencompute.org/wiki/Server/ODSA)



Please Do the Homework to Understand Power ZEF



# Chiplet Power Description (Power ZEF)



OPEN DOMAIN  
SPECIFIC  
ARCHITECTURE

CDX

ZEF is like LEF and DEF. This format is being developed to model mech, io, power, arch modeling of chiplets.

Power ZEF digitizes power information from datasheets and includes the following fields

- 1- Meta Data—Identifies chiplet, Voltage Domains, Abs Max, No of Modes
- 2- Mode Table—Identifies modes of operation with PVT and other environmental conditions
- 3- EC Table—Includes Min, Typ, Max values of current draw against various test conditions
- 4- Normalization Tables—Include current-draw normalization for voltage, temperature, frequency, and other operating conditions for all modes.

<https://github.com/zglue/ZEF>



# Chiplet System Power with ThraceSystem's PowerMeter™

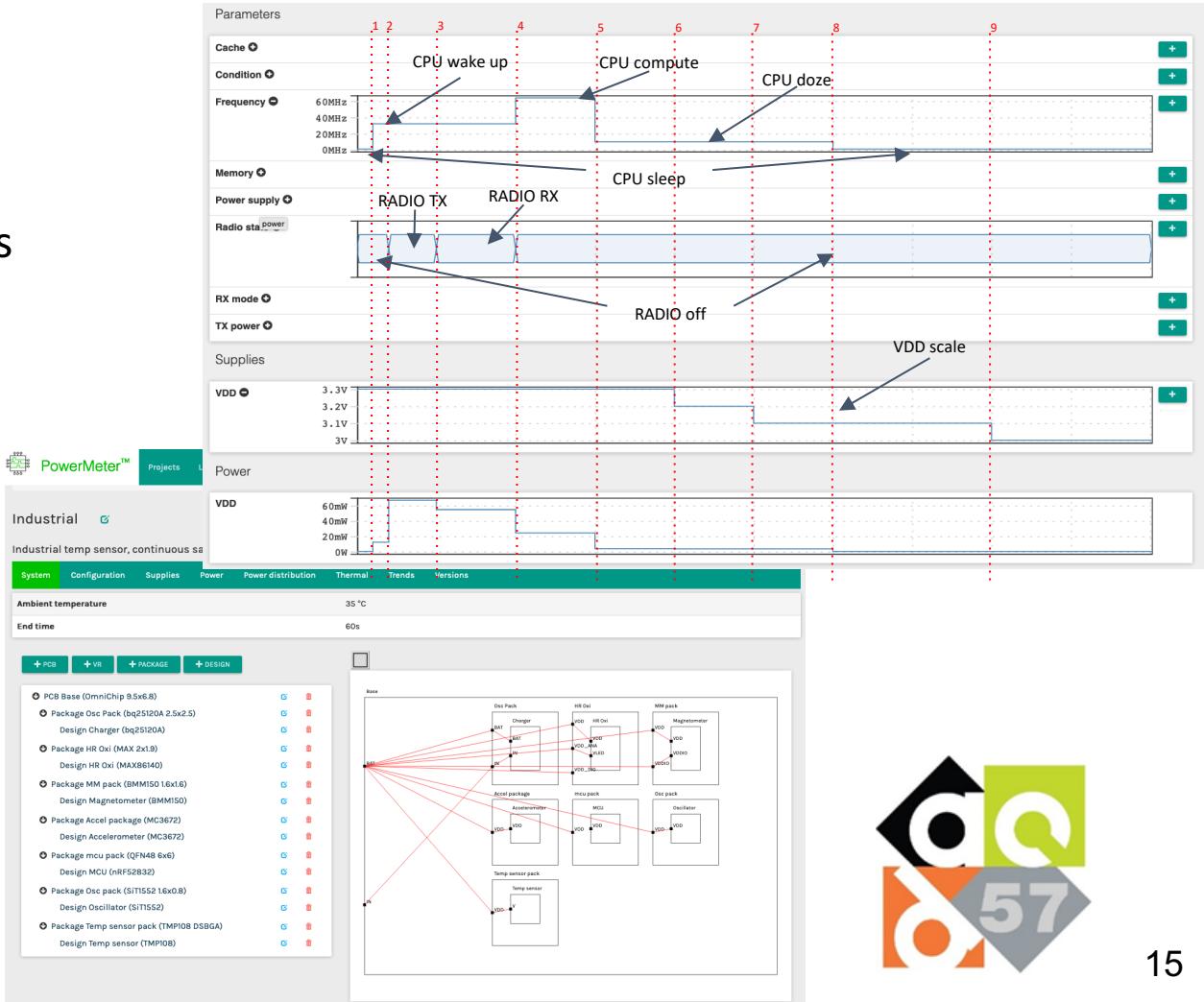


OPEN DOMAIN  
SPECIFIC  
ARCHITECTURE  
**CDX**

- PowerMeter has been built to handle any type of System Power definition
  - Liberty, UPM, Datasheet
- Easily specify custom Scenarios for power analysis
- Model the product as a complete interconnected system
  - From Gates to Board level, including Voltage Regulators
  - Power and Thermals
- Open API for flow integration



Slide Courtesy  
ThraceSystems



# Unified Power Models – UPM/2416

- **System level power model standard**

- Developed by Si2 and standardized by IEEE as 2416-2019
- Modeling flexibility with multiple standard data representations
- Supports system level power analysis with high level power models



- **Standard format** for internal & external models saves resources

- *Common language* facilitates efficient data exchange
- No need to support or translate external proprietary formats
- Avoids obsolescence trap of reliance on internal proprietary formats

- **Multi-level models ensure consistency from systems to gates**

- **P, V, T independent power models** save resources

- No need to build different libraries at different pVT corners

Slide Courtesy Si2

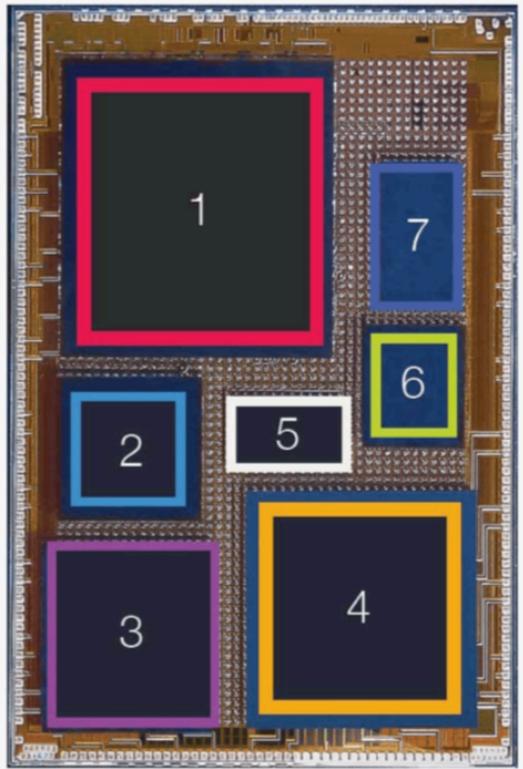
**Bold Items** are industry firsts





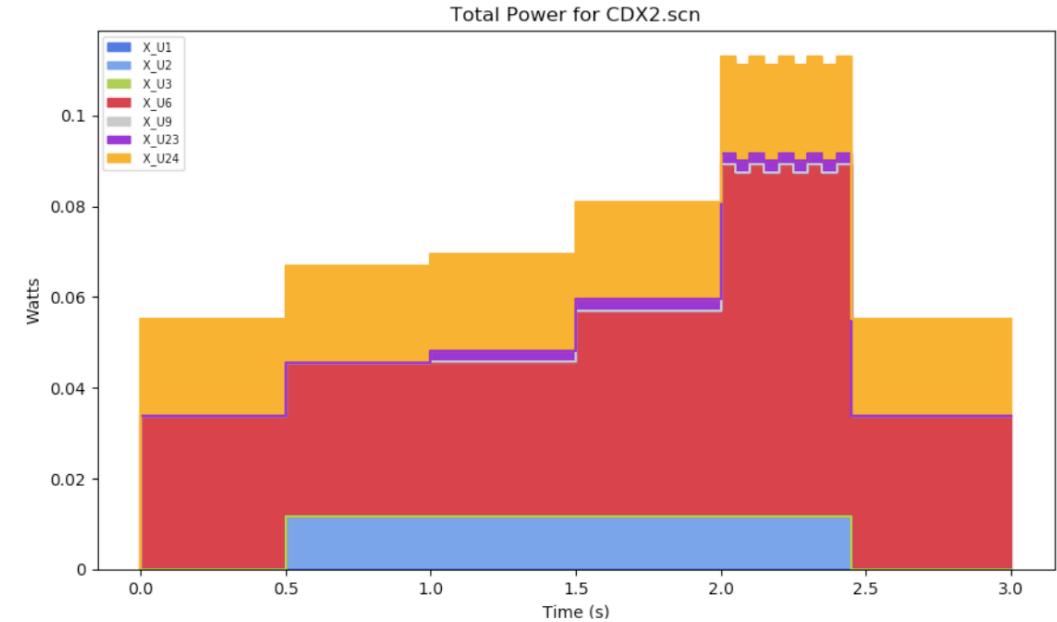
OPEN DOMAIN  
SPECIFIC  
ARCHITECTURE  
**CDX**

# UPM Example: 2.5D Chiplet Design



zGlue OmniChip

- 1 Nordic nRF52832 MCU with BLE
- 2 Bosch BMM150 Magnetometer (direction detection)
- 3 Maxim MAX86140 Heart-rate monitor/optical pulse oximeter
- 4 Texas Instruments BQ25120A Battery charger
- 5 Texas Instruments TMP108 Temperature sensor
- 6 mCube MC3672 Accelerometer (motion detection)
- 7 SiTime SiT1552 32 kHz oscillator



Slide Courtesy Si2

Design info courtesy of zGlue, Inc.



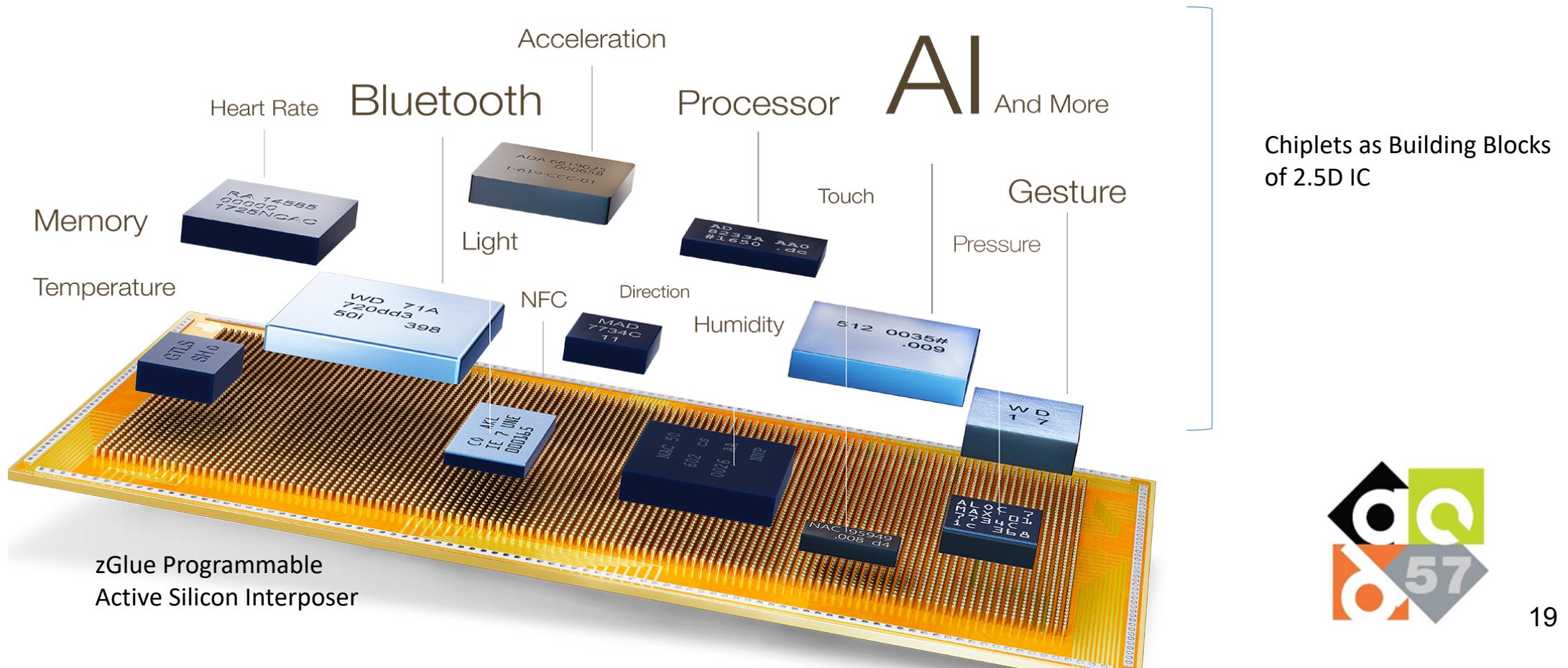
# Active Silicon Interposers

- Advanced Power Management – fine grain and adaptive
- Embedded Battery Management – adaptive and training based
- Embedded Sensing and Edge Processing – training based
- Over the Air updates and circuit updates
- Dynamic Circuit Adaptation
- Security Signature Detection

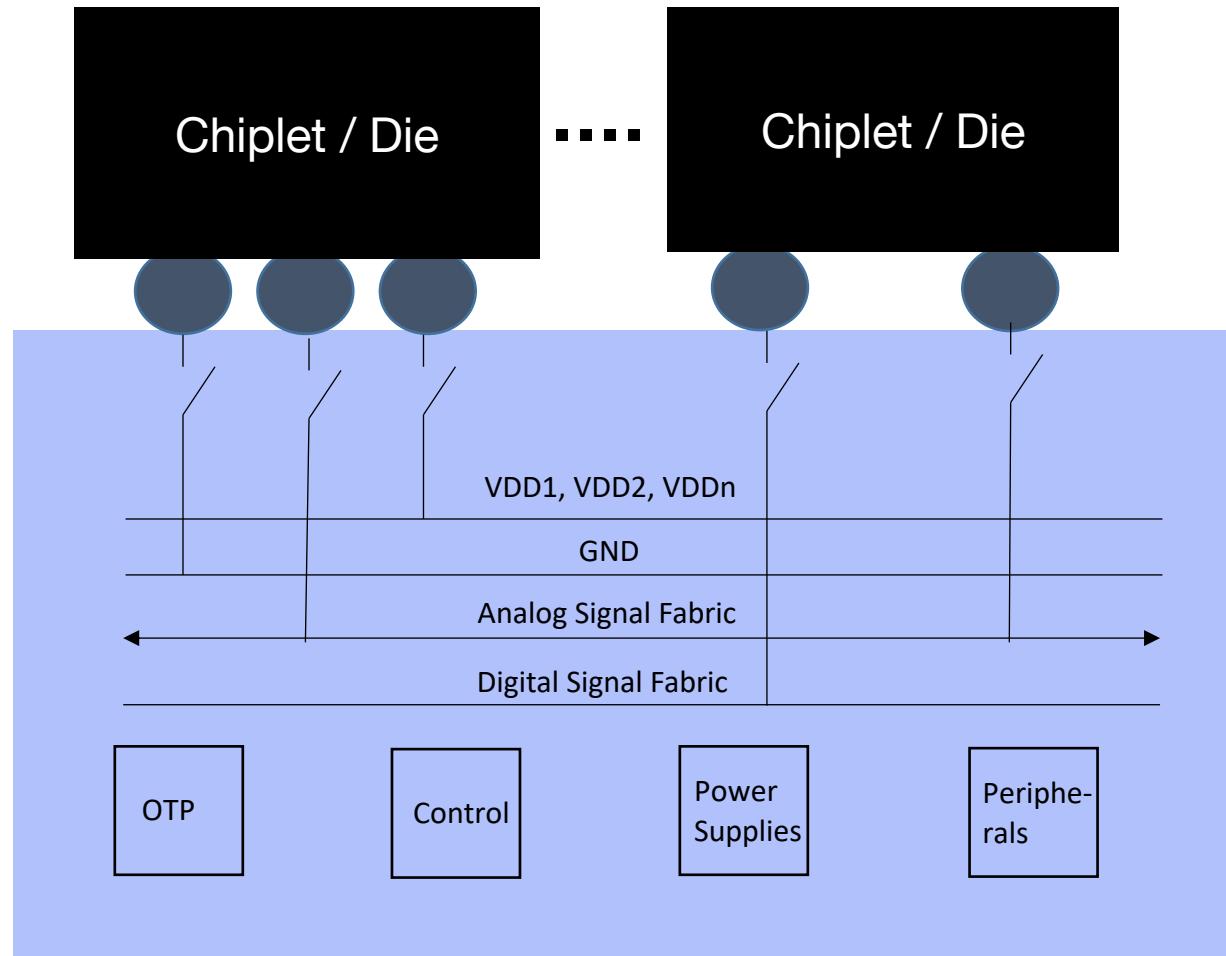


# zGlue “Active” Silicon Interposer Systems

zGlue's interposer technology addresses the affordability and quick development of chips by utilizing chiplets, which are used as lego blocks assembled on a base chip, all connected together using programmability in silicon and a cloud-based design software. zGlue uses programmability in silicon in a way similar to what FPGAs provide -- but instead of using an array of programmable gates, we allow programming inter-chiplet connectivity, chiplet power delivery, security, and self-test-and-repair functions.



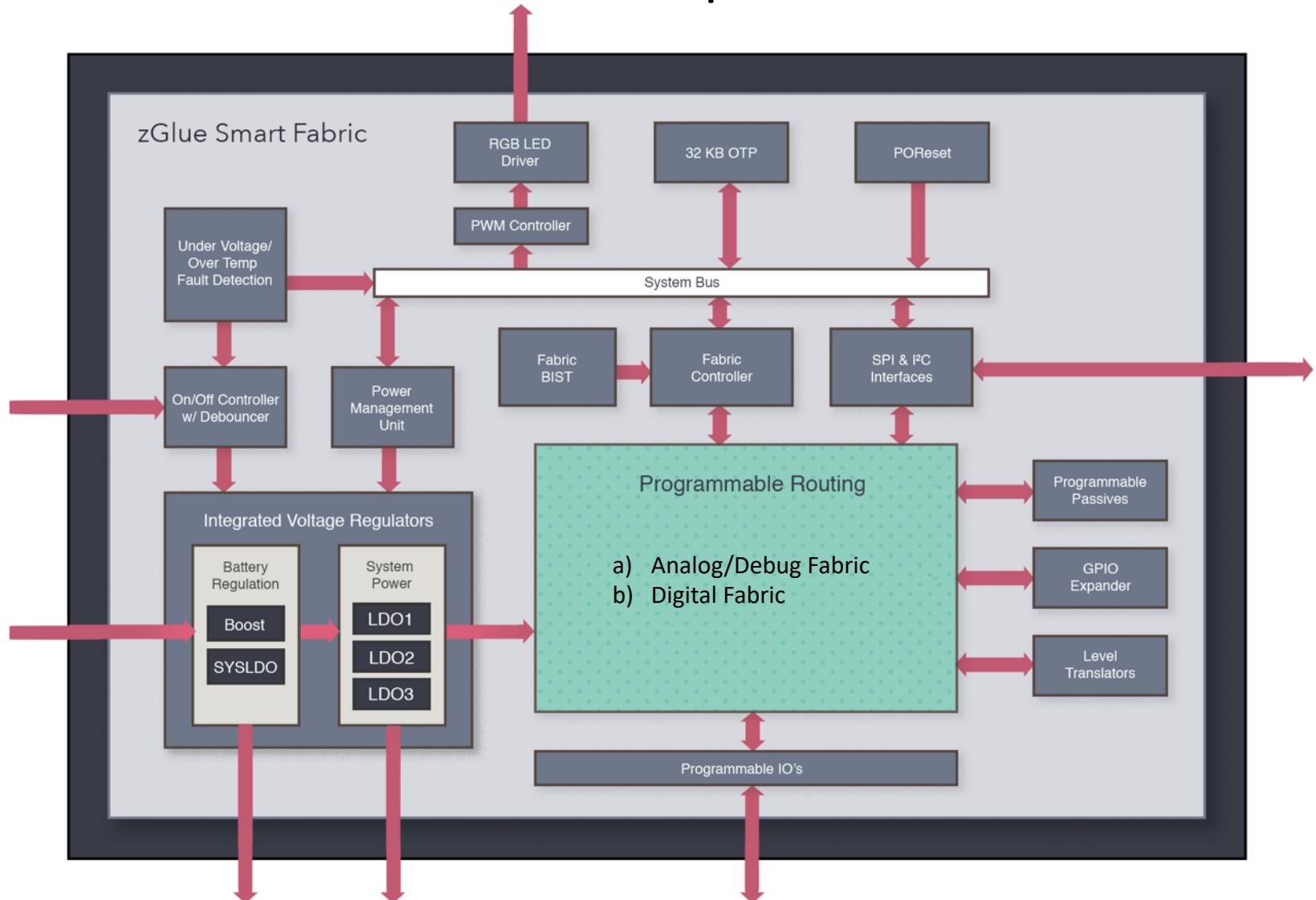
# zGlue Integration Platform (ZIP)



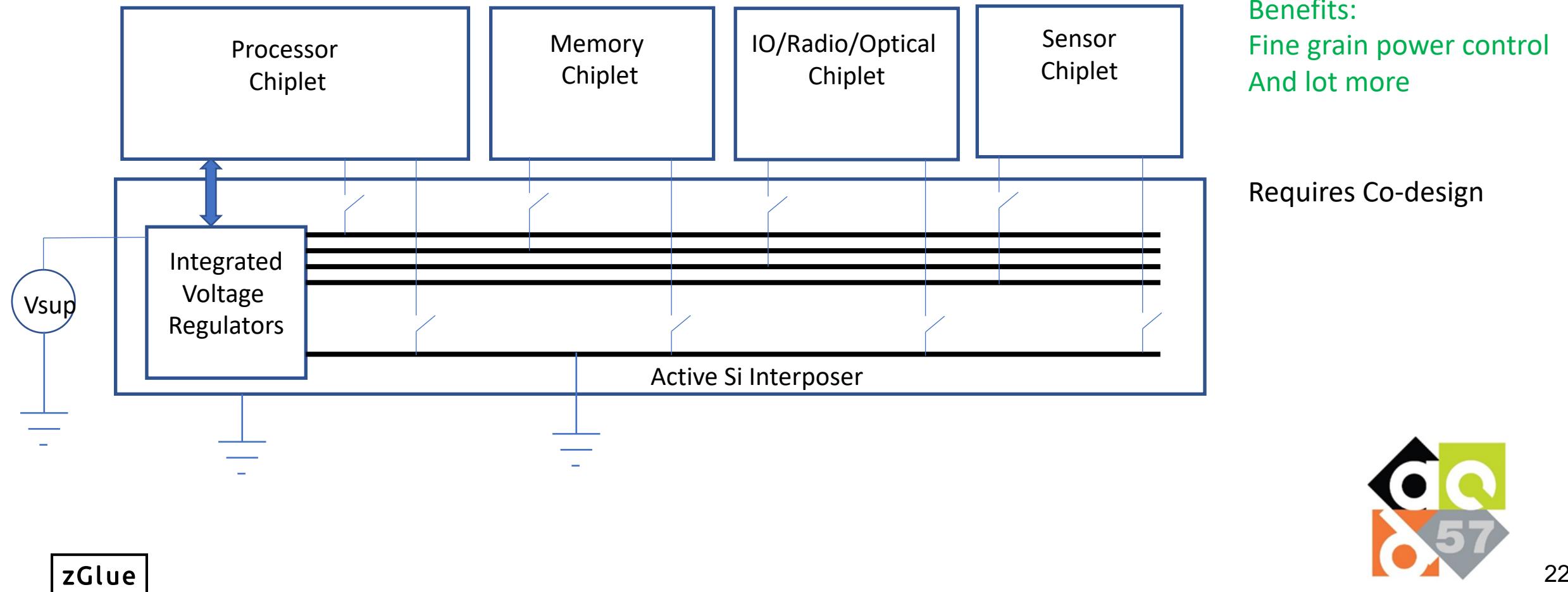
# zGlue Smart Fabric “Active Interposer”

## Embedded Functions:

- Built in Self Test and Repair
- Power Management Circuitry
- Voltage Regulators
  - LDO VR
  - Boost VR
  - Bypass Circuitry
  - Undervoltage Detect
- OTP Memory to store program and keys
- LED Drivers
- Fabric Controller
- Programmable Resistive Terminations
- GPIO Expander
- Level Shifters
- Programmable IOs



# Advanced Power Management in Active Silicon Interposers



# Summary

- 1- Power planning involves power modeling, design of power distribution, and PISI checks.
- 2- Early and accurate Power Estimates are key to selection of thermal solution for die stacking and side-by-side chiplet placement.
- 3- A power description of chiplet components is required. The example presented uses datasheets as a source for the power description at early design stage. A UPM based detailed power description is required at a later stage for accurate modeling especially for front-end chiplets.
- 4- Power modeling of passive Integration of Chiplets is similar to MCM design.
- 5- Active Si Interposers will be needed for advanced power management and performance designs.

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<https://dac2020.pathable.co/organizations/aKPenY37tCNL9WMG5>





Thank You Very Much

# HOMEWORK ASSIGNMENT

## Design Heterogeneous ICs with Chiplets – A Power Perspective

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<https://dac2020.pathable.co/organizations/aKPenY37tCNL9WMG5>

## Tutorial Homework Reference Material

zGlue OmniChip:

Overview: <https://zglue.com/products/omnichip>

Collaterals: <https://zglue.com/oci/project/omnichip>

Design Files: <https://zglue.com/applications/2647>

Supporting Material for DAC Tutorial: [https://drive.google.com/drive/u/1/folders/1liOxbHKNkF9jDC84DxXbXMkFnFpwKR\\_v](https://drive.google.com/drive/u/1/folders/1liOxbHKNkF9jDC84DxXbXMkFnFpwKR_v)

zGlue University Courses: <https://zglue.com/university>

zGlue Chiplet Library: <https://chipletstore.zglue.com/products/chipletstore>

zGlue ChipBuilder: <https://chipbuilder.zglue.com>



# Homework

1- Review OmniChip: <https://zglue.com/products/omnichip>

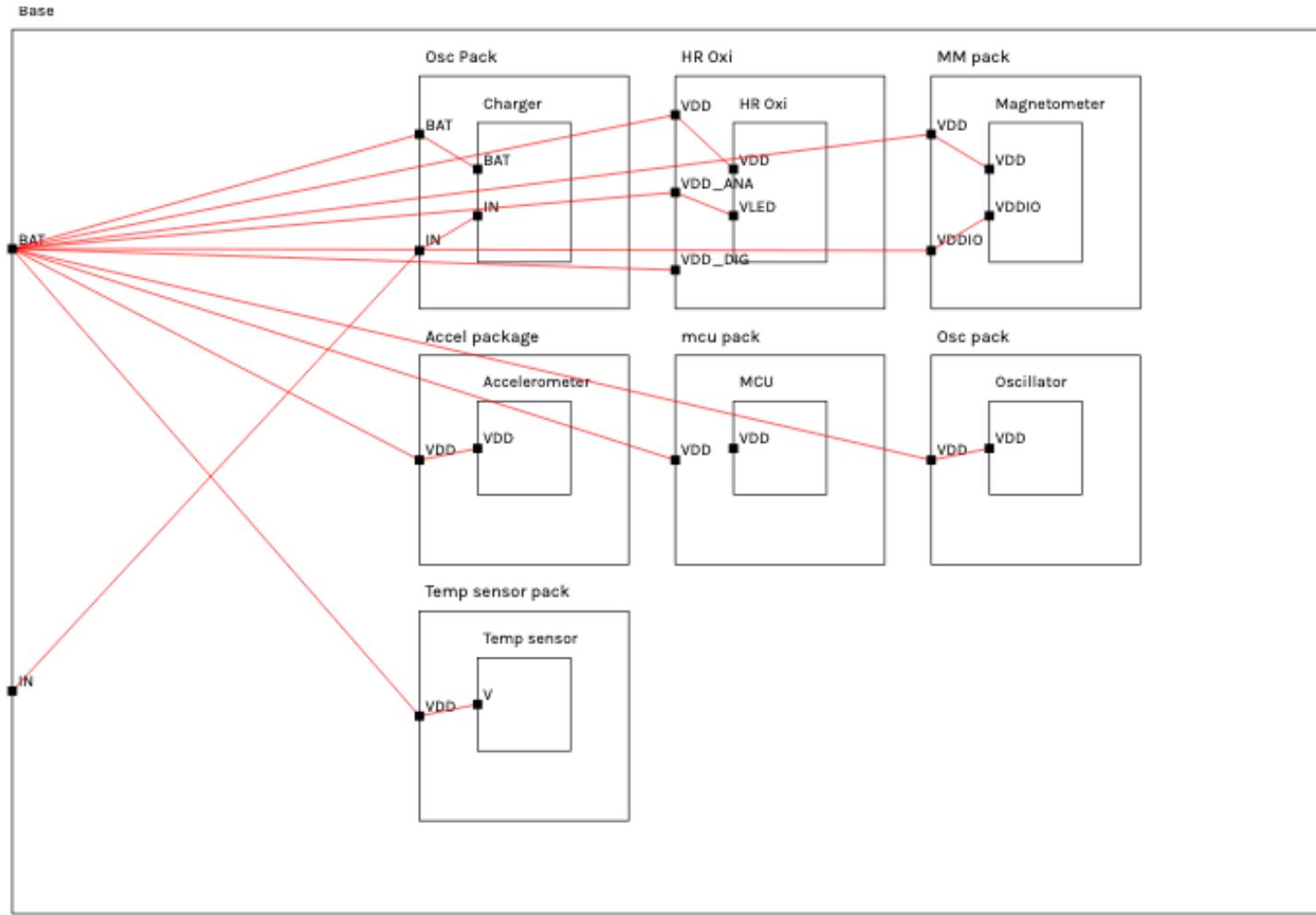
- a) How many chiplets are in this system?
- b) List each chiplet in OmniChip and its function

Chiplet Name	Function



# Homework

What power source is the V pin of TMP108 connected to?



# Homework

3- Open OmniChip Design in ChipBuilder. (You will need to login. Setting up an account is free but required for security reasons. Proper identification and 2FA security is required for pro features. Third party logins (FB, Goog, in) are supported. Chrome is the ONLY supported browser. Incognito not supported)

a) Visit: <https://zglue.com/applications/2647>

b) Login and you should land at  
<https://chipbuilder.zglue.com/system/2647>

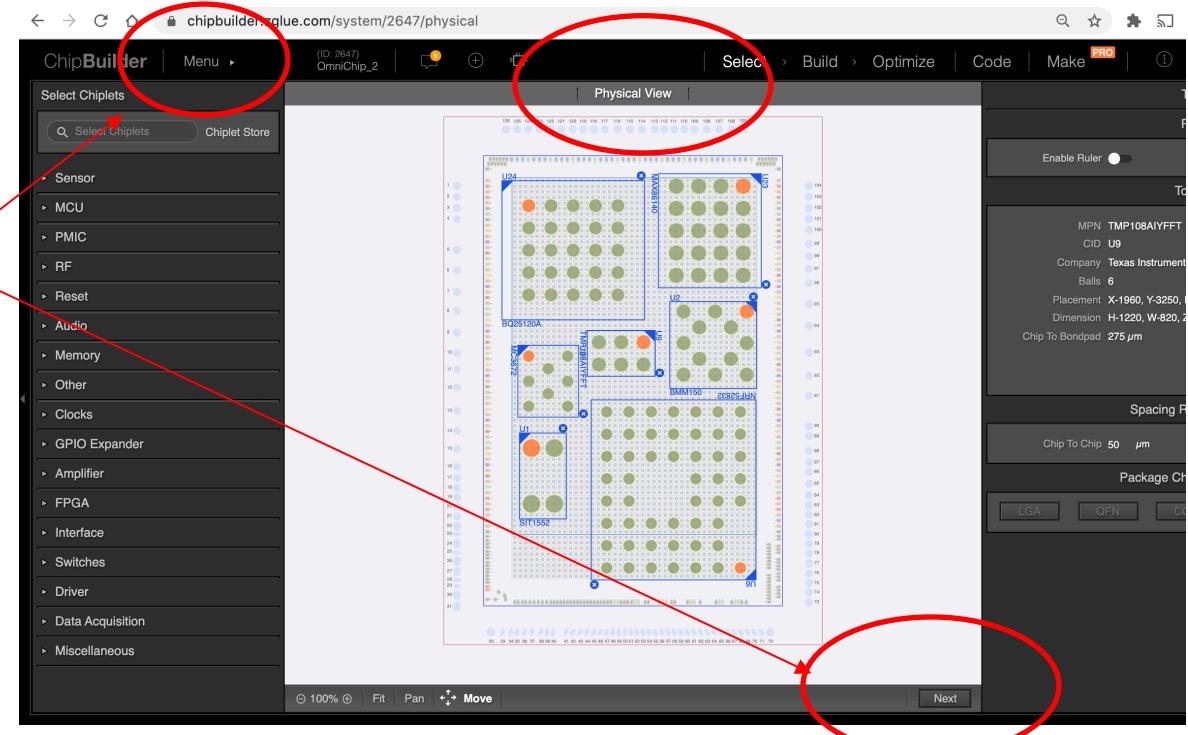
c) Click Next and go to Schematic View. Keep clicking next until you get to 3D view. Rotate it around. What kind of Package stack up is used?

d) What kind of package is used for OmniChip? QFN, LGA, BGA?

e) What are the dimensions of package substrate of OmniChip, x, y, z?

f) Do you think OmniChip needs a heat spreader or heatsink?

g) 'Save As' your own copy and modify the design. OR create a new one and play with chiplet based design.



<https://zglue.com/university/curriculum/chipbuilder-quickstart-tutorial/1>

# Homework

3- Download datasheet for TMP108

a) <https://chipletstore.zglue.com/products/chipletstore>

b) search for TMP108

The screenshot shows the zGlue ChipletStore homepage. At the top, there's a navigation bar with links for OCI (NEW), PRODUCTS, TECHNOLOGY, COMPANY, zGLUE UNIVERSITY, EN, and 中文. Below the navigation is a banner for "ChipletStore 2440" with the subtext "Explore our trove of 2440 to uncover the chiplet your design requires". To the right of the banner is a section titled "Why Become A Chiplet Vendor" with four numbered points: 1. Be part of zGlue rapid growing chiplet ecosystem, 2. List your chiplet portfolio with a personalized URL, 3. Control user access to your chiplet portfolio, 4. Receive business analytic information. There's also a "Find out more" button and a "Log In" button. On the far right, there's a "Chiplet Console" icon. Below the banner is a search bar containing the text "tmp108" with a magnifying glass icon and a "Search" button. To the right of the search bar are links for "Advanced Search", "Suggest new chiplet", and "Download chiplets as CSV". Below the search bar is a grid of category filters with checkboxes: Sensor (58), MCU (355), PMIC (722), RF (70), Reset (4), Audio (79); Memory (289), Other (13), Clocks (9), GPIO Expander (3), Amplifier (226), FPGA (31); Miscellaneous (29), Interface (146), Switches (292), Driver (72), Data Acquisition (100). At the bottom, there's a table with columns: Manufacturing Part Number, Manufacturer, Category, Description, Datasheet, and Select Chiplets. The first row shows the product details for TMP108AIYFFT by Texas Instruments under the Sensor category. The "Datasheet" column contains a blue arrow icon pointing to the right, and the "Select Chiplets" column contains an "Add" button.

Manufacturing Part Number ↑      Manufacturer ↑      Category      Description      Datasheet      Select Chiplets

Manufacturing Part Number	Manufacturer	Category	Description	Datasheet	Select Chiplets
1 TMP108AIYFFT	Texas Instruments	Sensor	Low Power Digital Temperature Sensor With Two-Wire Serial Interface In WCSP		Add

c) download datasheet



# Homework

4- Take a look at the TMP108 datasheet and answer the following questions

- a) How many Vdd rails are there?
- b) What are the min, typ, and max values of Vdd?
- c) What kind of IO does this chip use?
- d) What is the power issue with Open Drain IOs? (this is generic question)
- e) How many modes of operation can you count for this chip?
- f) What is the shutdown current for this chip at 1.8V and 25C? See page 4
- g) What is the quiescent current changing with the I2C frequency. What is the reason for steep current increase with frequency?
- h) What is the shutdown current for this chip at 3.6V and 125C? See page 8--this is the normalization data
- e) Now try to read the power ZEF file for TMP108 at

[https://docs.google.com/spreadsheets/d/1V-xcuTvl\\_RY945oZrovVbi16B3S1EK3PhcxuThgoMfY](https://docs.google.com/spreadsheets/d/1V-xcuTvl_RY945oZrovVbi16B3S1EK3PhcxuThgoMfY)

Note the four sections, meta data, modes of operation, EC table, and normalization data. This is an encoded form of the power information provided by the chiplet vendor converted to a machine-readable format. Power solvers can read and make use of this data to calculate different scenarios.



## Homework

5- What is the most power hungry condition of TMP108 that a designer should avoid to reduce power dissipation.

- Create a power dissipation scenario assuming OmniChip is used in an industrial tracker. Assume a worker wears it 8 hours in a industrial setting lifting moving 10 boxes an hour. The tracker is used to monitor the movement activity for box counting.



## Homework

6- If power modeling of OmniChip intrigues you, download its collaterals from  
[https://drive.google.com/drive/u/1/folders/1liOxbHKNkF9jDC84DxXbXMkFnFpwKR\\_v](https://drive.google.com/drive/u/1/folders/1liOxbHKNkF9jDC84DxXbXMkFnFpwKR_v)

You will notice that the low-hanging fruit in the power dissipation are the radio transmission in the MCU. See if you can spot it.

Try to make Power zef files for other 6 chiplets.

Use the power profile estimates and with the help from a thermal modeling tool, simulate power dissipation profile. Use the STEP files in the folder.

Make a data-driven decision on what kind of thermal cooling solution is appropriate for this chip.

Assume a 200mAh battery and estimate if that battery can last for one day for your scenario in #5.

If you need help, contact [jawad@zglue.com](mailto:jawad@zglue.com). Email the completed homework assignment  
if you want it graded and want feedback.

