https://sites.google.com/site/mazdaecutechnicaldata/ics

D151811-0360

Denso D151811-0360 8bit ADC with serial interface

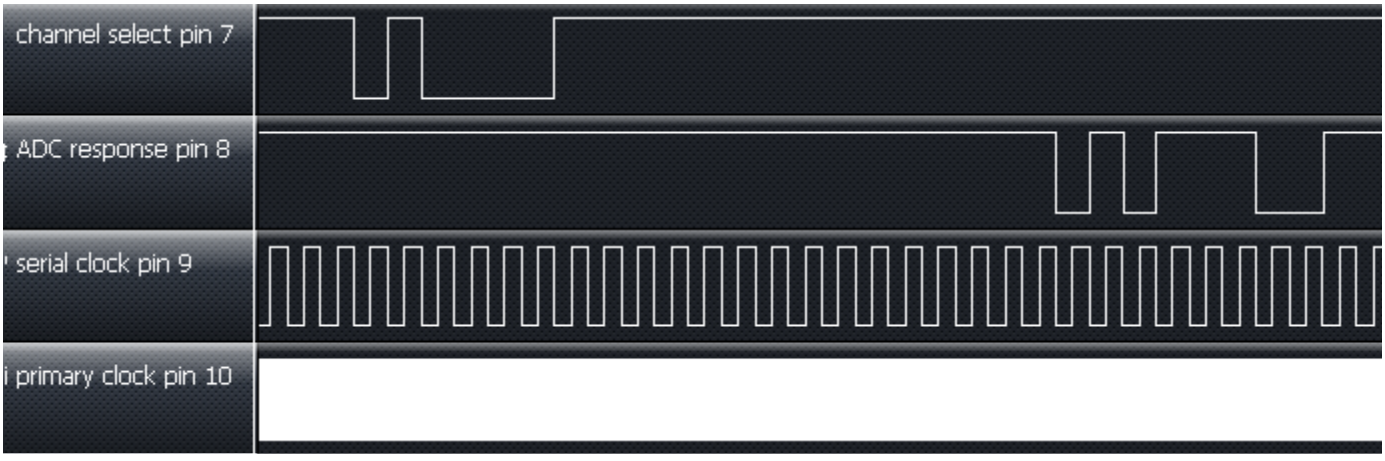
ADC requires a 1MHz 50% duty cycle wave on pin 10.

Channel number control signal on pin 7, ADC reading output on pin 8 works in sync with 62.5KHz serial interface clock 50% wave which should be provided on pin 9.

Control input line should be high while idle, high signal is logical 1 and low signal is logical zero. To request ADC reading, you send the chip 6 bits: logical zero (low) bit followed by a logical 1 bit (high) and four bit channel number (least significant bit first)

Data output line is high while idle. ADC response consists of 9 bits: low bit to indicate the response start and 8 bits of data, least significant bit first. All bits low mean zero voltage and all bits high mean +5v.

Here in example of a valid Request/response sequence:
here channel 15 reading is requested (pin 28) and 3v result is returned:



pin 1 ? optional, +5v in some applications
pin 2 ? optional, +5v in some applications
pin 3 +5v

pin 4 ADC channel 0
pin 5 ADC channel 1
pin 6 ? optional, +5v in some applications
pin 7 serial interface control input
pin 8 serial interface data output
pin 9 serial interface clock, 62.5 KHz, 50% duty cycle
pin 10 primary clock, 1 MHz, 50% duty cycle
pin 11 ground
pin 12 ?
pin 13 ? optional, ground in some applications
pin 14 ? optional, ground in some applications
pin 15 ADC channel 2
pin 16 ADC channel 3
pin 17 ADC channel 4
pin 18 ADC channel 5
pin 19 ADC channel 6
pin 20 ADC channel 7
pin 21 ADC channel 8
pin 22 ADC channel 9
pin 23 ADC channel 10
pin 24 ADC channel 11
pin 25 ADC channel 12
pin 26 ADC channel 13
pin 27 ADC channel 14
pin 28 ADC channel 15