**PROJECT SELECTION:**

1. **User can select core, ISA, and extensions**

* User can select bits 32 or 64
* User can select extensions” M”,” F”,” C” where “I” is selected by default

1. **User can select devices**

* User should at least select 1 device (GPIO, SPI, UART, 12C, TIMER, SPI Flash)

1. **User can select Bus interconnect**

* User can select 1 bus interconnect (TL-VL, TLC, WISHBONE)

1. **After selecting core, device, and bus interconnect user can finalize Soc**

* User can read code of chisel and user can edit code

1. **User can generate RTL**

* User can cancel RTL generating during process

1. **User can verify RTL**

* User can verify RTL by custom Test or predefine Test

1. **User can select test cases**

* User can select 1 or more test cases
* User can make their own test case by writing code in “C”
* User can run all test cases
* user can see the output (Test Pass or Fail)

1. **user can generate log and report**

user can export CSV

1. **user can run synthesis**

* user can open synthesis design
* user can set clock frequency
* user can select board\ FPGA
* user can select input output port

1. **user can generate bit stream**

* user can upload bit stream
* user can see result of FPGA (connected or not)
* User can select available programs
* User can upload program
* User can write program

**CUSTOM COMPONENT:**

1. **User can select components**

* User can select core (PREVIOUS REQUIRMENTS TILL FPGA)
* User can select peripherals

\* User can see all peripheral list

\* User can see and verify code

* User can select bus interconnect
* User can see input output diagram of components

**VERIFICATION:**

* User can select core and ISS
* Then user can select test cases more than 1 or also user can select all test cases
* User can also create their own test case
* User can run the selected test cases
* System will show the error report, if occur