Anew Scheme Sensorless Control of BLDC Motor Using Software PLL and Third Harmonic Back-EMF

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Abstract- **High performance sensorless permanent magnet brushless DC motor operation requires proper and precise commutation sequence. In general, the average torque falls rapidly as the rotor speed increases above the base speed, hence the motor will frequently be found to have insufficient torque at higher speed. One way to counter this problem is by using third harmonic back-emf detection technique during high speed operation because the third harmonic is usually kept a constant relationship with rotor position for any motor speeds and load conditions. Therefore, we could potentially avoid the torque deterioration which commonly occurs in traditional sensorless technique due to the delay of the phase angle between current and back-emf. Furthermore this method is practically free of noise which may be introduced from inverter switches. In this work, we propose a new software scheme of phase-locked loop (PLL) of third harmonic back-emf detection in order to accomplish a precise switching strategy for improving torque produced during high speed operation.**

Keyword- **brushless direct current (BLDC) motor, sensorless control, third harmonic back electromotive force (EMF), phase-locked loop(PLL).**

I. INTRODUCTION

PM Brushless Motor has many sensorless drive solutions have been offered to eliminate the costly and unreliable position sensor for BLDC motor with trapezoidal back-EMF. These methods are described with details in [1]. However most of this work has a problem at low speed. However at rated speed and torque, the current is at the rated value and in full space quadrature with respect to rotor flux vector. At Speed above the rated speed, the commutation of the BLDC drive is significantly retarded due to freewheel diode conduction appear in the terminal voltage of the unenergized winding this will case low power factor, low output power capability furthermore X_s increases due to increasing frequency. This will cause undesired phase angle commutation when integrating sensorless depend on terminal voltage of unenergized phase. In addition, the advance angle commutation varies with motor parameter, speed and load condition. Hence it is out of control [3]. In case of retarded phase angle commutation the motor torque deteriorates at high speed. So the third harmonic based sensorless control is proposed for high speed operation. It should be pointed out that the third harmonic back-EMF has been used in sensorless control by detecting the zero crossing with a voltage comparator [4],[5]. Or by integrating the EMF and using a phase-locked loop (PLL) to keep the integration result being zero [3].Some preliminary results of this technique were reported in early paper. Whereas simulation and software PLL will be presented in this work.

II. SENSORLESS CONTROL USING THIRD HARMONIC VOLTAGE

Sensorless drive for PM BLDC motor required back-EMF to be indirectly measured. Basically all back-EMF based technique utilizes measured phase voltage which contains high frequency noise. Furthermore for heavy loaded motor and for large L/R electrical time, constant the zero crossing is not clearly appearing from phase voltage. Since the third harmonic of the back-EMF has three times greater frequency. This method is not sensitive to a time delay of low pass filter (LPF). Which is usually a problem of terminal voltage sensing method, the back-EMF can be represented using the Fourier series as:-

$$e_a = E_1 \sin\theta_r + E_3 \sin 3\theta_r + E_5 \sin 5\theta_r + \ldots \quad (1)$$

$$e_b = E_1 \sin(\theta_r + \frac{4\pi}{3}) + E_3 \sin 3(\theta_r + \frac{4\pi}{3}) + E_5 \sin 5(\theta_r + \frac{4\pi}{3}) + \ldots\ldots \quad (2)$$

$$e_c = E_1 \sin(\theta_r - \frac{4\pi}{3}) + E_3 \sin 3(\theta_r - \frac{4\pi}{3}) + E_5 \sin 5(\theta_r - \frac{4\pi}{3}) + \ldots. \quad (3)$$

Summing the three phase back-EMFs

$$e_a + e_b + e_c = 3E_3 \sin\theta_r + 3E_9 \sin 9\theta_r + \ldots\ldots \cong 3E_3 \sin 3\theta_r \quad (4)$$

Where e_a , e_b , e_c represent phase back-EMF, E_n represent n'th back-EMF harmonic.Assuming that inductance is constant at any rotor position due to surface-mounted permanent magnet motor topology, from the summation of three-terminal to neutral voltage, the third harmonic of the back-EMF can be derived as:

$$V_{sum} = v_{an} + v_{bn} + v_{cn} = (R + L\frac{d}{dt})(i_a + i_b + i_c) + (e_a + e_b + e_c)$$
$$= e_a + e_b + e_c \approx 3e_3 \sin 3\theta_r \qquad (5)$$

Where v_{an}, v_{bn}, v_{cn} are terminal to neutral voltage and i_a, i_b, i_c are phase current. The summed terminal voltage include only the triplent harmonics since the summation of the three phase currents is zero. The third harmonic voltage is an air-gap voltage component. And thus it is equal to the rate of change of rotor flux; therefore the integration of third-harmonic voltage gives the third harmonic rotor flux. It follow that zero-crossing of the third-harmonic rotor flux occur at 60 electrical degrees, which are exactly the desired switching instant(current commutation instant).thus the third-harmonic rotor flux(integrating third-harmonic stator voltage)is input to a zero-crossing detector and the output of the zero-crossing detector determine the switching function. "Fig. 1" shows the principle of the improved sensorless controller. In the steady state, the integration result of the third harmonic EMF, i.e. the net shaded area is zero. Thus, an inverter is switched off at 30 electrical degree prior to the occurrence of the back EMF zero crossing. Hence, normal commutation is realized. However, during the transient state, if the motor commutation is advanced, the integration result will be negative. This will reduce the input voltage of a voltage-controlled oscillator (VCO) in the PLL and consequently decrease the motor commutation frequency until the commutation is no longer advanced. In contrast, if the commutation is retarded, the integration result will be positive; hence the VCO input and motor commutation frequency will be increased until the commutation is no longer retarded. This is describe in [3] using hardware discrete component.

III. PHASE-LOCKED LOOP (PLL) ALGORITHM

"Fig. 2" shows the traditional block diagram for phase-locked loop [2] in discrete time. There are three function blocks in the signal flow diagram: a digital multiplier (phase detector), a digital filter and a voltage controlled oscillator (VCO). The input to the phase detector (PD) is the discrete third harmonic voltage $e_3(n)$ and square wave of the VCO, the output signal is denoted $e_{3i}(n)$ which is the multiplier of this two signal. The digital filter serves as loop filter, its output signal is $u_f(n)$. Finally, the VCO is supposed to generate a square wave output signal V_{CO}, at the sampling instants. The sampled VCO output signal is denoted $V_{CO}(n)$. The VCO is not able to compute signal directly rather this signal must be calculated indirectly from the phase $\theta(t)$ of the VCO instantaneous output angular frequency would be given by

$$\omega = \omega_0 + k_0 u_f \qquad (6)$$

Where ω_0 is the center (angular) frequency of the VCO

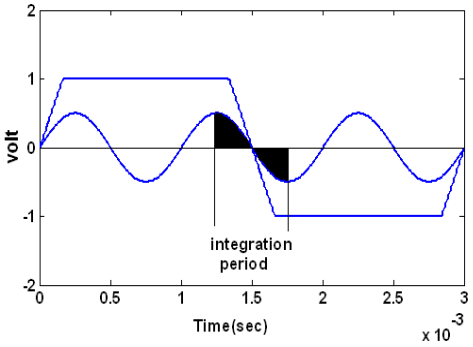

Figure 1. Back-EME and third harmonic

and k_0 is the VCO gain, the continuous output signal $V_{CO}(t)$ then would be given by

$$V_{CO} = rec(\omega(t).t) \qquad (7)$$

Where rect denotes the square wave function; refer to equation (6).the total phase $\theta(t)$, VCO output signal then would be:

$$\theta(t) = \int \omega(t)dt = \omega_o t + k_o \int u_f(t)dt \qquad (8)$$

where the total phase $\theta(t)$ is used to compute the instantaneous value of the VCO output signal V_{CO} it follows from the definition of the square wave function that V_{CO} is +1 when the phase $\theta(t)$ is either in the interval $0 < \theta_2 < \pi$ or in the interval $2\pi < \theta_2 < 3\pi$; etc. In all other cases,$u_2(t) = -1$.this computation scheme have to be adapted to the time-discrete ,when the digital filter output signal $u_f(n)$ at sampling instant t=nT and assume it stays constant during the time interval nT < t < (n+1)T, the total phase of the VCO output signal will change by an amount.

$$\Delta\theta = [\omega_o + k_o u_f(n)]T \qquad (9)$$

In that interval, If the phase $\theta(n)$ at sampling instant t=nT were known, we would be able to extrapolate the total phase $\theta(n+1)$ at sampling instant t=(n+1)T from

$$\theta(n+1) = \theta(n) + [\omega_o + k_o u_f(n)]T \qquad (10)$$

Given $\theta(n+1)$, we can also extrapolate the value of $Vco(n+1)$ at t= (n+1) T,

$$Vco(n+1) = 1 \quad \text{if} \quad 2k \le \theta_2(n+1) < (2k+1)\pi$$
Or $Vco(n+1) = -1$ if
$$(2k-1)\pi \le \theta_2(n+1) < 2k\pi \qquad (11)$$

Where k= integer.

At a given sampling instant t= nT, the output signal $e_{3i}(n)$ of the multiplier has to be computed by

$$e_{3i}(n) = k_d . e_3(n) . Vco(n) \qquad (12)$$

Where K_d is the gain of the phase detector. Given $e_{3i}(n)$ a new sample of u_f (n) must be computed; the digital filter transfer function is given in reference [2] as:

$$F(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \qquad (13)$$

Here a_1, b_0, b_1 are the filter coefficients .transforming eq. (13) into time domain we get the recursion

$$u_f(n) = -a_1 u_f(n-1) + b_o . e_{3i}(n) + b_1 . e_{3i}(n-1) \qquad (14)$$

The total phase of the VCO output signal at the next sampling instant will be

$$\theta(n+1) = \theta(n) + [\omega_o + k_o u_f(n)]T \qquad (15)$$

When the algorithm is executed over an extended period of time, the values of $\theta(n+1)$ will become very large and could soon exceed the allowable range of a floating number in the processor used. To avoid arithmetic overflow, θ_2 is limited to the range $-\pi < \theta_2 < \pi$.

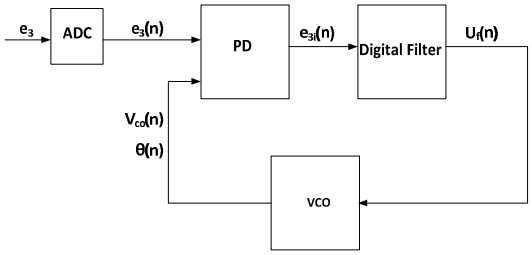

Figure 2. Block diagram showing software PLL arithmetic operation.

Whenever the computed value of $\theta_2(n+1)$ exceed $\pi, 2\pi$ is subtracted to confine it to that range. Now the value of $u_f(n+1)$ is easily computed by checking the sign of the range-limited total phase. If $\theta(n+1) \geq 0, Vco(n+1) = 1$; otherwise $Vco(n+1) = -1$ .Finally, the calculated values of $e_{3i}(n)$ are delayed by one sampling interval, i.e. $e_{3i}(n) \rightarrow e_{3i}(n-1)$

IV. Simulation Results And Discussion

"Fig. 3" shows the main block diagram for third harmonic sensorless control. The input to the low pass filter (LPF) is the third harmonic voltage"Fig.4" which is the voltage between neutral point of the motor and the star point of resistors this described in reference [5].The proposed sensorless control algorithm has been verified through numerical simulation and MATLAB simulation. "Fig. 5 and 6" illustrate the output of the phase –locked loop blocks which is performed in matlab simulink assume third harmonic voltage input(1 volt).the six step switching sequence of the motor is performed at each state change of the voltage controlled oscillator of the PLL which is occur at each peak of third harmonic voltage. This is used in conjunction with S-function to determine which two specific winding need two be excite. "Fig.7" shows the speed response while "Fig 8" show the current and phase-EMF at 10000 RPM with PI control strategy for the current.

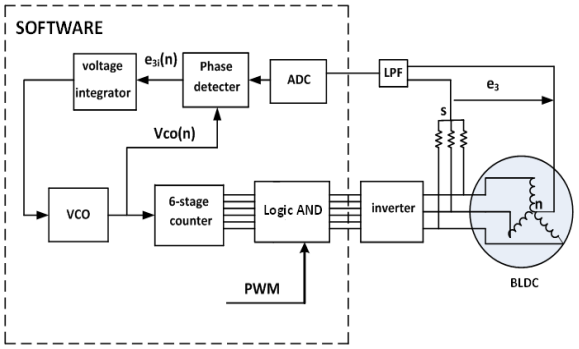

Figure 3.proposed sensorless controller

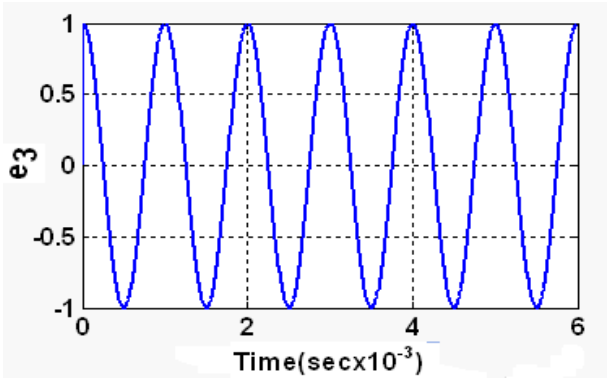

Figure 4.third harmonic voltage input to ADC

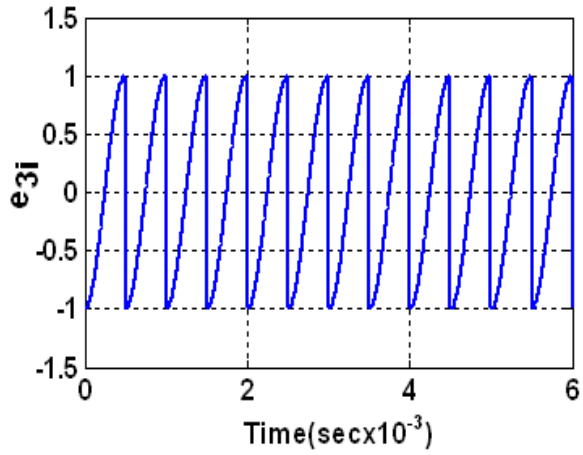

Figure 5. Phase detector output

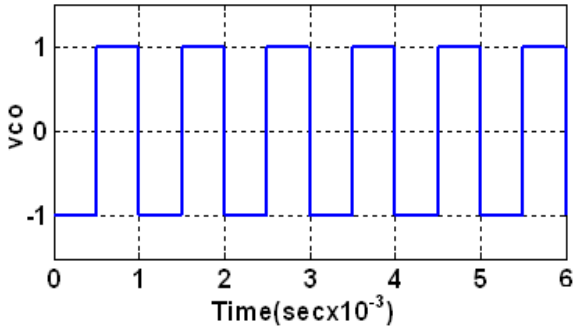

Figure 6. VCO output

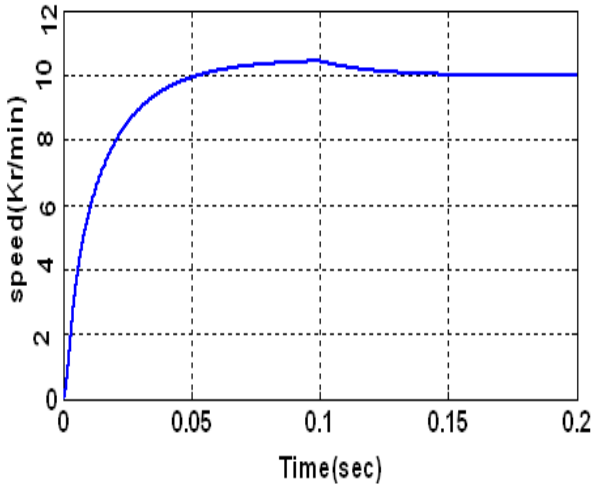

Figure 7. Speed response

both original and improved sensorless controller are investigated with the same parameter simulink and voltage source inverter,, if the normal commutation is achieved, the inverter switching status should change at the instant when the third harmonic EMF reaches its peak value(30 degree ahead of the main EMF). "Fig.8" show the waveform of main back-EMF and current when the motor operated with traditional sensorless controller at full speed(10000 RPM),as evident the motor commutation is retarded nearly by~10 electrical degree this is because a relatively wide voltage pulse due to the freewheel diode conduction.On the other hand, if the BLDC motor is operated with the improved controller at full speed, the retarding is significantly reduced to nearly 2 electrical degree as shown in "Fig. 9".this result prove that the improved controller is suitable for the full speed performance and will improve the motor performance at high speed.

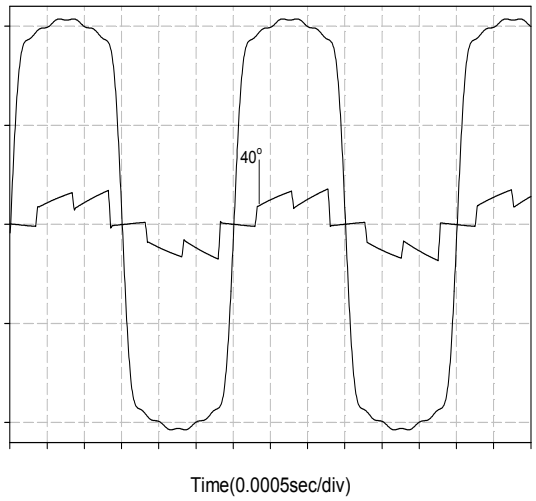

Figure 8. Waveform of the current and back-EMF with traditional Sensorless controller at 10000RPM,200 volt dc, EMF (50V/div), Current(4A/div)

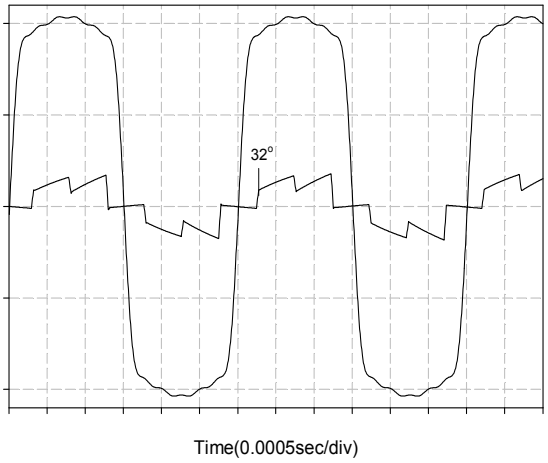

FIGURE 9. WAVEFORM OF THE CURRENT AND BACK-EMF WITH IMPROVED SENSORLESS CONTROLLER AT 10000RPM,200 VOLT DC, EMF (50V/DIV), CURRENT(4A/DIV

VI. CONCLUSION

The main objective of this work was to develop a brushless permanent magnet motor electronic commutation control that operates over a wide speed range with maximum motor efficiency. However at high speed the motor commutation is significantly retarded. in this paper an improved sensorless controller using third harmonic back-EMF with software phase locked loop has been developed to get precise commutation sequence. The validity of the proposed method is verified through matlab simulation , this result show a good improvement in commutation pulse at high speed thus the phase current is minimally delayed from the back-EMF ,and hence leading to improved power factor and higher torque production than those obtained using a conventional back-EMF zero crossing method.

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