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2/12/24

Postlab 03 (Timers)

1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt.

When I calculated for 4Hz I used the PSC value 7999 and ARR value 250. Using the same math that I used to get the 4Hz value we can get the values for the 60 Hz interrupt, which gives us the PSC value 7999 and ARR value 16.7 for 60 Hz interrupt.

2. Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function.

The following pins below are the ones that have the timer 3 capture/compare channel 1 alternate function.

- PA6
- PB4
- PC6
- PE3 – Can’t be used because it’s not on our board

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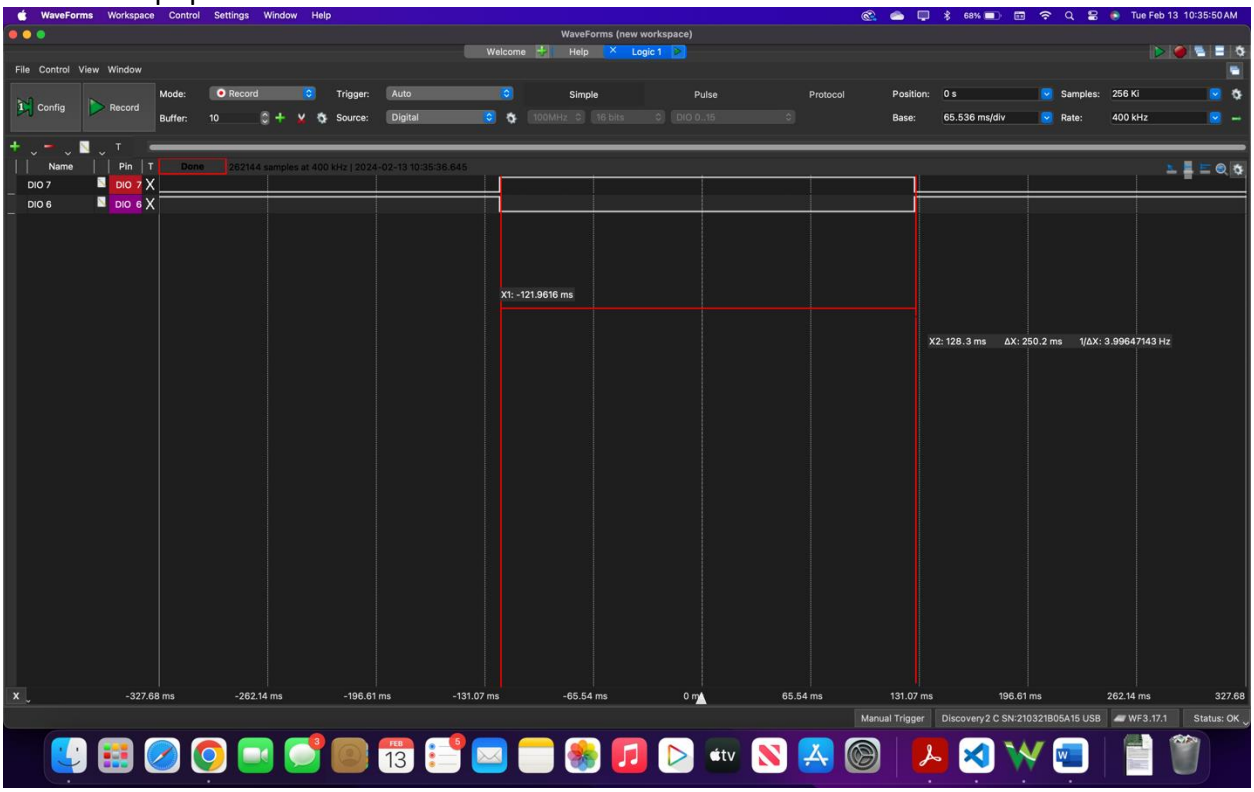
3. List your measured value of the timer UEV interrupt period from first experiment.

The measured value comes from the math 1/4Hz. This gives the measured value of the time UEV interrupt period as 250 milliseconds. This is shown in the screenshot below.



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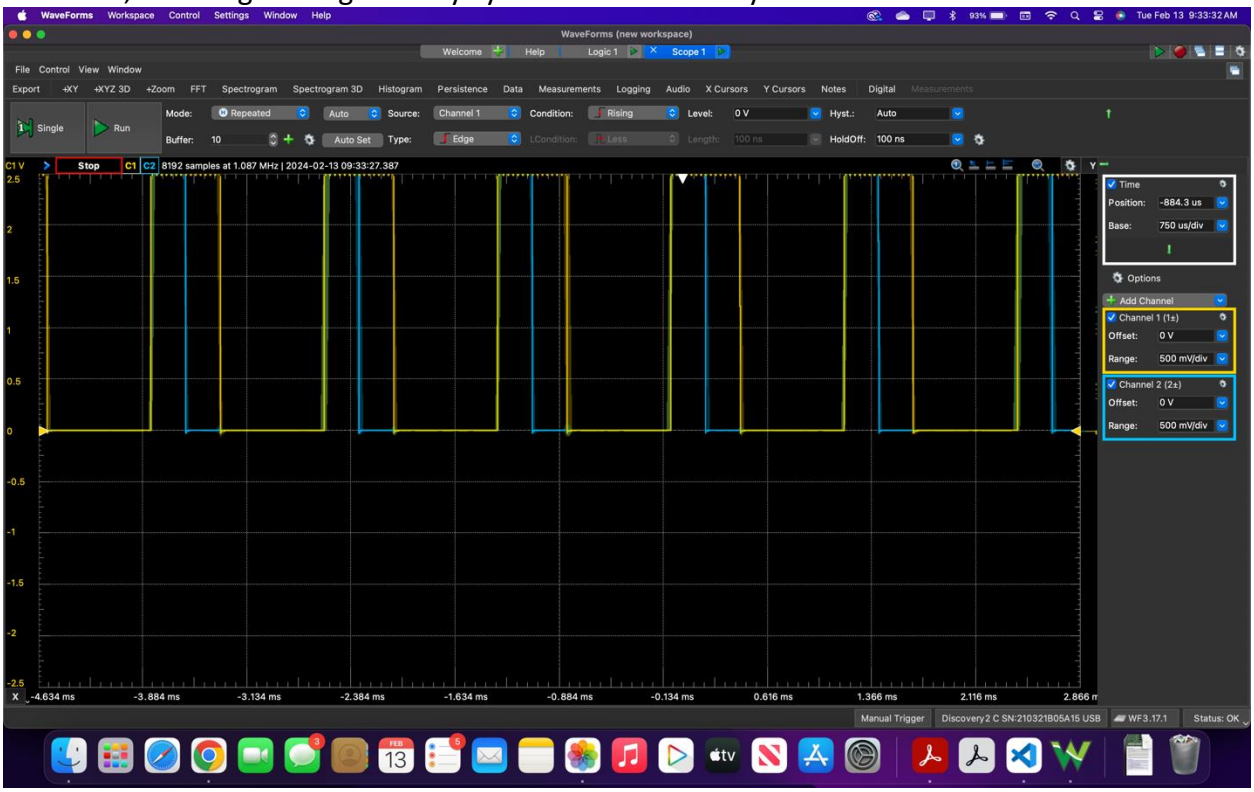
4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.

As the CCR1 value increases in the PWM mode 1, the portion of time the signal is high increases, resulting in a higher duty cycle. This is shown by the screenshot below.



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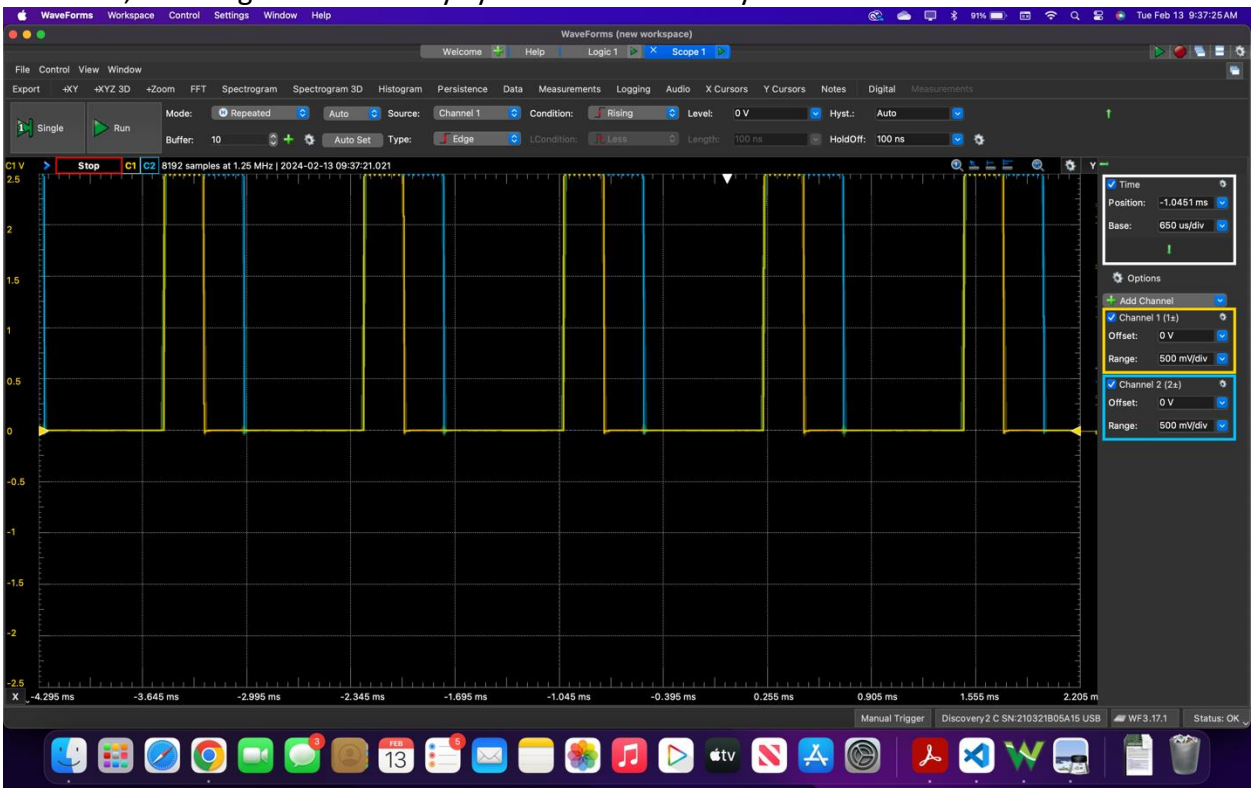
5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.

As the CCR2 value increases in the PWM mode 2, the portion of time the signal is high increases, resulting in a lower duty cycle. This is shown by the screenshot below.



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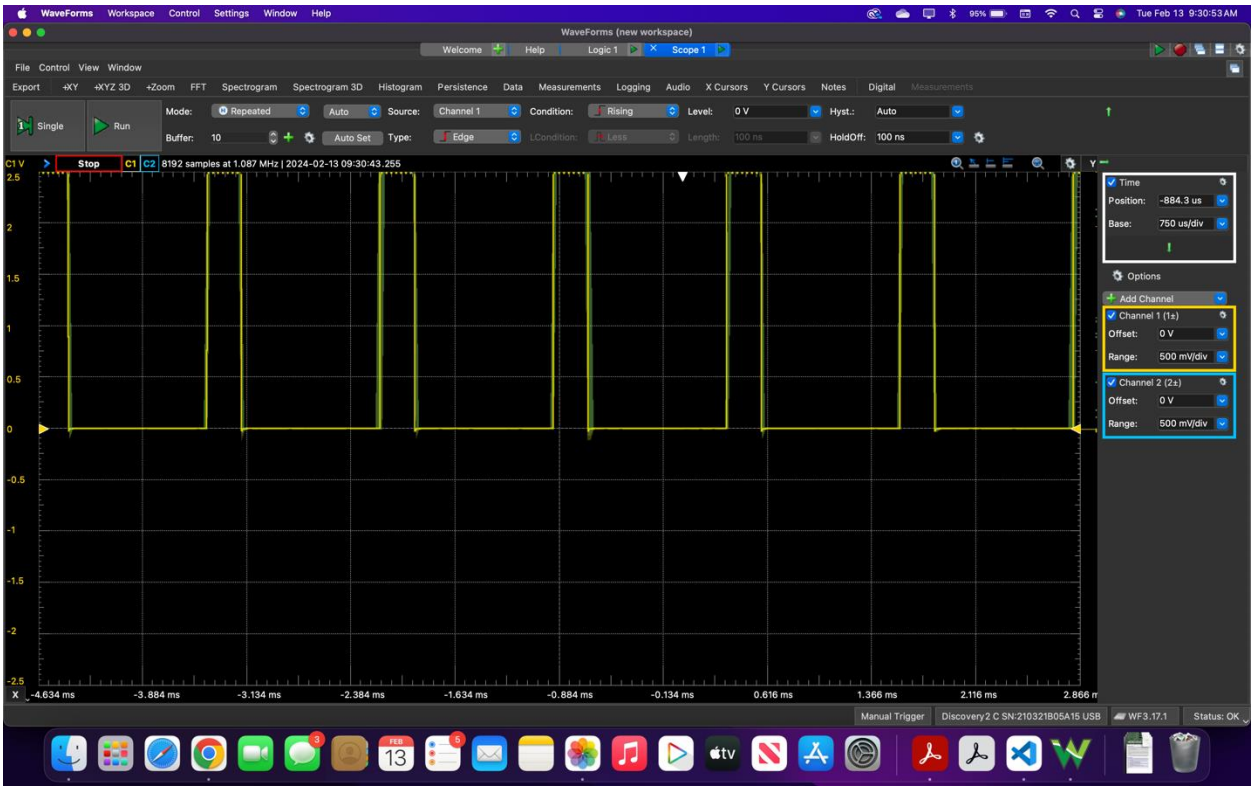
6. Include at least one logic analyzer screenshot of a PWM capture.

Here is the screenshot for when the capture/compare registers (CCRx) for both channels is set to 20% of the ARR value.



7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?

PWM mode 2 is shown in figure 3.6 of the lab manual.