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ECE 5780
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Postlab 02 (Interrupts)

1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?

PA0 and PC0 are mapped to EXTI line 0. Only one pin or group of pins can be assigned to a particular EXTI line at any given time. If you try to use both PA0 and PC0 for external interrupts simultaneously, you would run into conflicts because they are trying to use the same EXTI line.

2. What software priority level gives the highest priority? What level gives the lowest?

The software priority level 0 gives the highest priority. The software priority level with the highest numerical value gives the lowest priority, which in our case is 3.

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

Each IPR register contains four 8-bit regions to set the priority of an interrupt; the NVIC within the STM32F0 only has the uppermost two bits from these regions implemented, giving four possible configurable priority levels (0-3).

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

The latency between pushing the button and the LED change was 0.17 milliseconds. Screenshots of logic analyzer are shown on next page.

5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

You need to clear status flag bits in peripherals when servicing their interrupts so that the interrupt doesn't repeat continuously. If the status flag bit wasn't cleared the request would never get acknowledged as complete.

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