Project 1

CSc 137, Fall 2016, Faroughi

Due Oct. 3 in class

Problems 2.29 (b, d):

b: Use NOT and NAND primitive gates,

d: Enter the expression as is using the |, &, and ~ symbols as bit-wise logical operators).

Use the same test bench for both parts b and d. You would need to create two copies of the test bench module where in one copy you instantiate the module for part b and in the second test bench you instantiate the module for part d.

Project Report: Merge files including the simulation output into a single file separated by dash lines for clarity so the single combined file requires only a few pages to print (i.e., save papers). Submit your report containing also the following information:

a. Cover page with

   Name (legible)
   Section number (Sec 1: 3:00-4:15 or Sec 2: 5:30-6:45)
   Project number and title
   Semester (Fall 2016)

b. Analysis of the results. Show that test cases done by hand match those generated by simulating your Verilog code.