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Project 1

Verilog Model for $f = x\bar{y} + yz$

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Sec 2: 5:30-6:45
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2.29 b. Module

```
module Project1
(
        input x,y,z,
        output f
);
wire out1, out2, out3;
not  n1(out1,y);
nand n2(out2,out1,x);
nand n3(out3,y,z);
nand n4(f,out2,out3);
endmodule
```

2.29 b. Test Bench

```
`include "Project1.v"
module tester();
reg x,y,z;
wire f;

Project1 po(x,y,z,f);
initial begin
$display ("Time x y z  f");
$monitor ("%4d       %b", $time,f);
x=0; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test1
#1 //simulate
x=0; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test2
#1 //simulate
x=0; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test3
#1 //simulate
x=0; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test4
#1 //simulate
x=1; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test5
#1 //simulate
x=1; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test6
```

```
#1 //simulate
x=1; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test7
#1 //simulate
x=1; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test8
#1 //simulate
$finish;
end
endmodule
```

2.29 b Output

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Oct  4 18:33 2016
Time x y z  f
   0 0 0 0
   0        0
   1 0 0 1
   2 0 1 0
   3 0 1 1
   3        1
   4 1 0 0
   5 1 0 1
   6 1 1 0
   6        0
   7 1 1 1
   7        1
$finish called from file "project1_testBench.v", line 45.
$finish at simulation time                   8
           V C S   S i m u l a t i o n   R e p o r t
Time: 8
CPU Time:      0.520 seconds;       Data structure size:   0.0Mb
Tue Oct  4 18:33:10 2016
[bibodij@titan:39]>
```

……

2.29 d. Module

```
module Project1_AssignStatement
(
        input x,y,z,
        output f
);

assign f = ~y & x | y & z;
endmodule
```

2.29 d. Test Bench

```
`include " Project1_AssignStatement.v"
module tester();
reg x,y,z;
wire f;
```

```
Project1_AssignStatement po(x,y,z,f);
initial begin
$display ("Time x y z  f");
$monitor ("%4d       %b", $time,f);
x=0; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test1
#1 //simulate
x=0; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test2
#1 //simulate
x=0; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test3
#1 //simulate
x=0; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test4
#1 //simulate
x=1; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test5
#1 //simulate
x=1; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test6
#1 //simulate
x=1; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z);
//test7
#1 //simulate
x=1; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z);
//test8
#1 //simulate
$finish;
end
endmodule
```

2.29 d. Output

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Oct  4 18:54 2016
Time x y z  f
   0 0 0 0
   0        0
   1 0 0 1
   2 0 1 0
   3 0 1 1
   3        1
   4 1 0 0
   5 1 0 1
   6 1 1 0
   6        0
   7 1 1 1
   7        1
$finish called from file "project1_testBench.v", line 45.
$finish at simulation time                   8
          V C S   S i m u l a t i o n   R e p o r t
Time: 8
CPU Time:      0.540 seconds;       Data structure size:   0.0Mb
Tue Oct  4 18:54:53 2016
[bibodij@titan:41]>
```