10/5/2016

Project 1

Verilog Model for

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Sec 2: 5:30-6:45

Fall 2016

**2.29 b. Module**

module Project1

(

input x,y,z,

output f

);

wire out1, out2, out3;

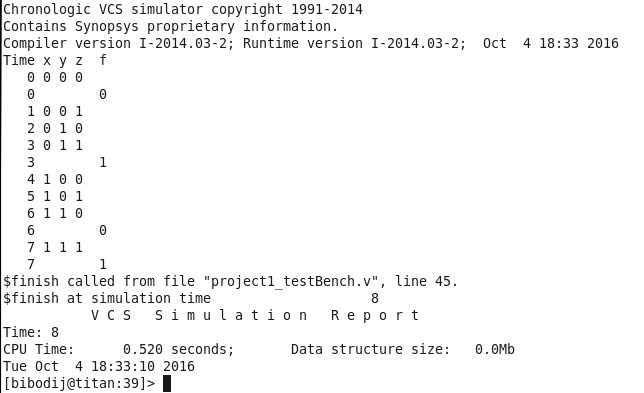
not n1(out1,y); nand n2(out2,out1,x); nand n3(out3,y,z); nand n4(f,out2,out3); endmodule

**2.29 b. Test Bench**

`include "Project1.v" module tester(); reg x,y,z; wire f;

Project1 po(x,y,z,f); initial begin $display ("Time x y z f"); $monitor ("%4d %b", $time,f); x=0; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test1 #1 //simulate x=0; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test2 #1 //simulate x=0; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test3 #1 //simulate x=0; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test4 #1 //simulate x=1; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test5 #1 //simulate x=1; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test6 #1 //simulate x=1; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test7 #1 //simulate x=1; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test8 #1 //simulate $finish; end endmodule

**2.29 b Output**



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**2.29 d. Module**

module Project1\_AssignStatement ( input x,y,z, output f );

assign endmodule

**2.29 d. Test Bench**

`include " Project1\_AssignStatement.v" module tester(); reg x,y,z; wire f;

Project1\_AssignStatement po(x,y,z,f); initial begin $display ("Time x y z f"); $monitor ("%4d %b", $time,f); x=0; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test1 #1 //simulate x=0; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test2 #1 //simulate x=0; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test3 #1 //simulate x=0; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test4 #1 //simulate x=1; y = 0; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test5 #1 //simulate x=1; y = 0; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test6 #1 //simulate x=1; y = 1; z = 0; $display("%4d %b %b %b", $time, x, y,z); //test7 #1 //simulate x=1; y = 1; z = 1; $display("%4d %b %b %b", $time, x, y,z); //test8 #1 //simulate $finish; end endmodule

**2.29 d. Output**

