

ANALOG PROJECT

Dr Rinkee Chopra

OBJECTIVE

TO DESIGN A BJT AMPLIFIER FOR A VOLTAGE GAIN OF APPROXIMATELY 150 AT 100 KHZ AND ANALYZE ITS INPUT/OUTPUT IMPEDANCE, BANDWIDTH, AND MAXIMUM SIGNAL SWING.

TO MODIFY THE DESIGN FOR A GAIN OF 250 AND COMPARE BOTH CASES.

OVERVIEW

1. A common-emitter BJT amplifier provides high voltage gain and is widely used in analog signal amplification.
2. In this configuration, the input signal is applied between the base and emitter, and the output is taken between the collector and emitter.
3. The small-signal voltage gain of a CE amplifier (with emitter bypass capacitor) is approximately given by:

$$A_v = -R_C/R_E$$

R_C is the effective load resistance at the collector
R_E thermal voltage divided by emitter current.

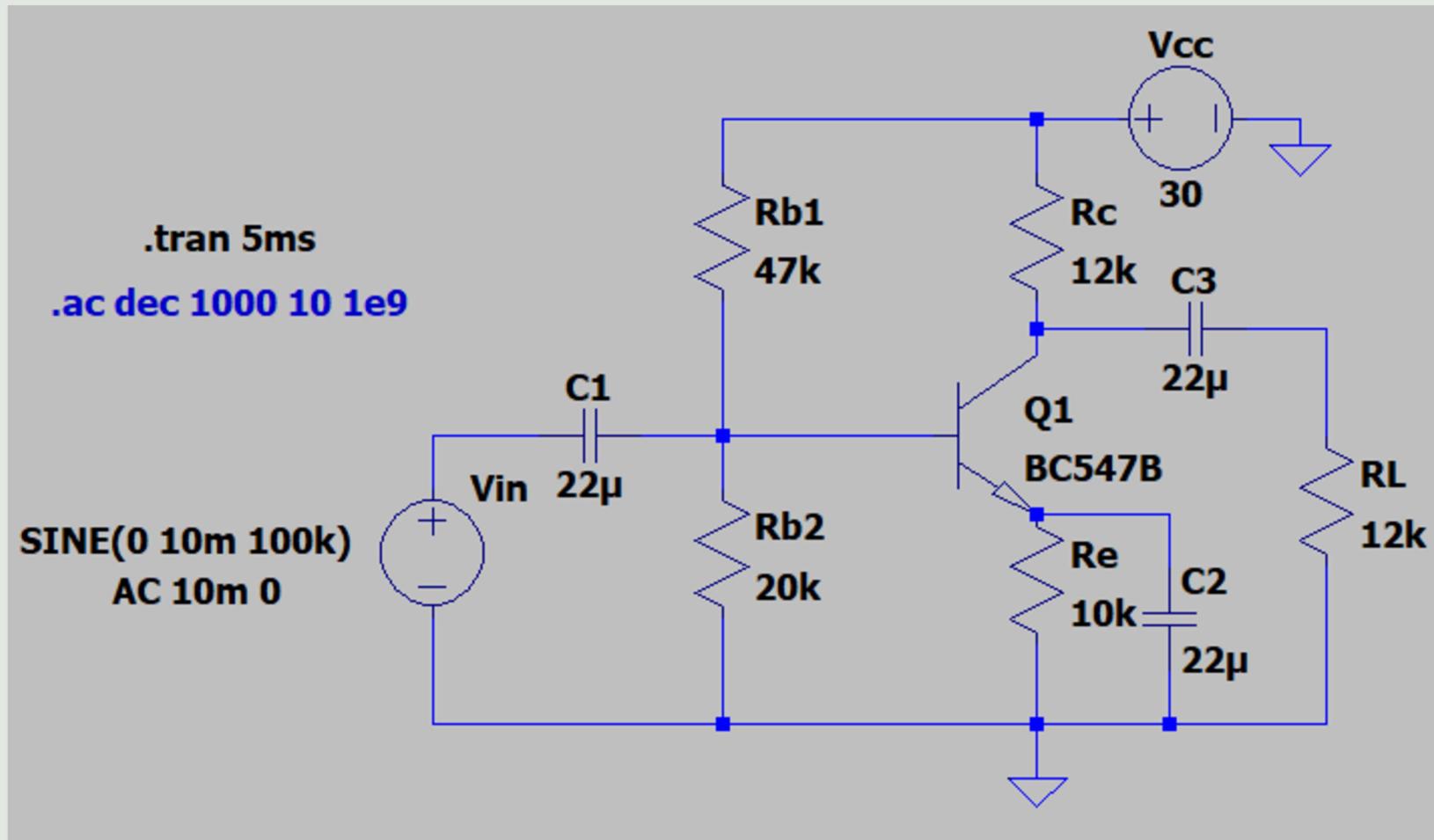
4. Input impedance is determined by the parallel combination of the biasing resistors and the input impedance looking into the transistor's base.
5. The output impedance is approximately equal to the collector resistance.
The maximum undistorted output signal swing is limited by the transistor's saturation and cutoff voltages.

KEY COMPONENTS :

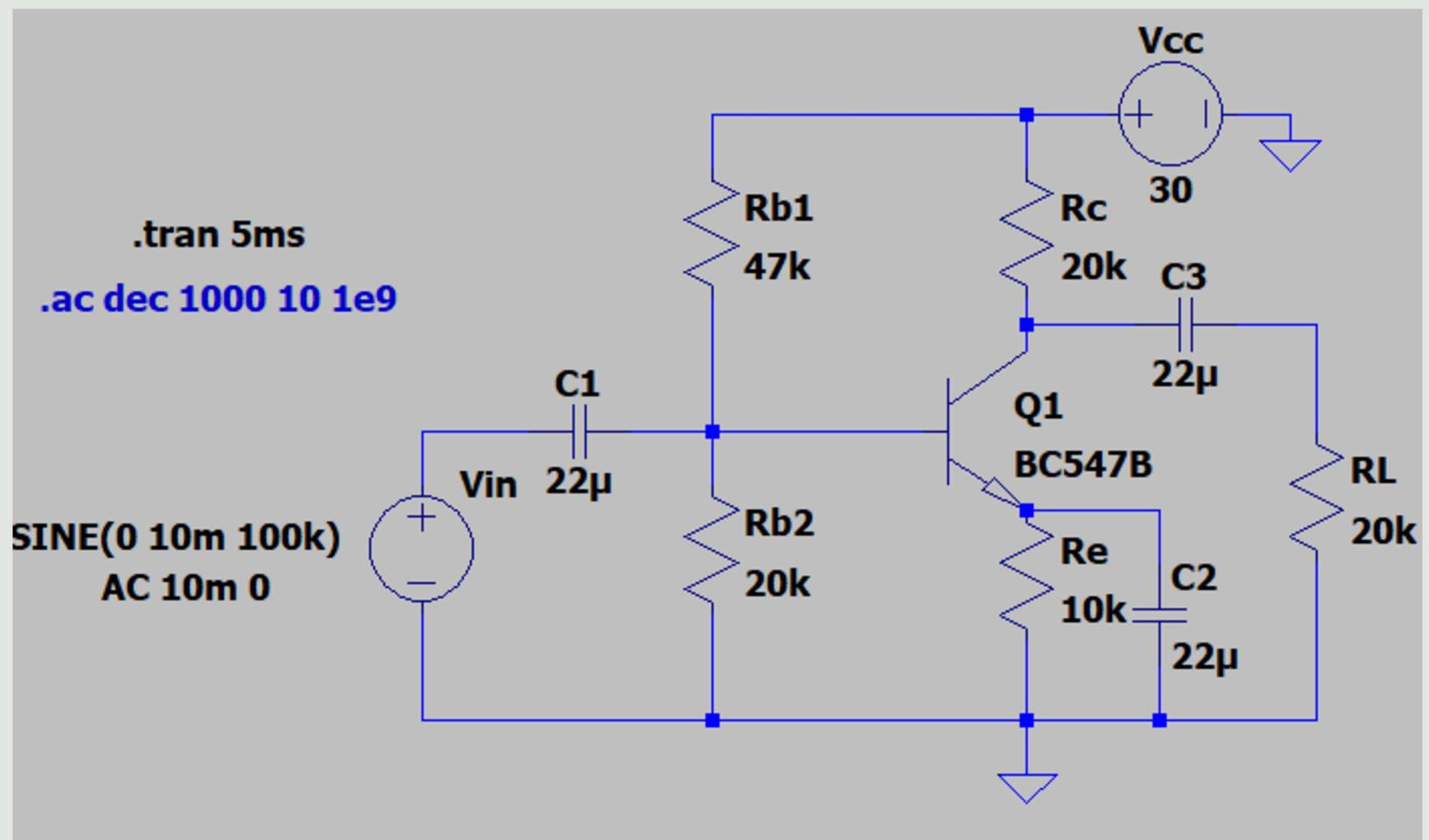
- Transistor: BC547B (NPN)
- Biasing resistors: $20\text{k}\Omega$, $47\text{k}\Omega$
- Collector resistor: $12\text{k}\Omega$
- Emitter resistor: $10\text{k}\Omega$ (bypassed)
- Load resistor: $12\text{k}\Omega$
- Supply Voltage: 30V
- Coupling/Bypass capacitors: $22\mu\text{F}$ each



CIRCUIT DIAGRAMS

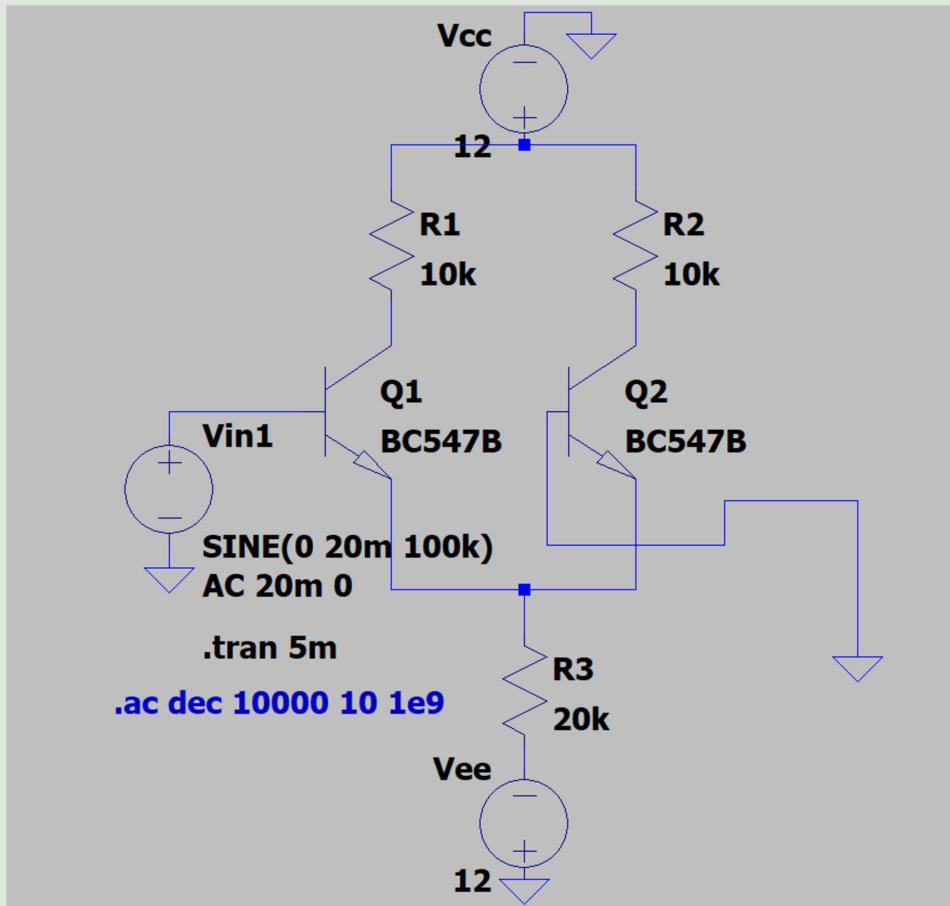


GAIN=150



GAIN=250

USING DIFFERENTIAL AMPLIFIER



DESIGN CALCULATIONS:

→ Bias Resistors in Parallel:

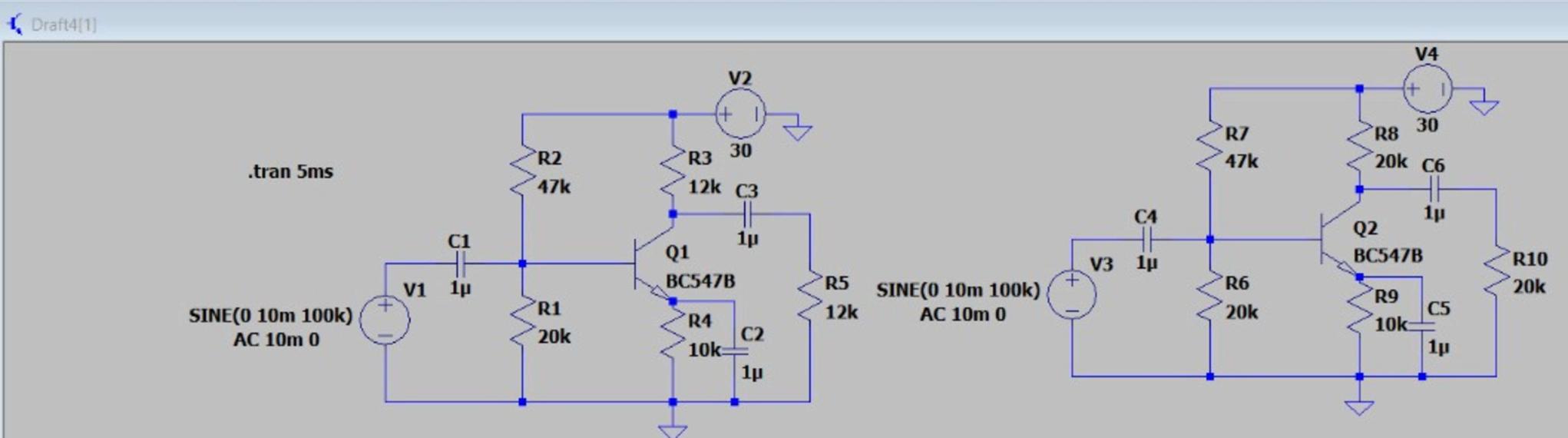
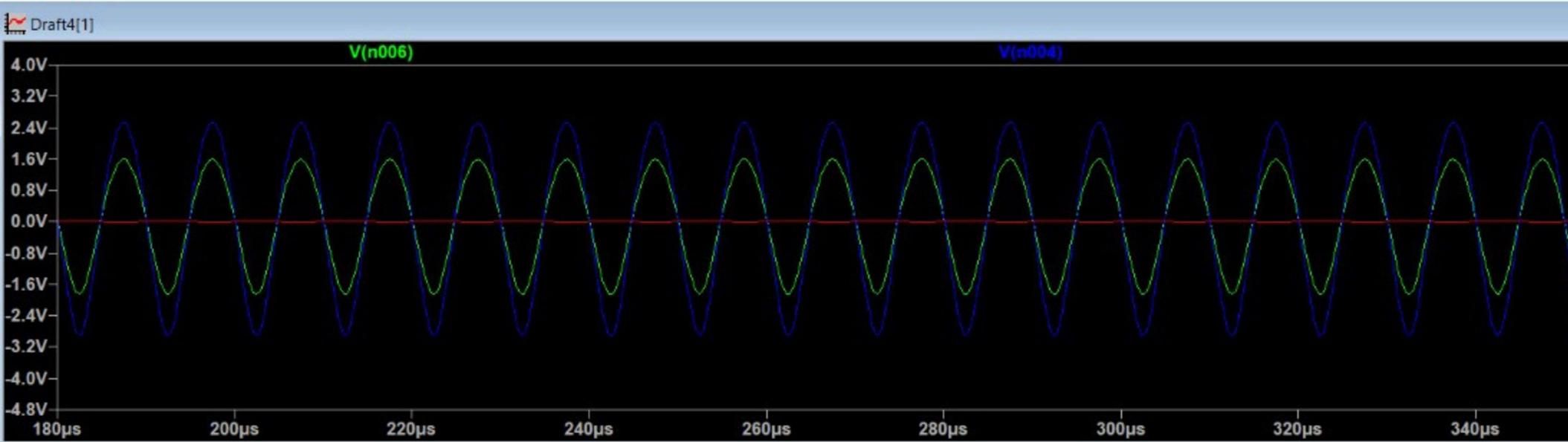
$$R_6 \parallel R_7 = \frac{20k \times 47k}{20k + 47k} = 14.04k\Omega$$

→ Total Input Impedance:

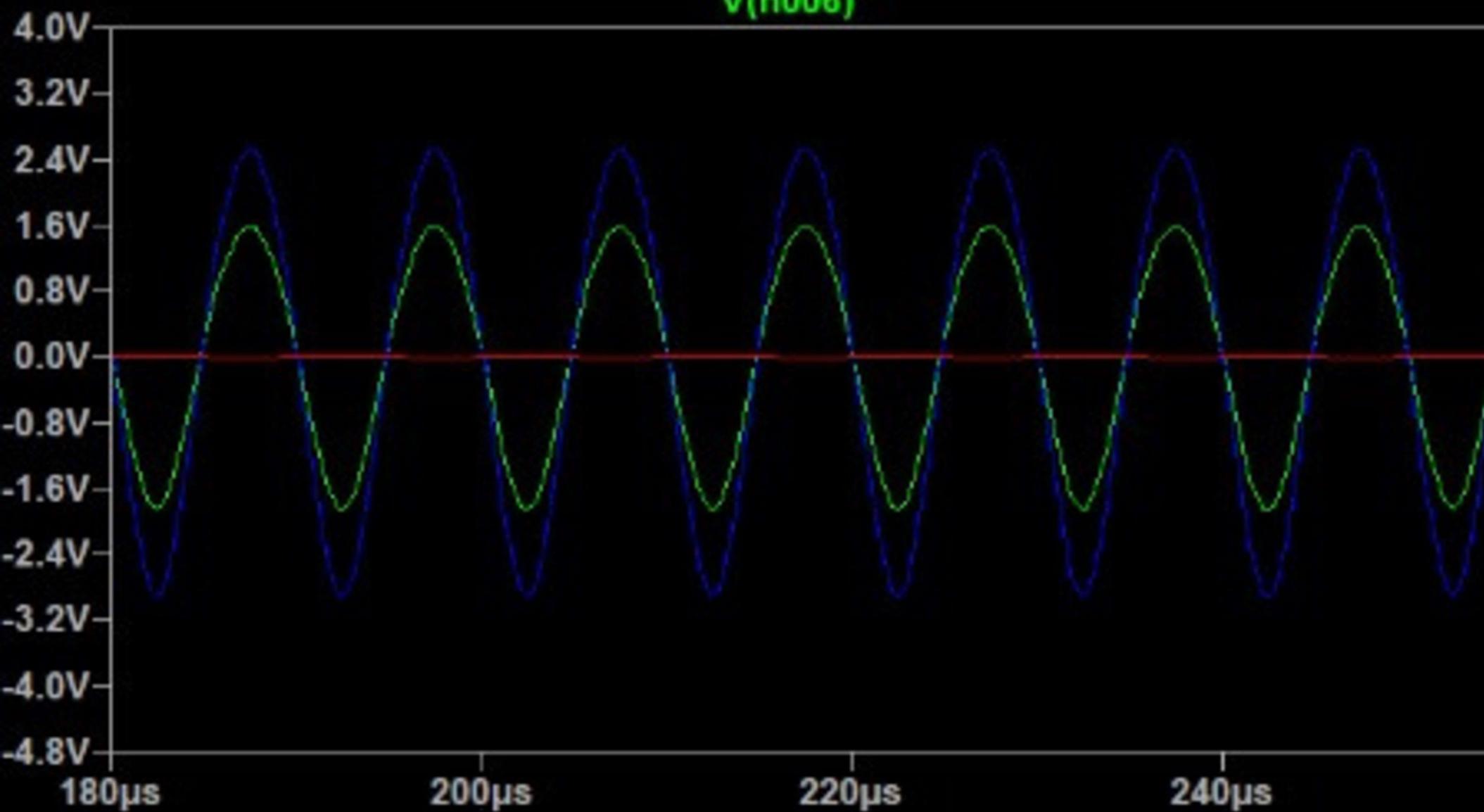
$$Z_{in} = (R_6 \parallel R_7) \parallel r_\pi = \frac{14.04k \times 6.67k}{14.04k + 6.67k} \approx 4.53k\Omega$$

→ Output Impedance:

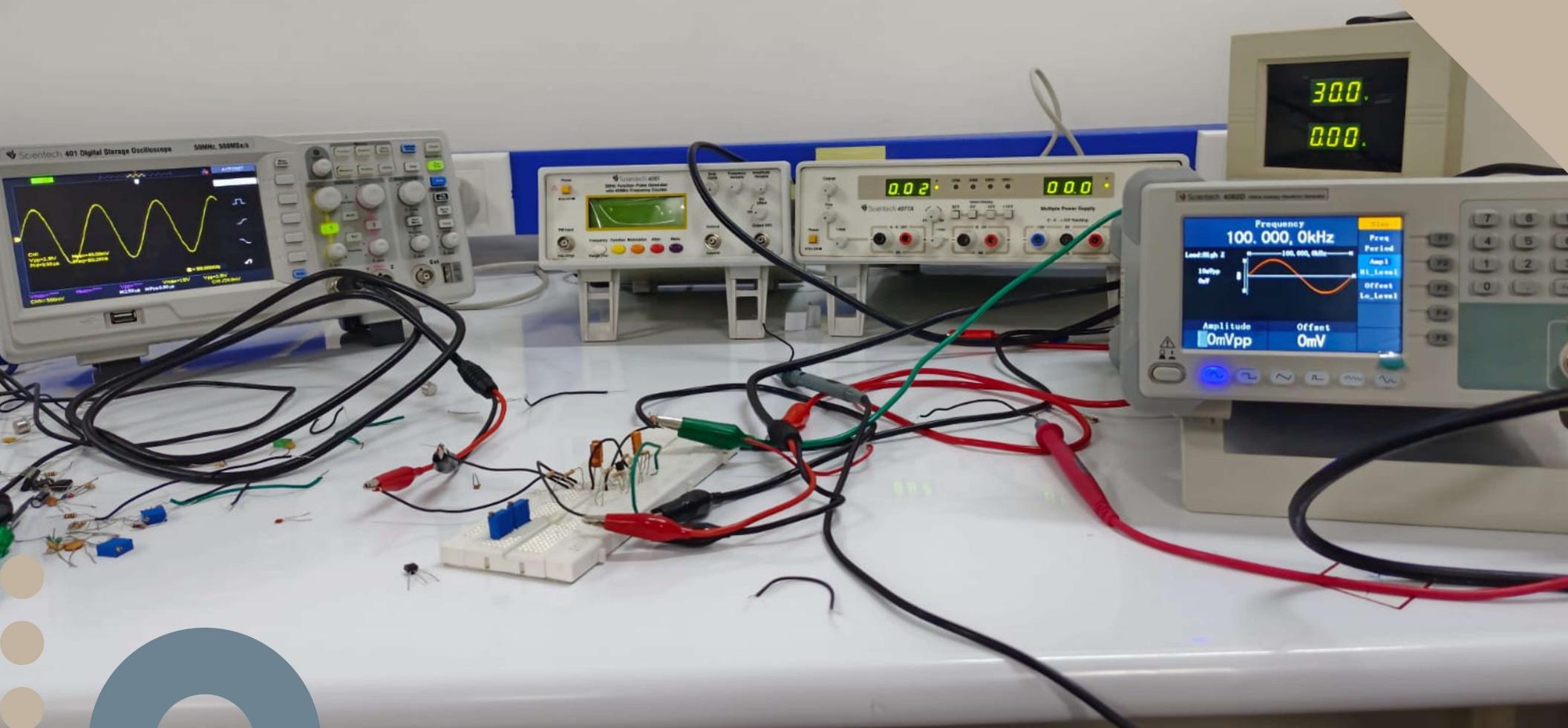
$$Z_{out} = R_8 \parallel R_{10} = \frac{20k \times 20k}{20k + 20k} = 10k\Omega$$



V(n006)

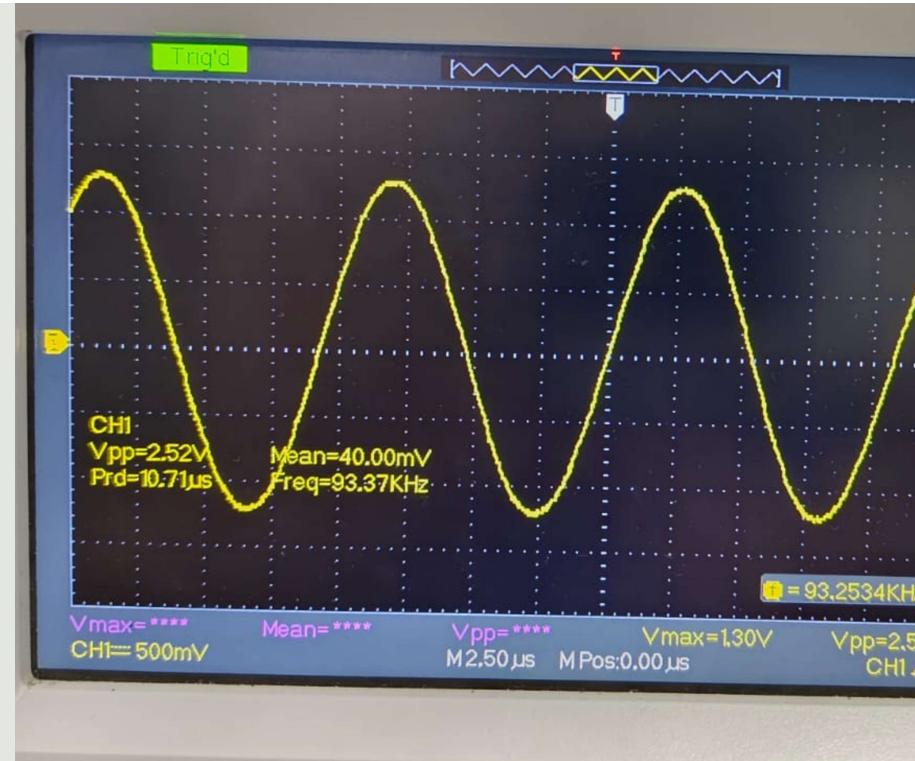
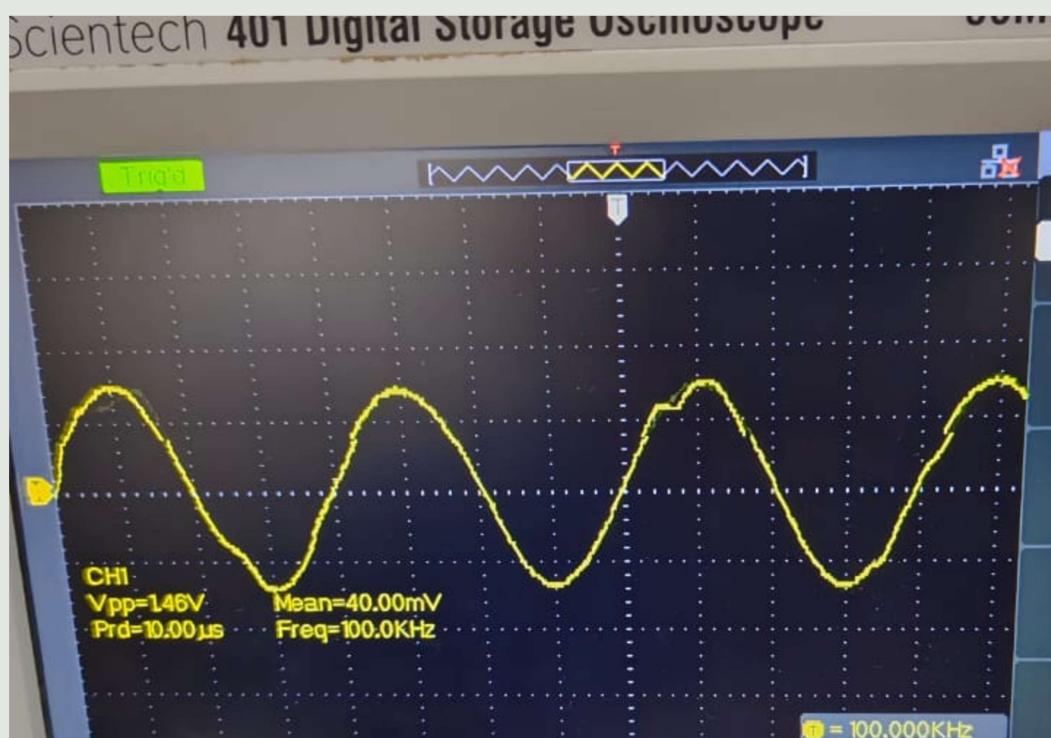


SNAPSHOT OF HARDWARE IMPLEMENTATION



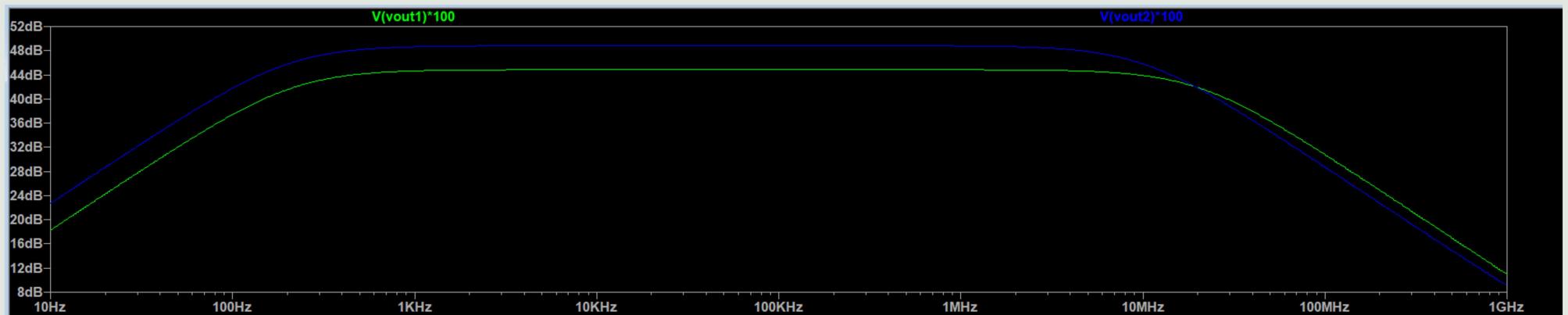
OUTPUTS OF HARDWARE IMPLEMENTATION

150 GAIN



250 GAIN

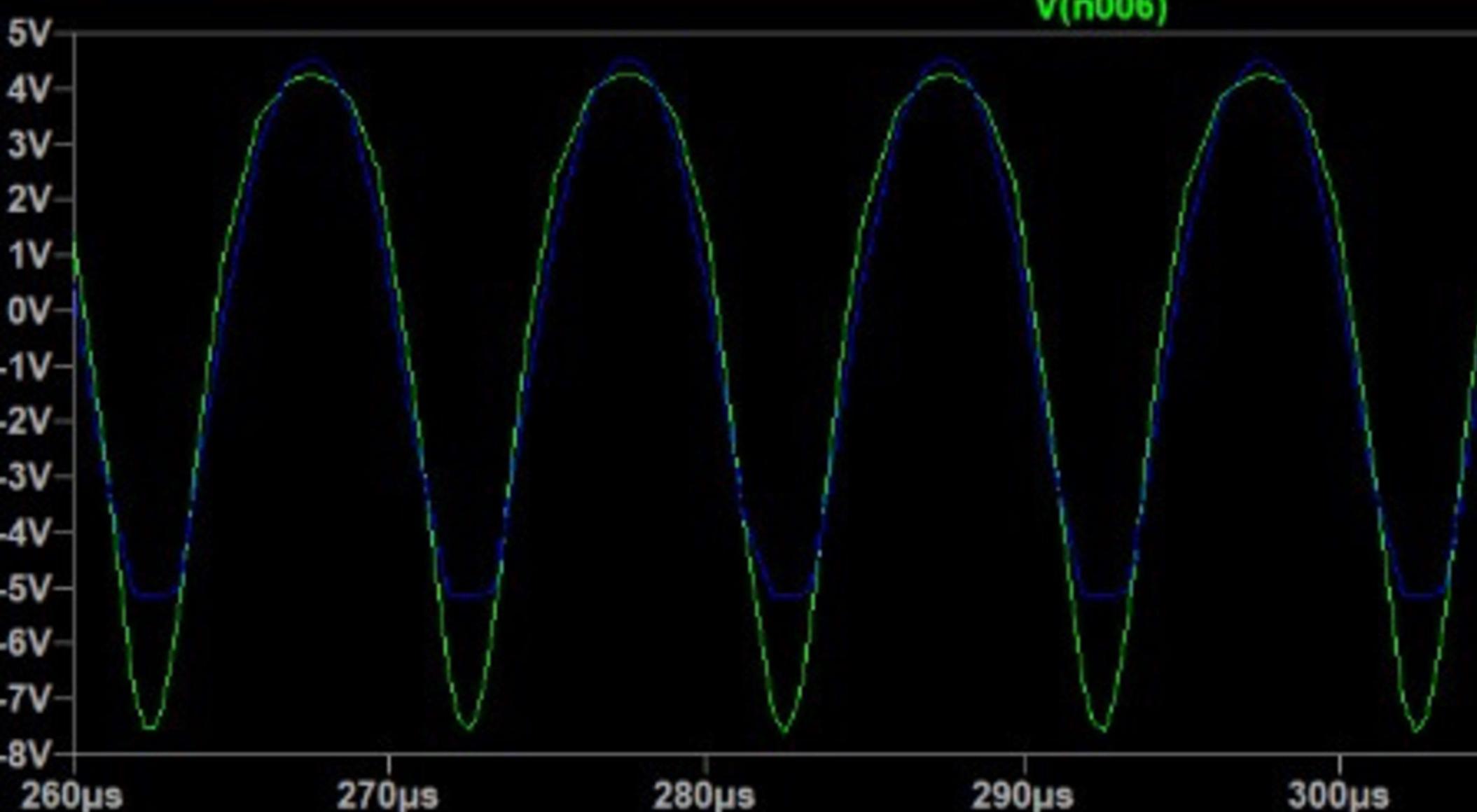
FREQUENCY RESPONSE



FOR 150 GAIN: $F1=215\text{Hz}$; $F2=18.9\text{MHz}$

FOR 250 GAIN: $F1=204\text{Hz}$; $F2=17.12\text{MHz}$

V(n006)



WHAT IS THE MAXIMUM ALLOWED INPUT AND OUTPUT SIGNAL SWING TO OBTAIN DISTORTION FREE SIGNAL?

FOR 150 GAIN, WE GOT 4V MAX OUTPUT.SO THE
MAXIMUM ALLOWED INPUT IS $4/150=26.7\text{mV}$

FOR 250 GAIN, WE GOT 5V MAX OUTPUT.SO THE
MAXIMUM ALLOWED INPUT IS $5/250=20\text{mV}$

REASON:

THE LOW MAXIMUM OUTPUT VOLTAGE ($\approx 4V$ PEAK) FOR 150 GAIN IS PRIMARILY DUE TO A HIGH Emitter RESISTOR ($10K\Omega$), THE BIASING NETWORK SETS THE TRANSISTOR'S Q-POINT AWAY FROM THE MIDPOINT OF THE SUPPLY VOLTAGE, LIMITING THE AVAILABLE SWING BEFORE THE TRANSISTOR EITHER SATURATES OR CUTS OFF. THUS IT CAN BE DEFINED AS THE Q POINT STRAYS AWAY FROM MIDDLE POINT, IT ENTERS A NON LINEAR REGION.

CONCLUSION

- Successfully designed and simulated a BJT common-emitter amplifier achieving a gain of ~150 at 100kHz.
- After modification, achieved a gain of ~250 with minor adjustments.
- Higher gain resulted in reduced input swing tolerance and slight narrowing of bandwidth, consistent with the gain-bandwidth tradeoff.
- Amplifier shows good performance in the 100 kHz range with satisfactory input and output impedance values.

Thank You