JAY SARKAR

Western Digital Corporation
5601 Great Oaks Parkway, San Jose, CA – 95119

jsarkar@utexas.edu, 650-207-0369

Citizenship United States

Education

The University of Texas at Austin **Austin, Texas**
Ph.D. in Electrical & Computer Engineering (Solid-State Electronics) **December 2007**
Dissertation Title: *"Non-volatile Memory Devices beyond Process-scaled Planar Flash Technology"*
Awarded *"The Ben Streetman Prize for Outstanding Research in Electronic and Photonic Materials and Devices"*, 2007.
Dissertation Advisors: Prof. Sanjay K. Banerjee and Dr. Robert J. Gleixner of Intel.

Rice University **Houston, Texas**
M.S. in Applied Physics **May 2004**
Thesis Title: *"Engineering the electromagnetic environment in a nanostructure to study single-electron tunneling"*, advised by Prof. Alex J. Rimberg.
Awarded *Dean's Fellowship*, 2001.

Indian Institute of Technology **Kharagpur, India**
B.Sc. (Honors) in Physics **June 2001**

Experience

Western Digital Corporation (HGST) **San Jose, California**
Technologist, Solid-State Storage Analytics and Robustness R&D *Nov. 2014 – present*
Principal Engineer, SSD Reliability Science and Engineering *May 2013 – Oct. 2014*
Lead ownership for establishing and directing research and development on knowledge based system-level data analytics methodologies, methodologies for robustness and statistical validation frameworks for enterprise/data-center solid-state storage technologies and devices (SSD). Developed the first known/published physics-aligned, interpretable Machine Learning based predictive analytic methodologies for high-reliability/performance solid-state storage. Research on explainable supervised and unsupervised classification methodologies include characterization, integration, interpretation and modeling of the fundamental predictors for enabling designs of individually self-aware and adaptive systems under dynamic operational data throughput and workload stresses, concomitant with physics of system design. Interfacing across multiple organizational teams and a corporate joint-venture, develop intellectual property and author peer-reviewed publications disseminating developed generalizable methodologies across internal stake-holders and external research community. Along with guiding robust development and validation methodologies, help influence and define technical strategies for analytics methods on SSD and emerging persistent memory technologies, while mentoring junior colleagues towards realization of organizational goals.

Numonyx B.V. (Intel spin-off, now Micron**) and Intel Corporation** **San Jose, California**
Senior Research & Development Engineer *Oct. 2007 – Jun. 2010*
Researched and developed Phase Change Memory (PCM/3D Xpoint) science and technology at 90 and 45 nm lithographic geometries, towards enabling the novel non-volatile memory technology and potential novel schemes of information processing that leverage analog-resistive and low-latency storage/memory architectures. Direct responsibilities included developing the core physical models of intrinsic operational evolution and large-array robustness of PCM technology, focused on fundamental device/array physics and materials science. Enabled and improved on technology capabilities by incorporating such understanding towards optimizing the reliability/performance envelope of the technology – with application of developed physical and statistical models towards array-programming microcode algorithm design and silicon process developments. Played a key role in enabling the technology and first product to exceed 1 Million set/reset cycles endurance, while meeting or exceeding orthogonal requirements of performance and retention. Authored peer-reviewed publications and intellectual property in a cross-functional and collaborative role with design and process research teams, helping enable the first successful implementation of PCM technology in the industry, with subsequent volume manufacturing at Micron and Intel.

Graduate Intern, Technical *Mar. – Sep. 2007; May – Aug. 2006 & 2005*

Designed, implemented, interpreted experiments and testing methodology towards understanding Phase Change Memory device physics, materials science and reliability; and an initial demonstration of multi-state engineering for multi-level cell operation.

Qualcomm Incorporated, Qualcomm MEMS Technologies **San Jose, California**

Senior Engineer, MEMS Research and Innovation Center *Jul. 2010 – Nov. 2012*

Owned multiple, diverse areas of research and development on lifetime performance of novel MEMS-based reflective display technology for low-power usage with color and video capabilities. Technical areas included developing understanding on impact of material and component properties, environmental stressors, encapsulation and system design on technology figures of merit and lifetime. Established ab-initio characterization methodologies and models that estimated the intrinsic capabilities of the technology lifetime, for factors including aging, tribology and packaging design. Based on developed understanding, demonstrated multiple strategies of process and design improvements by 2x – 10x for various capability limits of the glass-based technology. Developed intellectual property and helped enable subsequent core technology research & development.

The University of Texas at Austin, Microelectronics Research Center **Austin, Texas**

Graduate Research Assistant and Ph.D. candidate *Aug. 2004 – Sep. 2007*

Dissertation research demonstrated design, fabrication and characterization of a novel vertical, gate-all-around (3-D, GAA) inherently nanowire-scalable Flash memory transistor with protein-mediated ordering of nanocrystal quantum dot floating-gate for ultra-high density integration, excellent electrostatic control and reliable retention. Original research additionally developed fundamental physical and electrical models of device physics, materials science and associated reliability of Phase Change Memory science and technology.

Rice University **Houston, Texas**

Graduate Research Assistant and M.S. candidate *Aug. 2001 – Aug. 2004*

Thesis research on few-electron transport physics, based on a nanostructure designed, fabricated and characterized on a GaAs-AlGaAs heterostructure substrate with a 2-D electron system. Taught undergraduate laboratory classes and mentored undergraduate researchers.

J Nehru Center for Advanced Scientific Research **Bangalore, India**

Summer Research Fellow & Rajiv Gandhi Talent Scholarship awardee *May – Aug., 1999 & 2000*

Designed, implemented and optimized one of the first diskless, distributed memory Beowulf Clusters (a high-performance parallel computing platform based on commodity components and open-source software) in India to enable research based on molecular dynamics simulations.

Awards & Honors

Various corporate-internal awards at Western Digital, Qualcomm and Numonyx/Intel (including best paper award and first prize in hackathon), 2007-2018

IEEE Senior Member Elevation, 2018

Ben Streetman Prize for Outstanding Research in Electronic and Photonic Materials and Devices 2007*:* The University of Texas at Austin - university-wide interdisciplinary award

Graduate Research Assistantship 2004-2007*:* Microelectronics Research Center, UT Austin (SRC/MARCO-FCRP); *2002-2004:* Rice University (NSF)

Dean's Fellowship 2001-2002: Rice Quantum Institute, Rice University

Debesh Kamal Scholarship and B.D. Bangur Endowment Scholarship 2001: R.K. Mission Institute of Culture and B.D. Bangur Endowment, India

Rajiv Gandhi Science Talent Research Scholarship, 2000 and *Summer Research Fellowship*, 1999 & 2000: Awarded based on a nationally competitive selection and judging by JNCASR, India

Professional Activities & Affiliations

Vice-Chair, System Reliability Committee, International Reliability Physics Symposium 2019

Technical Program Committee Member on System Reliability (Focus Session), IEEE International Reliability Physics Symposium (IRPS) 2018

Co-Moderator, Solid-State Storage and Memory Workshop on "Resiliency in design, system-level considerations and role of usage analytics", IRPS 2018

Invited Speaker, IEEE Silicon Valley Chapter technical seminars on SSD & ML methods 2018

Senior Member, IEEE (Computer Society & Electron Devices Society) 2005 - present

Certification in Fundamentals of Technical Project Management, PM Training Pros 2012

Grand Awards Judge, Intel Science and Education Fair, Society for Science and the Public 2010

Ad-hoc reviewer: *IEEE Electron Device Letters, IEEE Transactions on Electron Devices, Journal of Electrochemical Society* and *Journal of Materials Science* 2007 - 2013

Technical Reviewer of book proposals on Linux-based clustering technologies and open-source software, Addison Wesley Professional Publishing, CA 2000 - 2001

Patents *(each bearing data-driven proofs of concept)*

Invention disclosure "Method and System for Autonomously Adaptive Solid-State Storage Health and Performance", **J. Sarkar**, C. Peterson, in filing, Oct. 2018

U.S. patent 15/979,348 "Method and System for a Storage (SSD) drive-level failure and health prediction leveraging machine learning on internal parametric data", **J. Sarkar**, C. Peterson, A. Sanayei, Y. Zhang, V. Mohan, filed/pending Oct. 2017

U.S. patent 13/535,772 "MEMS Device Encapsulation with Corner or Edge Seals", W. Lee, **J. Sarkar**, J. Liu, R. Wieler, filed Jan. 2014

U.S. patent 8,036,016 "Maintenance Process to Enhance Memory Endurance", **J. Sarkar** and Robert Gleixner, issued Oct. 2011

Refereed Publications *(peer-reviewed international conferences and journals*)

"Machine-Learned Assessment and Prediction of Robust Solid-State Storage System Reliability Physics", **Jay Sarkar**, Cory Peterson and Amir Sanayei, *2018 International Reliability Physics Symposium (IRPS)* March **2018**, *pp. 3C.6-1 – 3C.6-8.*

"Robust Error-Management and Impact of Throughput in Solid State Storage – Characterization and First System Reliability Model", **Jay Sarkar**, Cory Peterson, Yao Zhang and Steve Lock, *2017 Annual Reliability and Maintainability Symposium (RAMS)* **2017,** *pp.* 1-6.

"Reliability Characterization and Modeling of Solid State Storage", **Jay Sarkar** and Frank Sun, *2015 Annual Reliability and Maintainability Symposium (RAMS),* **2015**, *pp. 1-6.*

"Protein-Assembled Nanocrystal-Based Vertical Flash Memory Devices with Al_2O_3 Integration" , F. Ferdousi, **J. Sarkar**, S. Tang, D. Shahrjerdi, T. Akyol, E. Tutuc, S.K. Banerjee, *Journal of Electronic Materials*, **38**, p. 438, 2009

"Vertical Flash memory devices with protein-assembled nanocrystal floating gate and Al_2O_3 control oxide", F. Ferdousi, **J. Sarkar**, D. Shahrjerdi, T. Akyol, J. P. Donnelly, E. Tutuc, S. K. Banerjee, *66th IEEE Device Research Conference* **2008**

"Evolution of Phase Change Memory characteristics with operating cycles: electrical characterization and physical modeling" **J. Sarkar** and Bob Gleixner, *Applied Physics Letters* **91**, p. 233506, 2007

"Bio-nano approaches to fabricating quantum-dot floating gate flash memories", S. Banerjee, Shan Tang, **J. Sarkar**, Davood Shahrjerdi, Chang Lee, *International Conference on Solid State Devices and Materials* **2007**, Ibaraki, Japan (**invited**)

"Protein-mediated assembly of nanocrystal floating gate in a vertical flash cell", **J. Sarkar**, Shan Tang, Domingo Garcia, Sanjay Banerjee, *22nd IEEE Non Volatile Semiconductor Memory Workshop* **2007**, p. 34 – 35

"Flash memory with nanoparticle floating gate", Sanjay Banerjee, Shan Tang, **J. Sarkar**, Davood Shahrjerdi, Chang Lee, *Particles 2007*, Toronto, Canada (**invited**)

"Data retention characterization of Phase-Change Memory arrays", B. Gleixner, A. Pirovano, **J. Sarkar**, F. Ottogalli, E. Tortorelli, M. Tosi and R. Bez, *Proceedings of 45th Annual IEEE International Reliability Physics Symposium* **2007**, p. 542 - 546 (**invited**)

"Vertical flash memory with nanocrystal floating gate for ultra-dense integration and good retention", **J. Sarkar**, Sagnik Dey, Davood Shahrjerdi and Sanjay Banerjee, *Electron Device Letters*, **28**, p. 449 – 451, 2007

"Vertical flash memory with protein-mediated assembly of nanocrystal floating gate", **J. Sarkar**, Shan Tang, Davood Shahrjerdi and Sanjay Banerjee, *Applied Physics Letters*, **90**, p. 103512, 2007 – **editorially selected** for the *Virtual Journal of Nanoscale Science and Technology*, **15**, issue 11 (March 19th, 2007) and the *Virtual Journal of Biological Physics Research*, **13**, issue 6 (March 15th, 2007)

"Vertical (3-D) flash memory with SiGe nanocrystal floating gate", **J. Sarkar**, S. Dey, Y. Liu, D. Shahrjerdi, D. Q. Kelly and S. K. Banerjee, *64th IEEE Device Research Conference Digest* **2006**, p. 267 – 268

"Fabrication of Self-Assembled Ni Nanocrystal Flash Memories Using a Polymeric Template", D. Shahrjerdi, **J. Sarkar**, X. Gao, D. Q. Kelly, S. K. Banerjee, *64th IEEE Device Research Conference Digest*, p. 269 – 270, 2006

"Fabrication of Dense Ordered Arrays of Metal Dots for Flash Memory Application", D. Shahrjerdi, **J. Sarkar**, S. K. Banerjee, *Materials Research Society Spring Meeting*, 2006

"Improved performance of SiGe nanocrystal memory with VARIOT tunnel barrier", Y. Liu, S. Tang, S. Dey, D. Kelly, **J. Sarkar**, S. K. Banerjee, *IEEE Transactions on Electron Devices*, **53**, p. 2598 – 2602, 2006

"Engineering the electromagnetic environment in a semiconductor nanostructure to study single electron tunneling oscillations", **J. Sarkar**, Zhonqing Zhi, Alex Rimberg, *APS Annual March Meeting*, Montreal, **2004**

References Available on request