

**Department of Electrical Engineering  
Indian Institute of Technology Bombay**

## **EE344: Electronic Design Lab**



## **20 MHz Trans-Impedance Amplifier**

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# 1 Project Objectives

1. To design a TIA for POF receiver having both low noise and high bandwidth, upto about 20MHz.
2. Designing circuit using minimum number of elements, we use high frequency BJT along with JFET.
3. Testing of your circuit using a Si PIN photodiode, optical signal transmitted using a LED Transmitter through a POF.

## Design Approach

### 2 TIA using TL081

This version uses a TL081 Op-amp to design the TIA. The circuit we tested is shown below

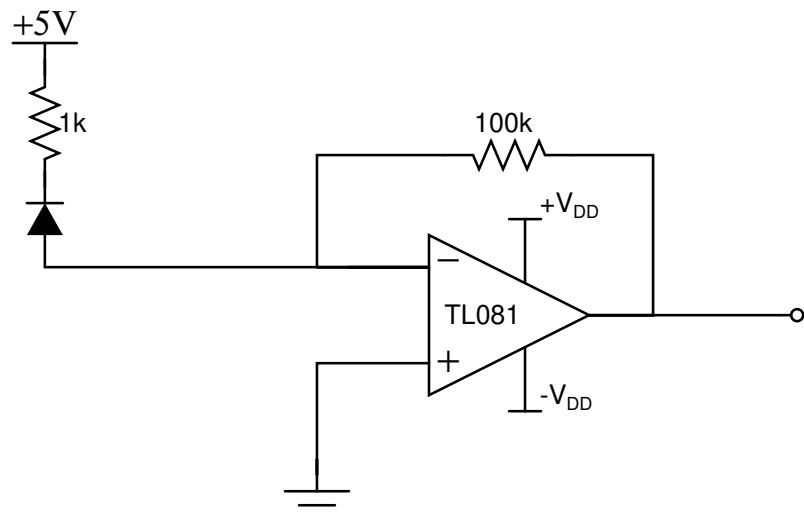


Figure 1: TIA using TL081

The experimental results are as follows:

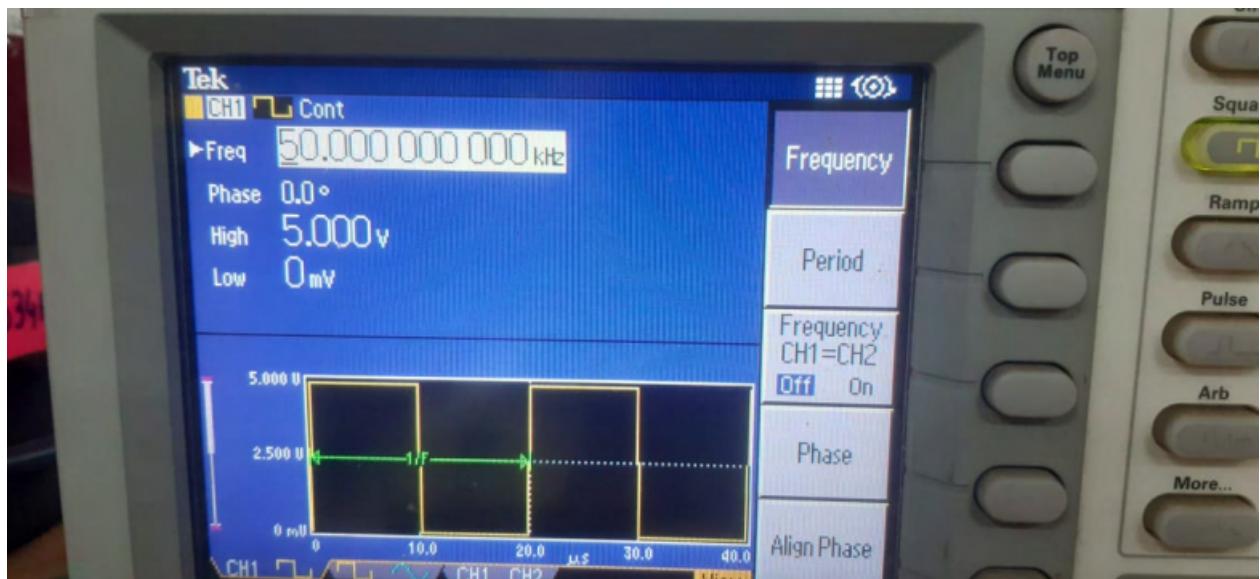


Figure 2: 50 KHz signal as input to LED

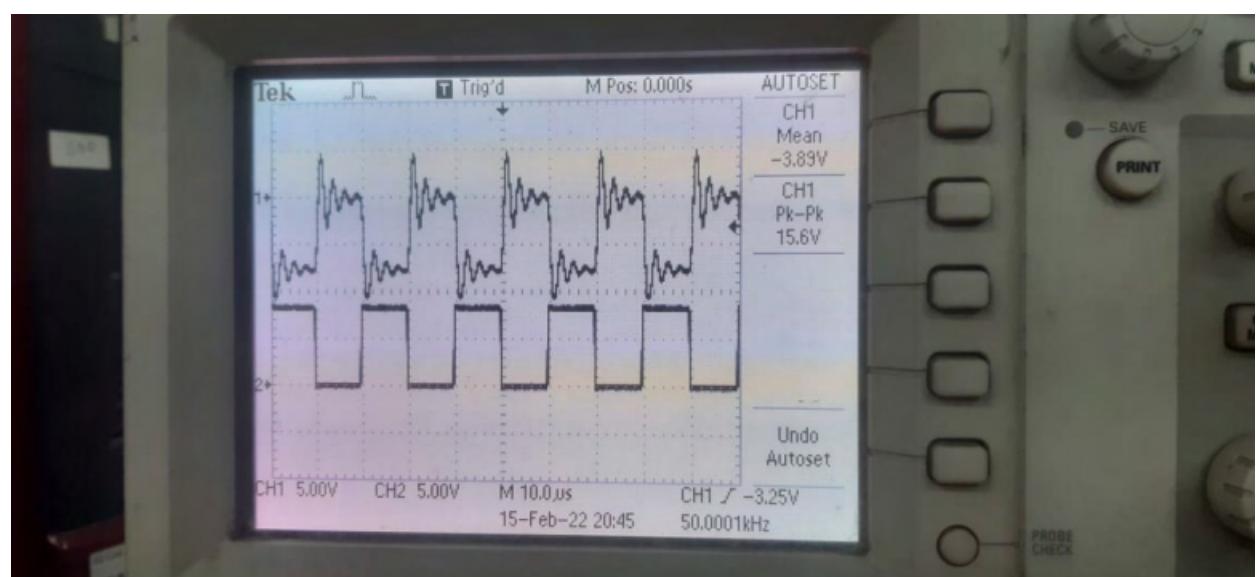


Figure 3: Output waveform

### 3 TIA Version1

This design consists of a CS stage using JFET followed by two CE stages

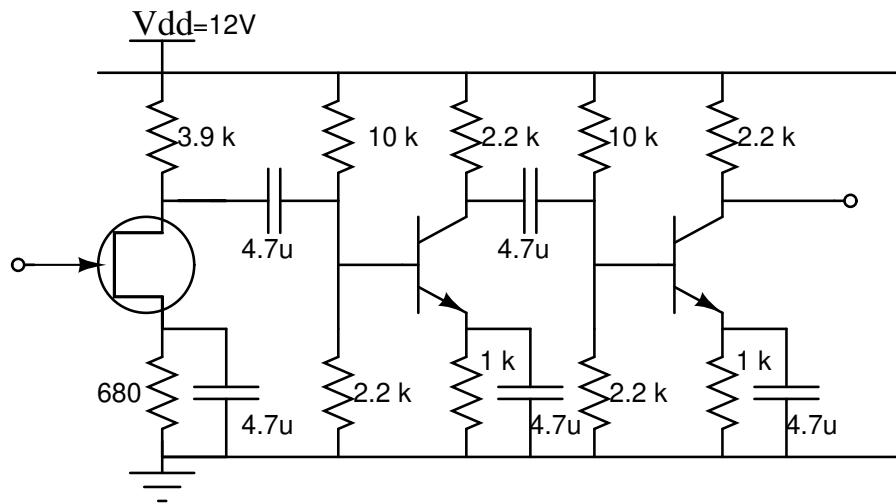


Figure 4: 3 stage TIA

We designed and tested each of the stage individually and cascaded them sequentially

### 3.1 JFET CS stage

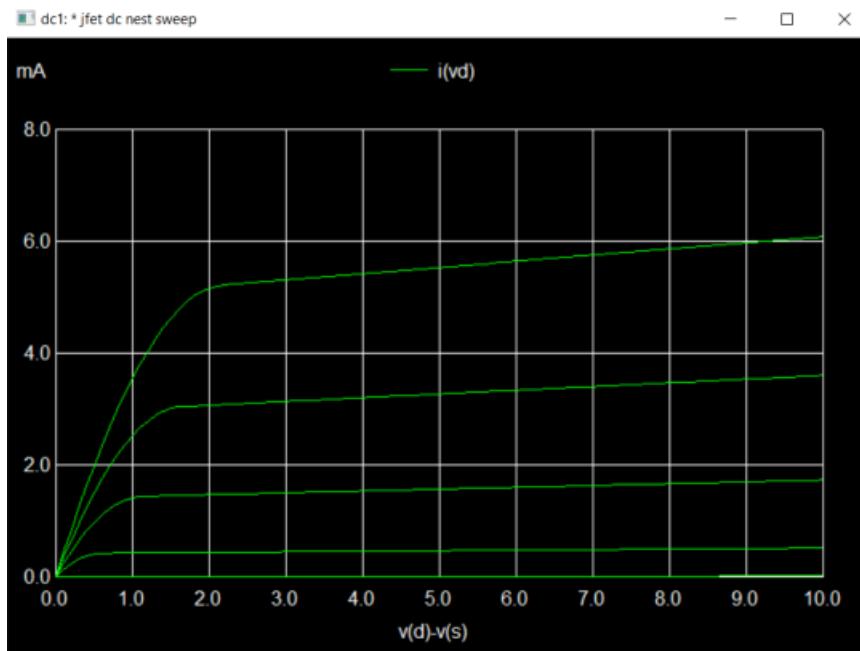


Figure 5: JFET I-V characteristics

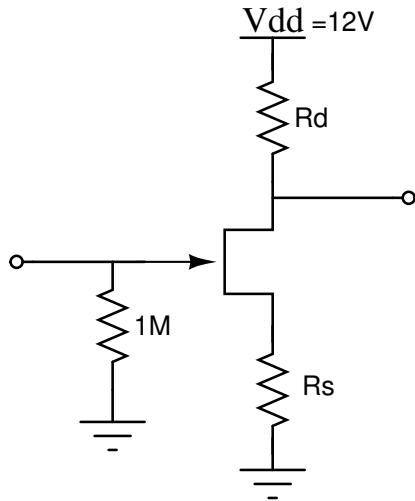


Figure 6: JFET CS stage

From I-V characteristics we take operating point as  $V_{GS} = -1V$  and  $V_{DS} = 5V$ , we get

$$I_d = 1.565mA$$

Thus,

$$R_d = \frac{6V}{1.565mA} = 3.83k\Omega$$

$$R_s = \frac{1V}{1.565mA} = 638.9\Omega$$

We take  $R_s = 680\Omega$  and  $R_d = 3.9k\Omega$

We do the small signal analysis for JFET,  $g_m$  for JFET is given as

$$g_m = 2 \frac{I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

Using min-max values of  $I_{DSS}$  from the datasheet, we get

$$g_m = 2mS(min) - 5mS(max) \implies Gain = 7.8(min) - 19.5(max)$$

### 3.1.1 Experimental Results

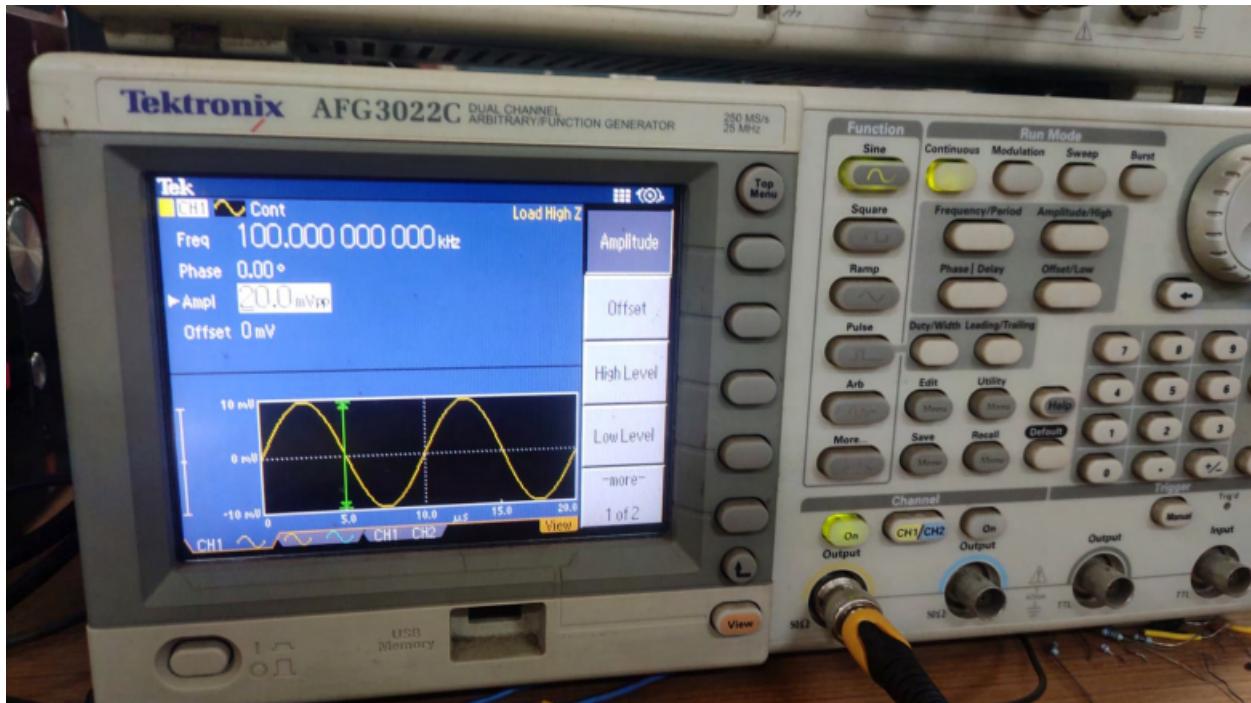


Figure 7: 100 KHz, 20mV  $V_{pp}$  sine-signal as input to CS Amplifier

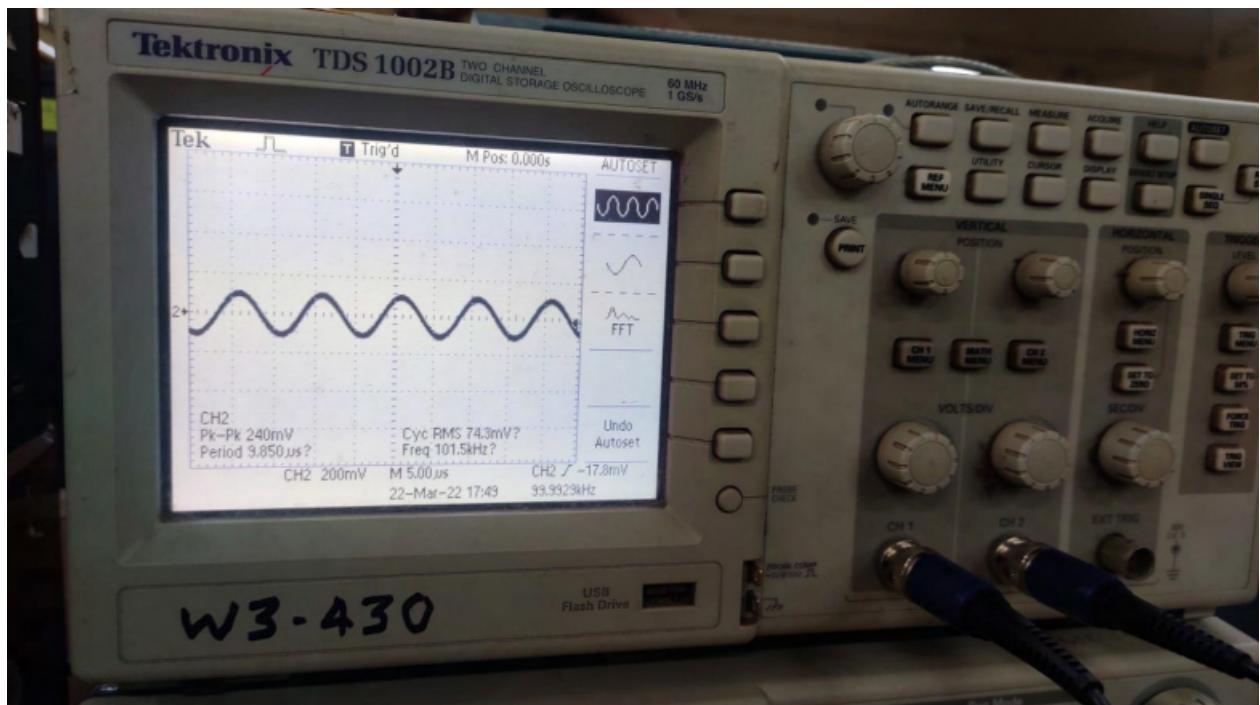


Figure 8: Output waveform

The measured DC values are,

$$V_D = 4.7V, V_G = 0V, V_S = 1.2V$$

$$V_{GS} = -1.2V, V_{DS} = 3.5V, I_D = \frac{12 - 4.7}{3.9k} = 1.8717mA$$

The experimental gain is approximately -12.

### 3.2 BJT CE stage

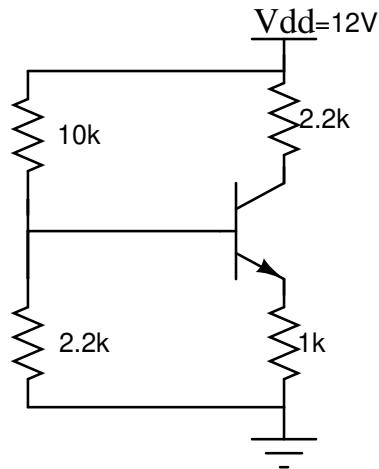


Figure 9: BJT CE stage

Analysis of the above circuit,

$$V_B = 12 \frac{2.2}{12.2} = 2.163$$

taking  $V_{BE} = 0.7$  and  $\beta = 100$

$$V_E = 1.463V \implies I_E = 1.463mA$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{1.463}{101} = 0.014mA$$

$$I_C = \beta I_B = 1.448mA \implies V_C = 12 - 3.186 = 8.81V$$

### 3.2.1 Experimental Results

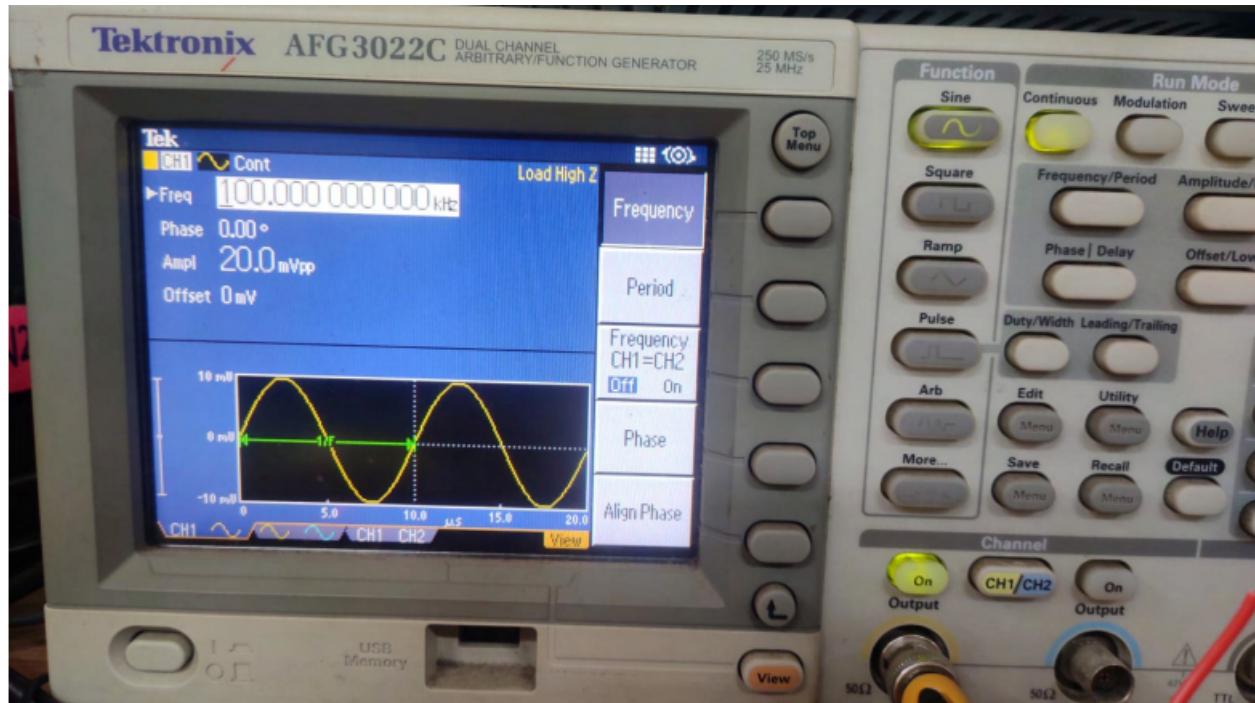


Figure 10: 100 KHz, 20mV  $V_{pp}$  sine-signal as input to CE Amplifier

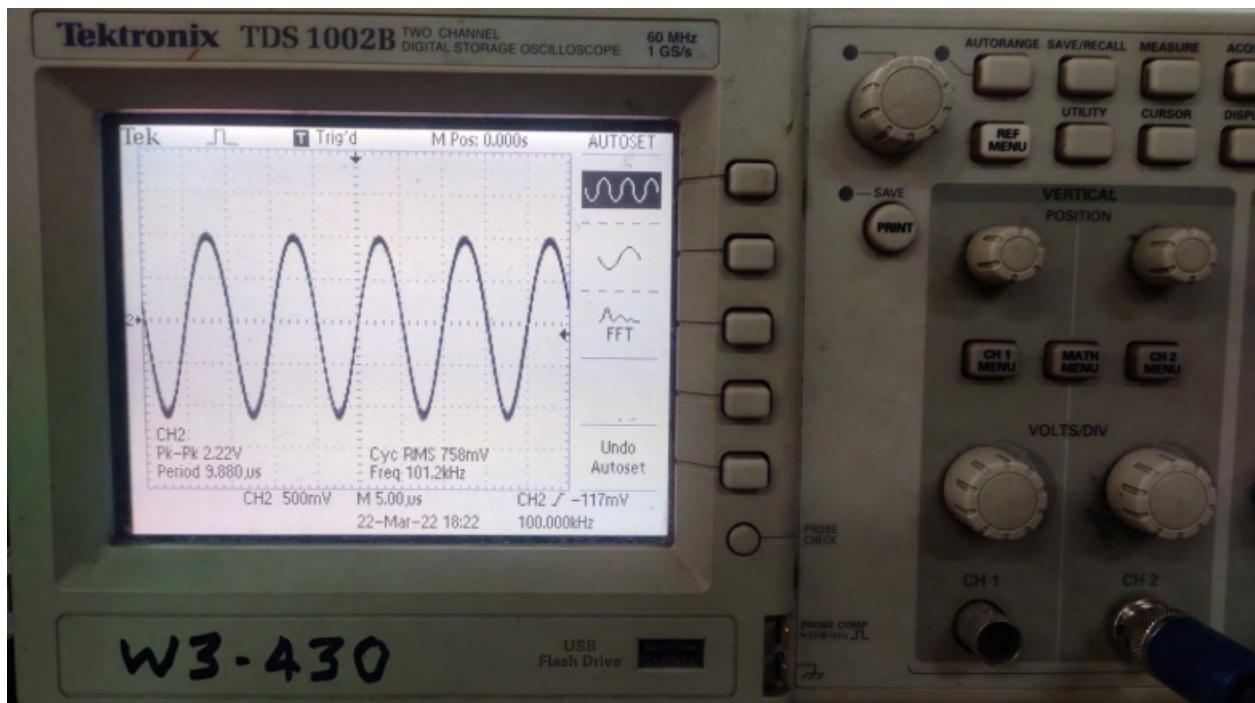


Figure 11: Output waveform

The measured DC values are,

$$V_B = 2.16V, V_E = 1.5V, V_C = 8.62V$$

$$I_E = \frac{1.5}{1k} = 1.5mA$$

The experimental gain is approximately -110.

### 3.3 CS-CE cascaded

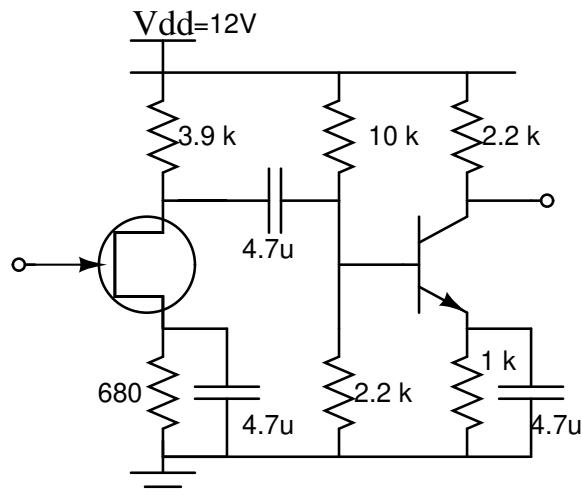


Figure 12: CS-CE cascaded

The experimental results are as follows:

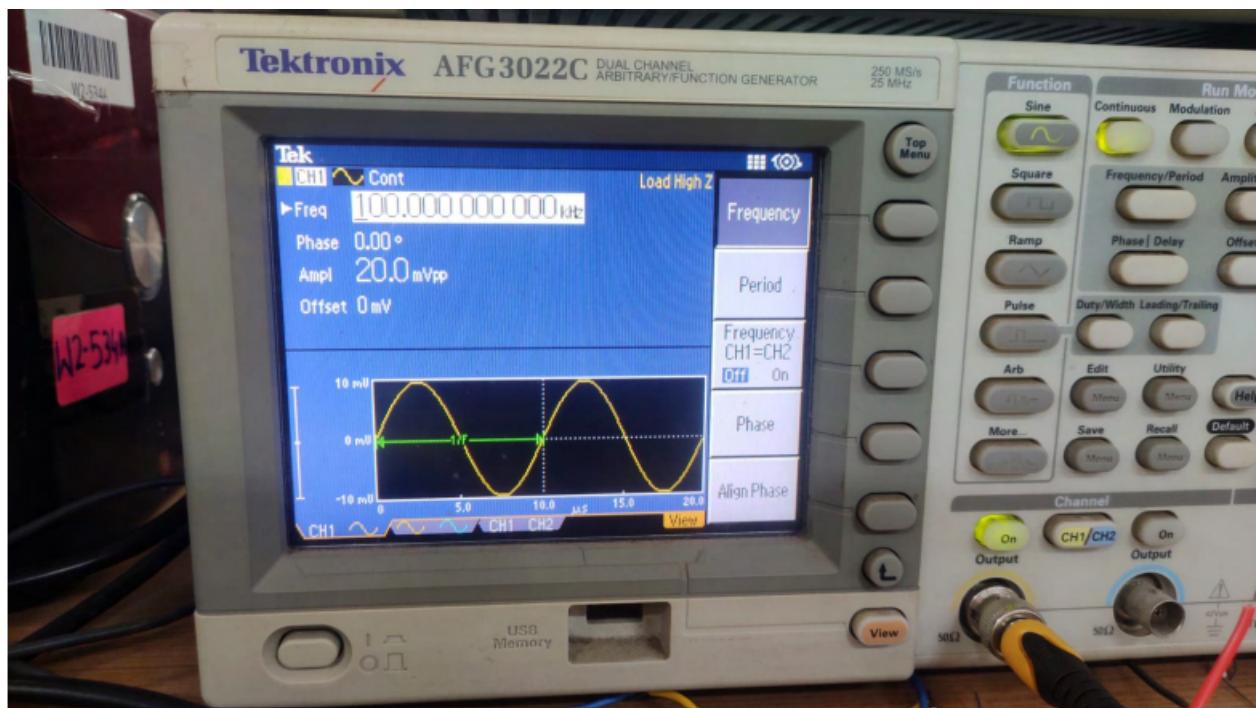


Figure 13: 100 KHz, 20mV  $V_{pp}$  sine-signal as input to 2 stage CS-CE Amplifier

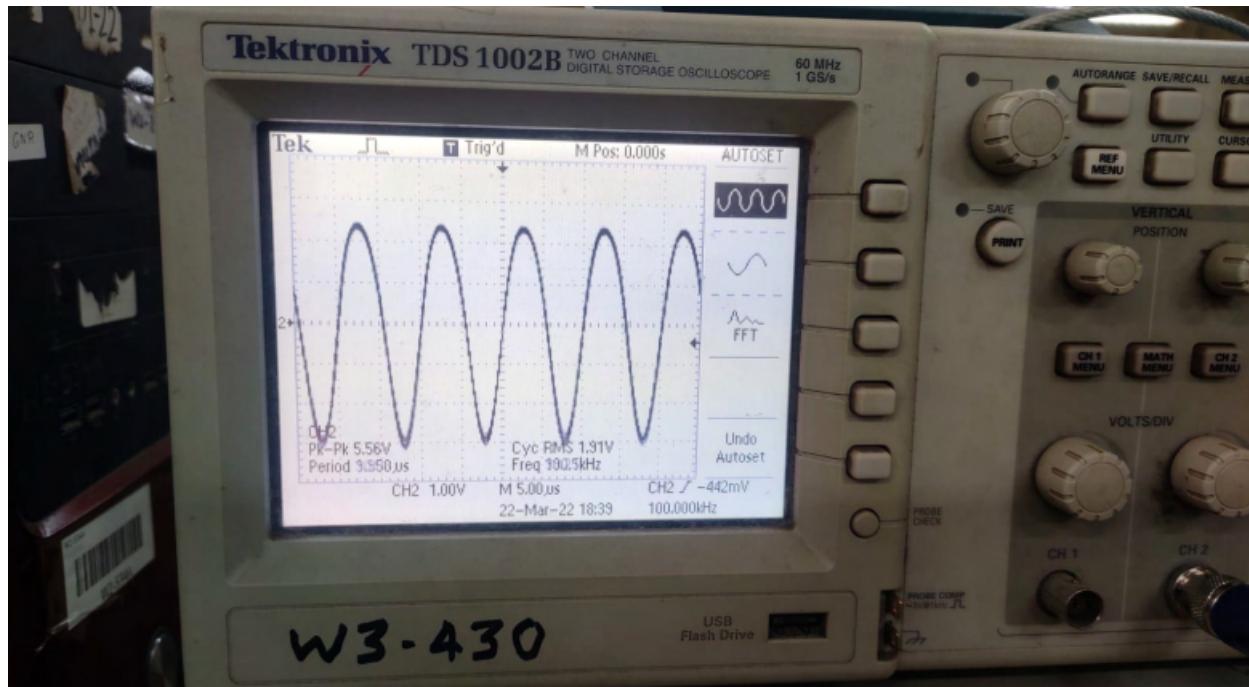
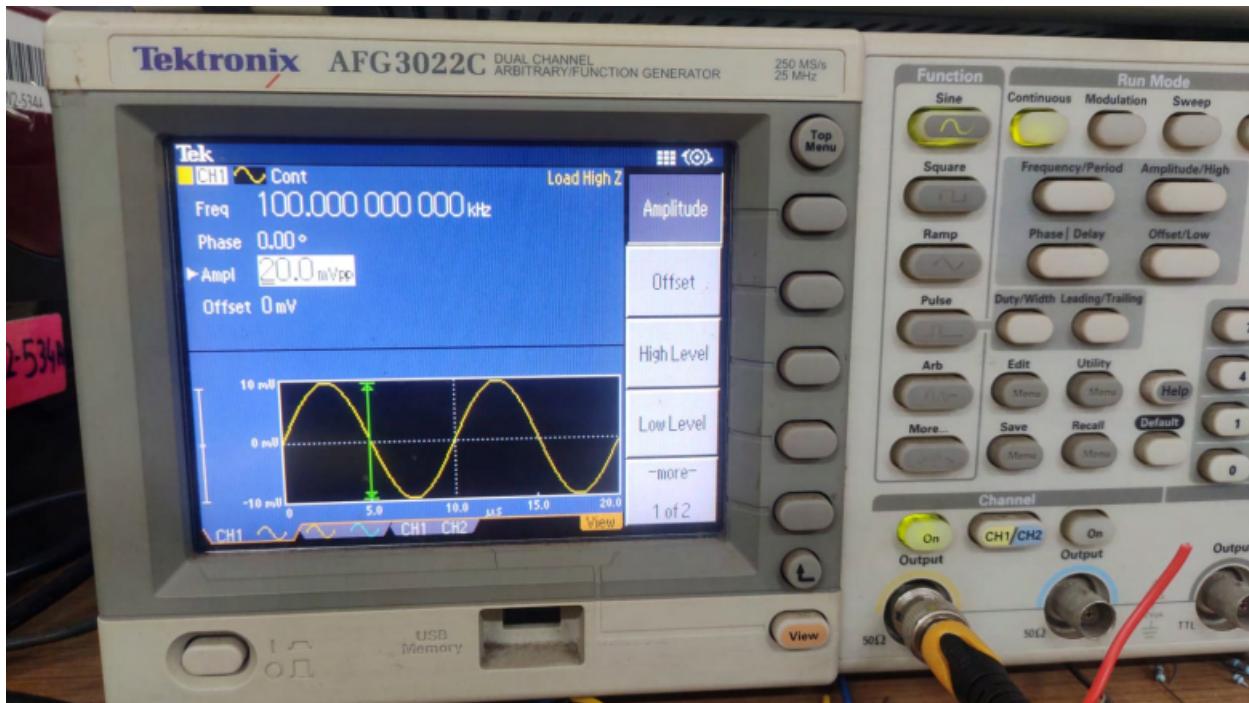


Figure 14: Output waveform

We get a gain of approximately 278

### 3.4 CS-CE-CE cascaded as an amplifier

#### 3.4.1 Experimental Results

Figure 15: 100 KHz, 20mV  $V_{pp}$  sine-signal as input to 2 stage CS-CE Amplifier

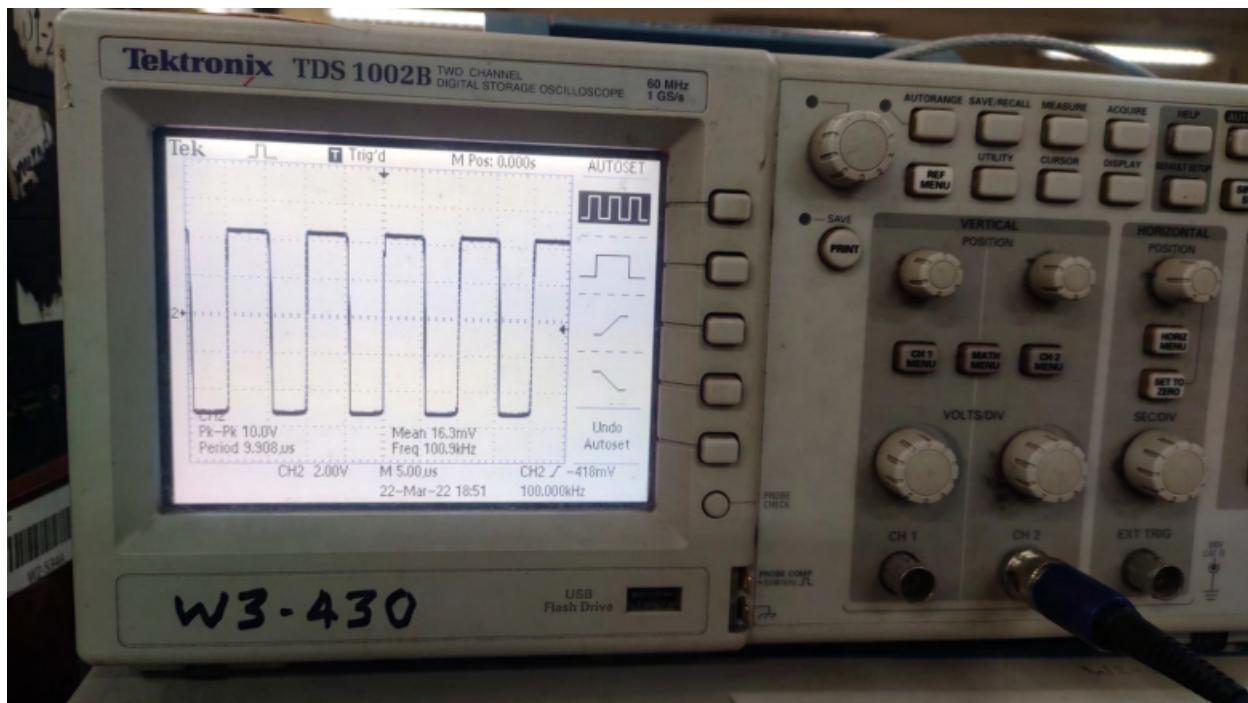


Figure 16: Output waveform

We get a gain of 500. The sinusoidal output signal gets clipped at min and max values.

### 3.5 Complete circuit using photodiode and feedback

Here we try different values of feedback resistors and different clock frequencies as an input to LED. The circuit we tested is shown below ( $A_V$  is the 3-stage [CS-CE-CE] amplifier)

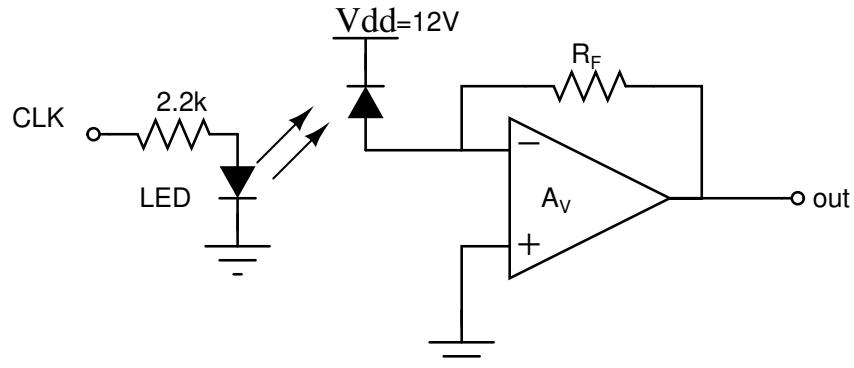


Figure 17: Transmitter-Receiver Circuit

#### 3.5.1 Experimental Results

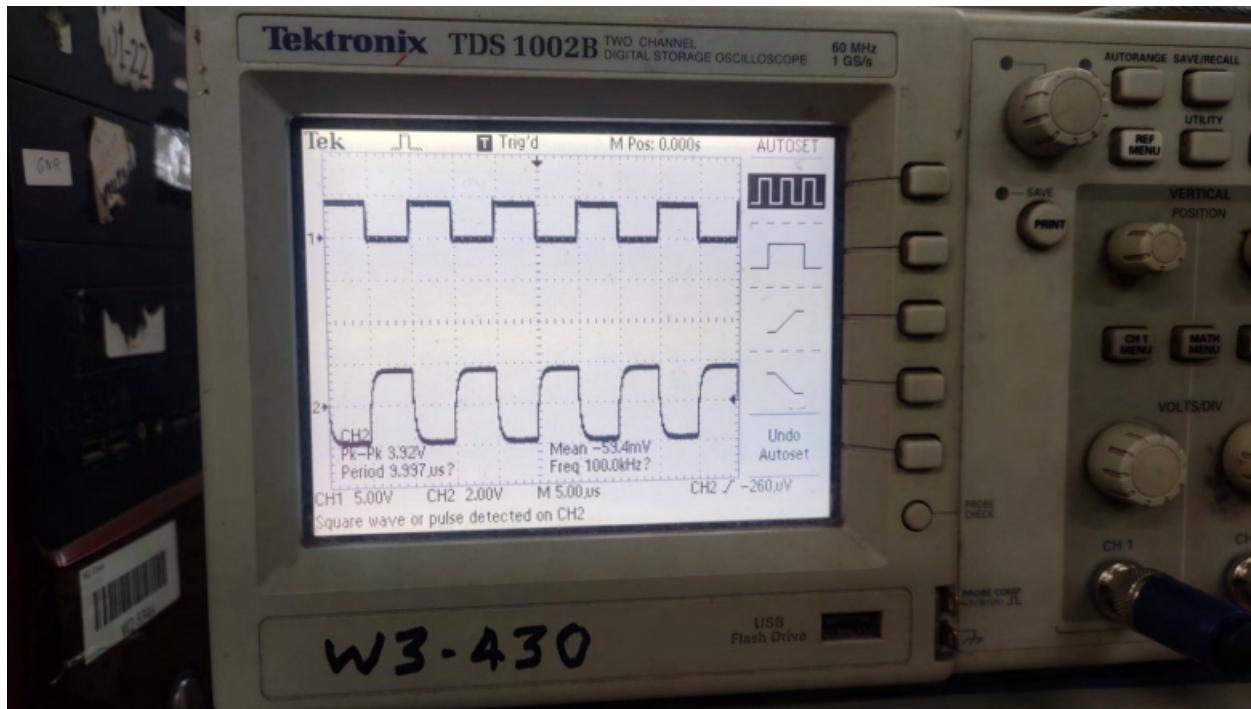
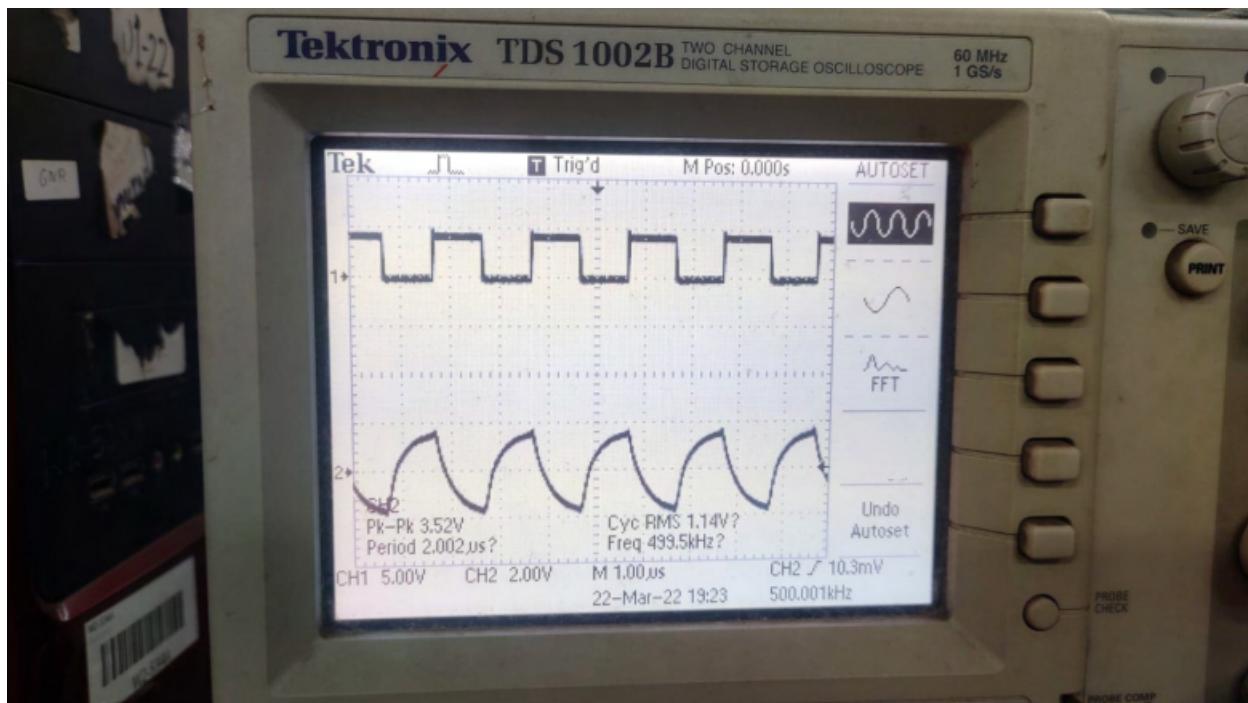
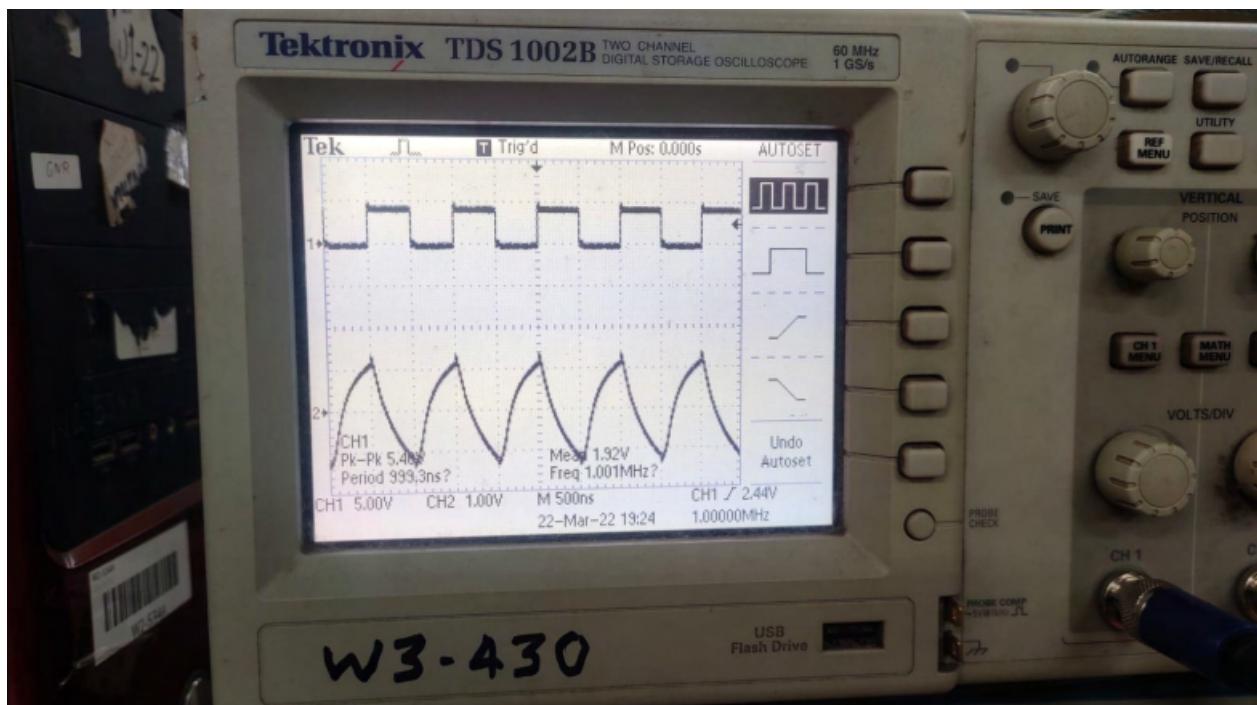
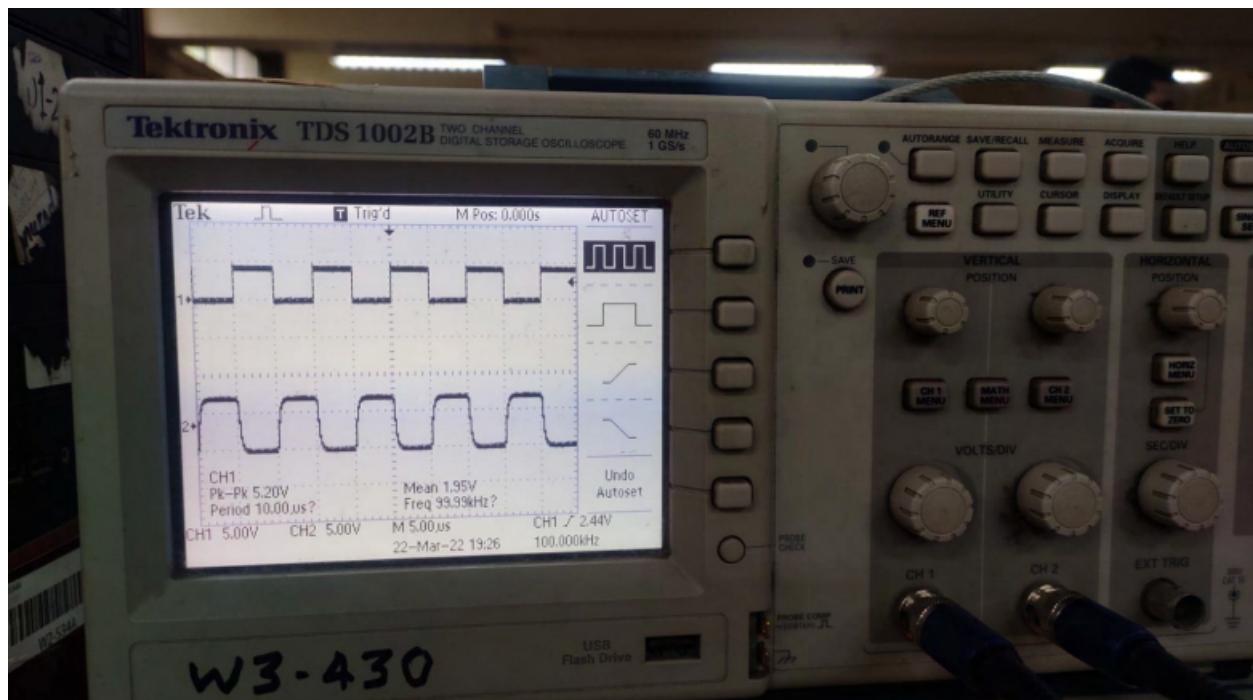
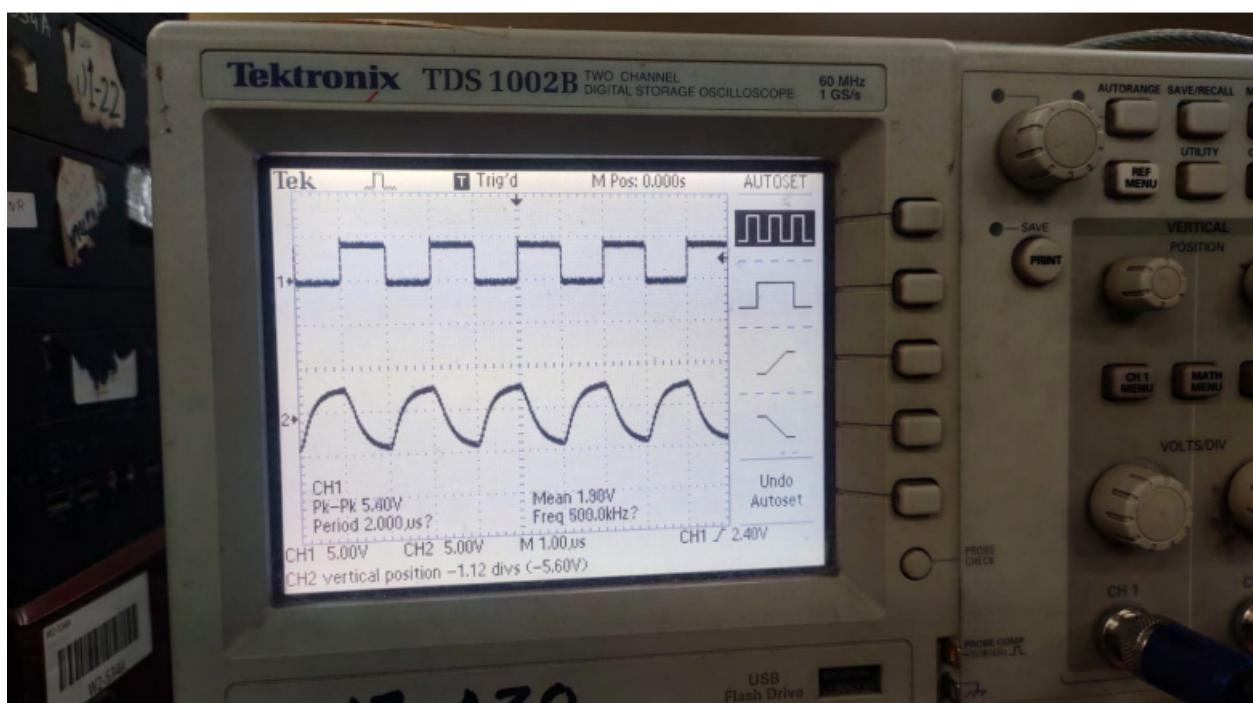
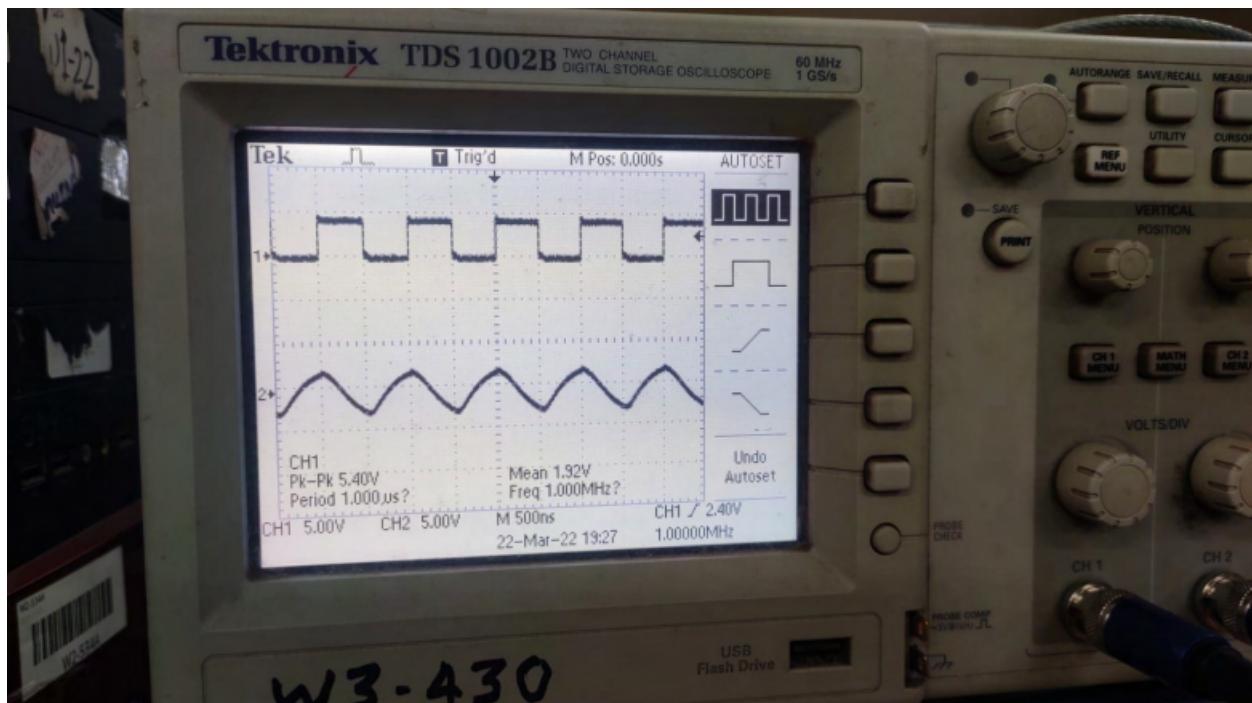
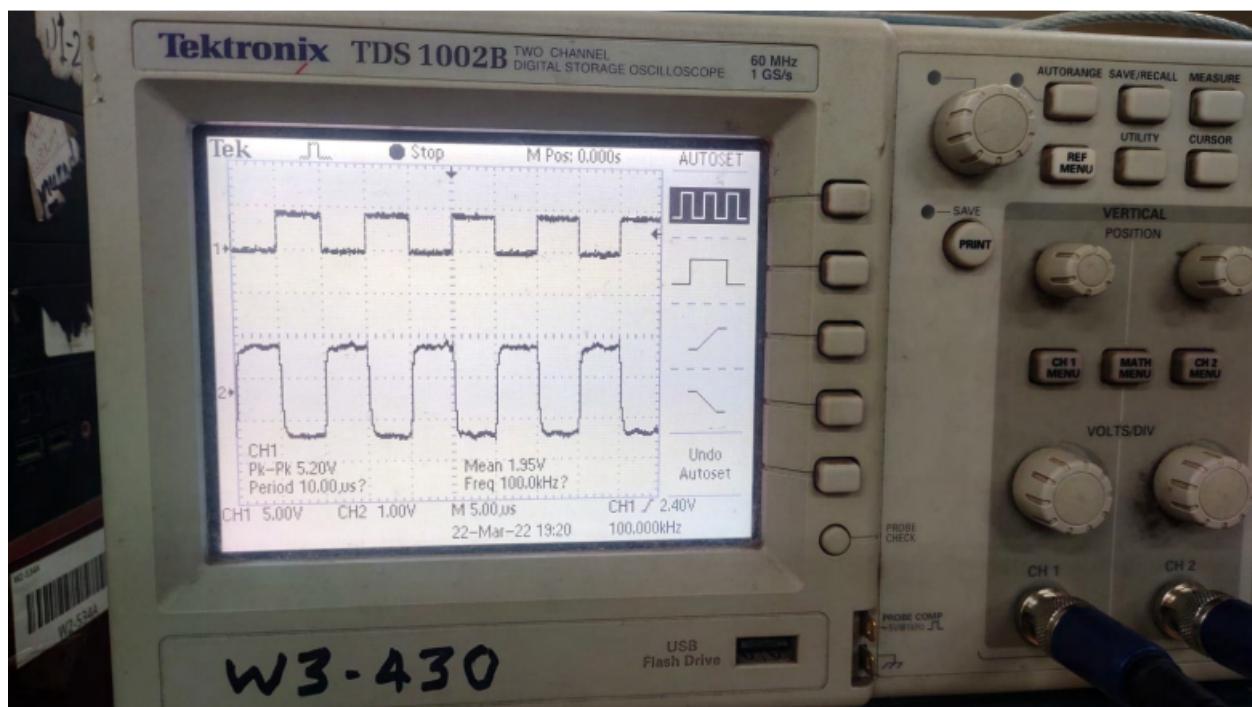
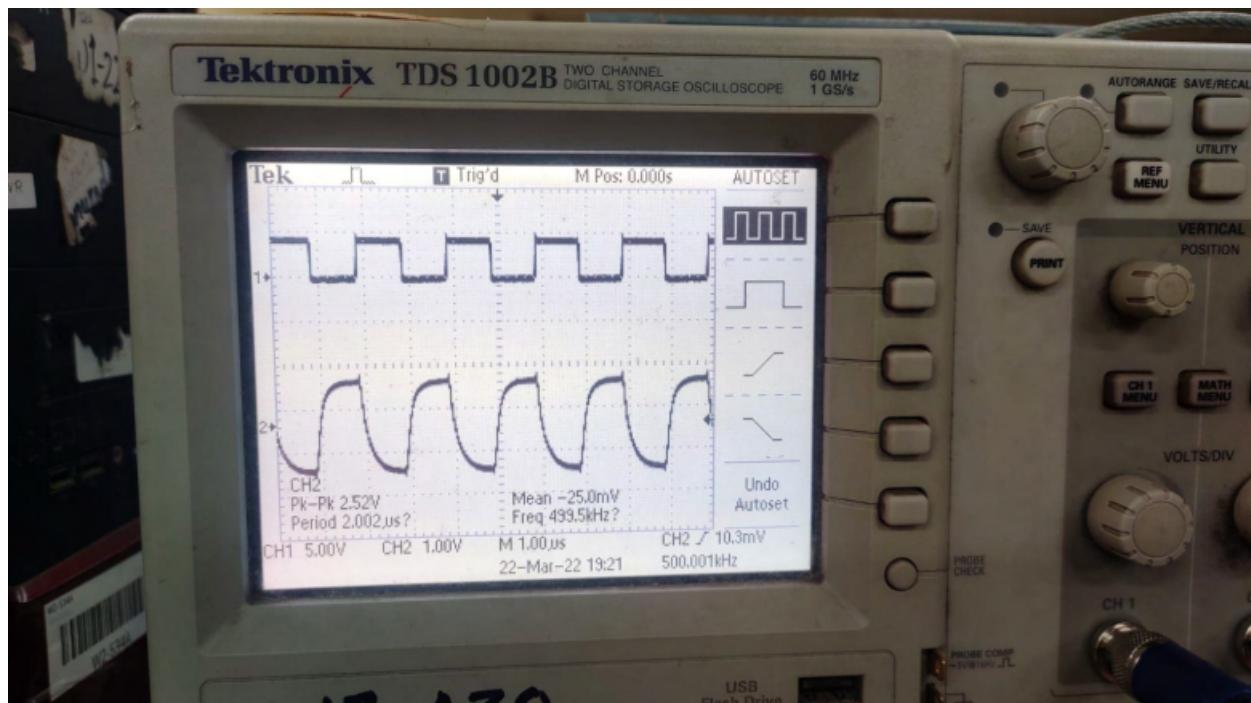
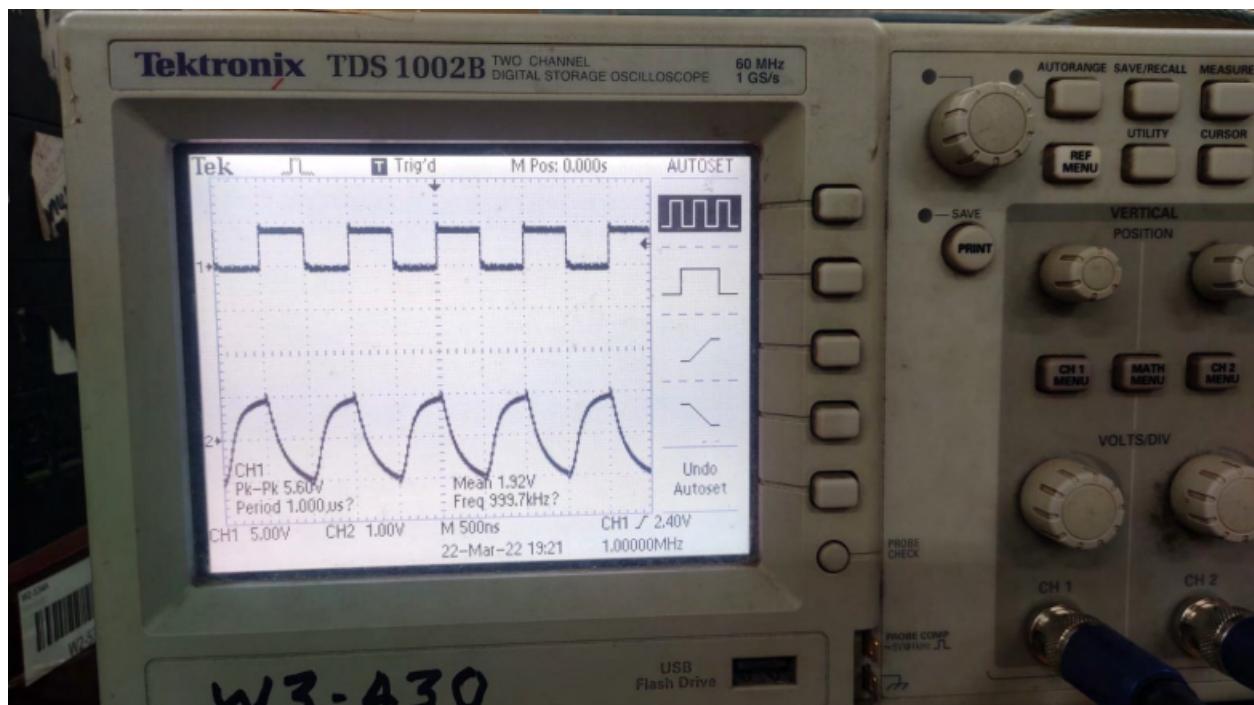


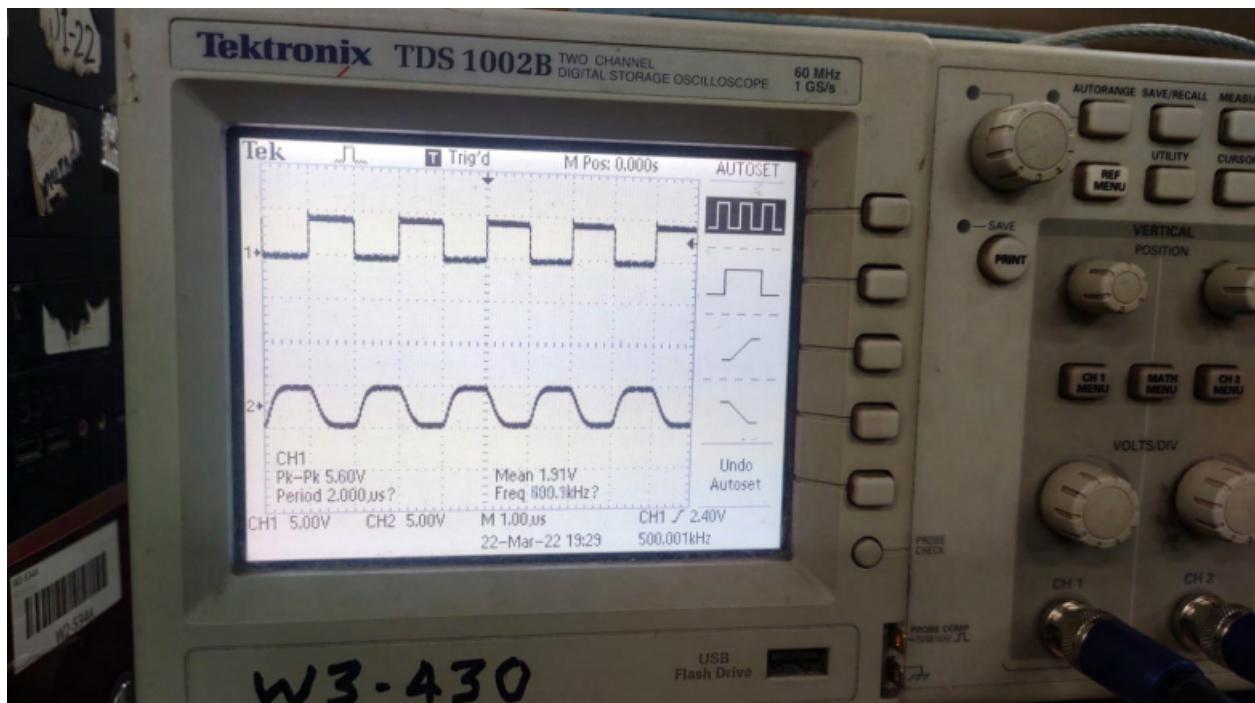
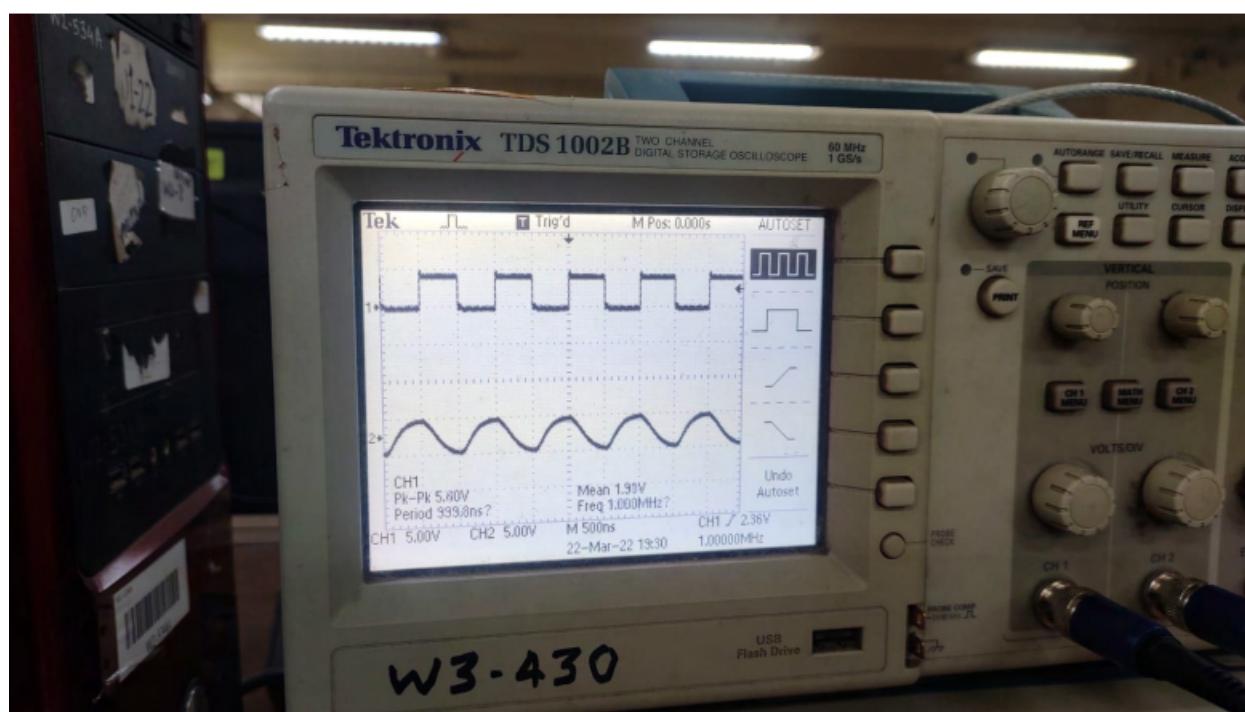
Figure 18: Output waveform for  $R_F=1M$  and  $f_{clk}=100\text{kHz}$

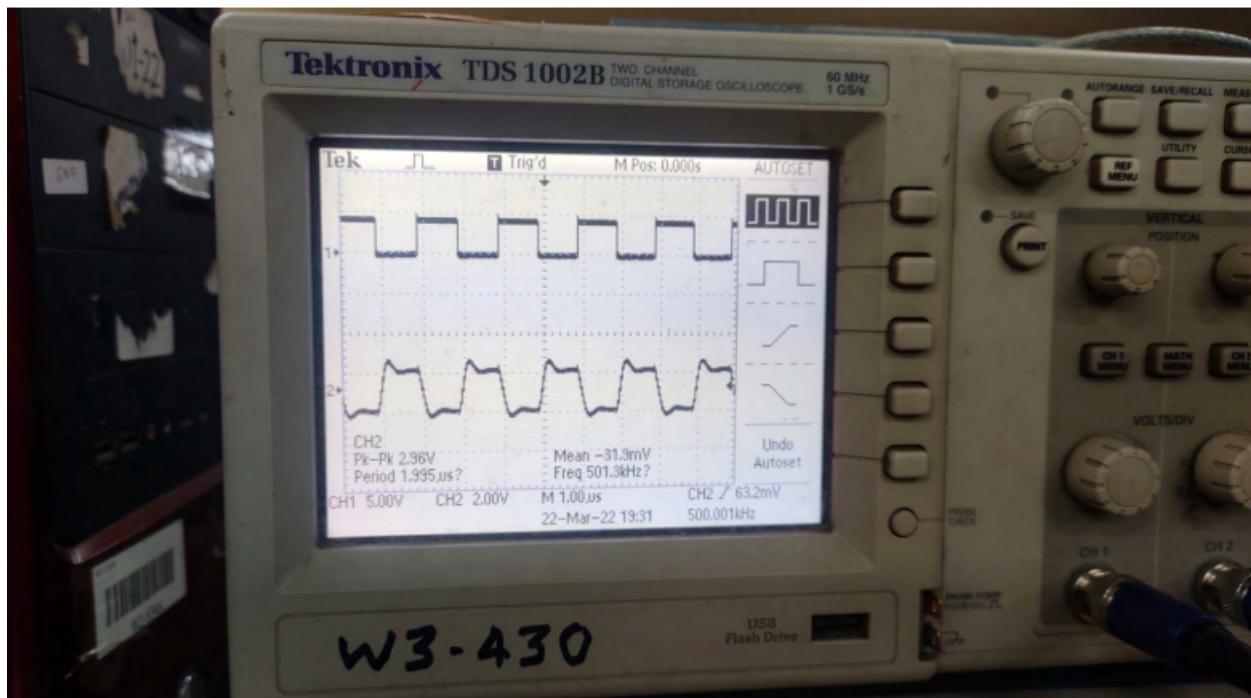
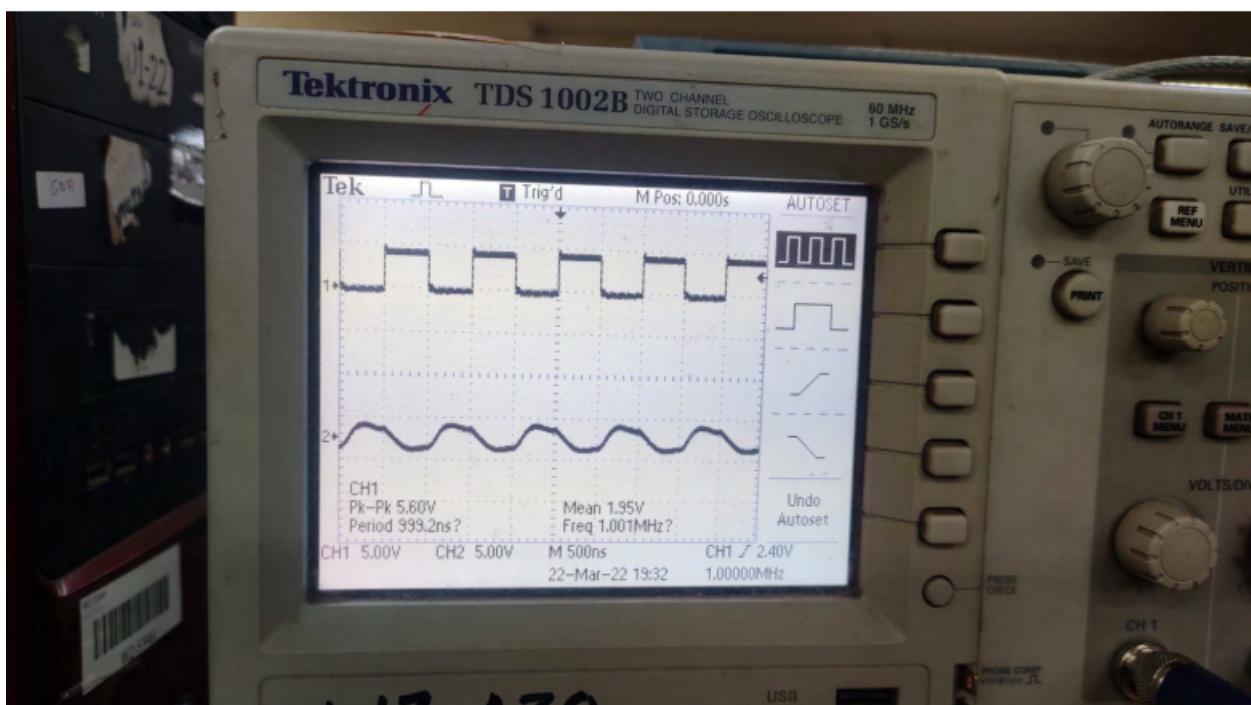
Figure 19: Output waveform for  $R_F=1\text{M}$  and  $f_{clk}=500\text{kHz}$ Figure 20: Output waveform for  $R_F=1\text{M}$  and  $f_{clk}=1\text{MHz}$

Figure 21: Output waveform for  $R_F=820k$  and  $f_{clk}=100\text{kHz}$ Figure 22: Output waveform for  $R_F=820k$  and  $f_{clk}=500\text{kHz}$

Figure 23: Output waveform for  $R_F=820\text{k}$  and  $f_{clk}=1\text{MHz}$ Figure 24: Output waveform for  $R_F=680\text{k}$  and  $f_{clk}=100\text{kHz}$

Figure 25: Output waveform for  $R_F=680k$  and  $f_{clk}=500\text{kHz}$ Figure 26: Output waveform for  $R_F=680k$  and  $f_{clk}=1\text{MHz}$

Figure 27: Output waveform for  $R_F=460k$  and  $f_{clk}=500\text{kHz}$ Figure 28: Output waveform for  $R_F=460k$  and  $f_{clk}=1\text{MHz}$

Figure 29: Output waveform for  $R_F=220k$  and  $f_{clk}=500\text{kHz}$ Figure 30: Output waveform for  $R_F=220k$  and  $f_{clk}=1\text{MHz}$

### 3.6 PCB Design

The schematic and board of the PCB designed for this version is shown below.

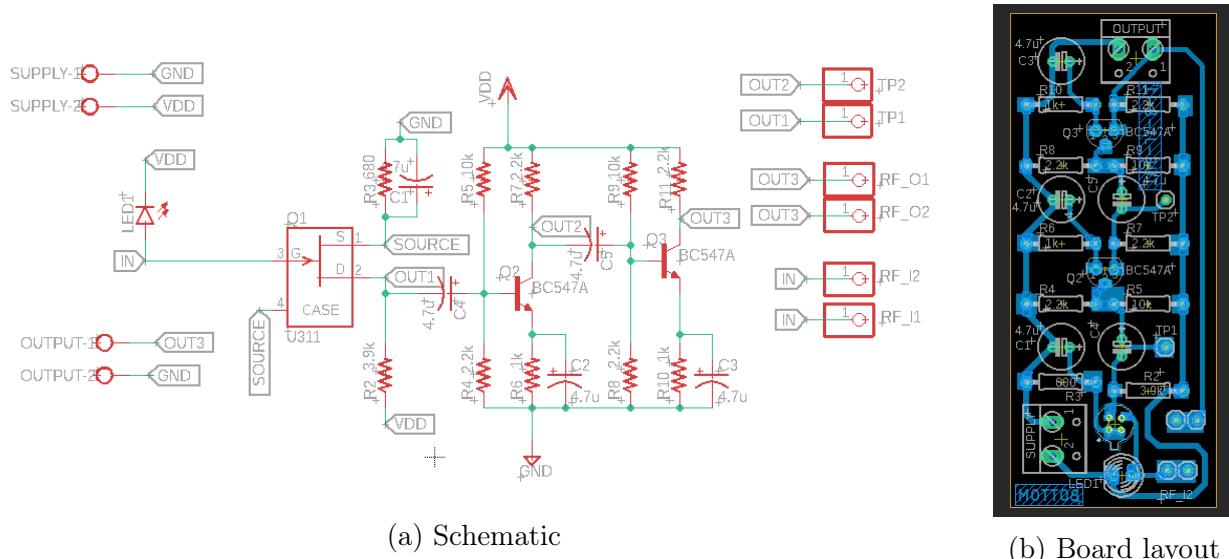


Figure 31: Designed PCB

### 3.6.1 PCB Testing experimental results

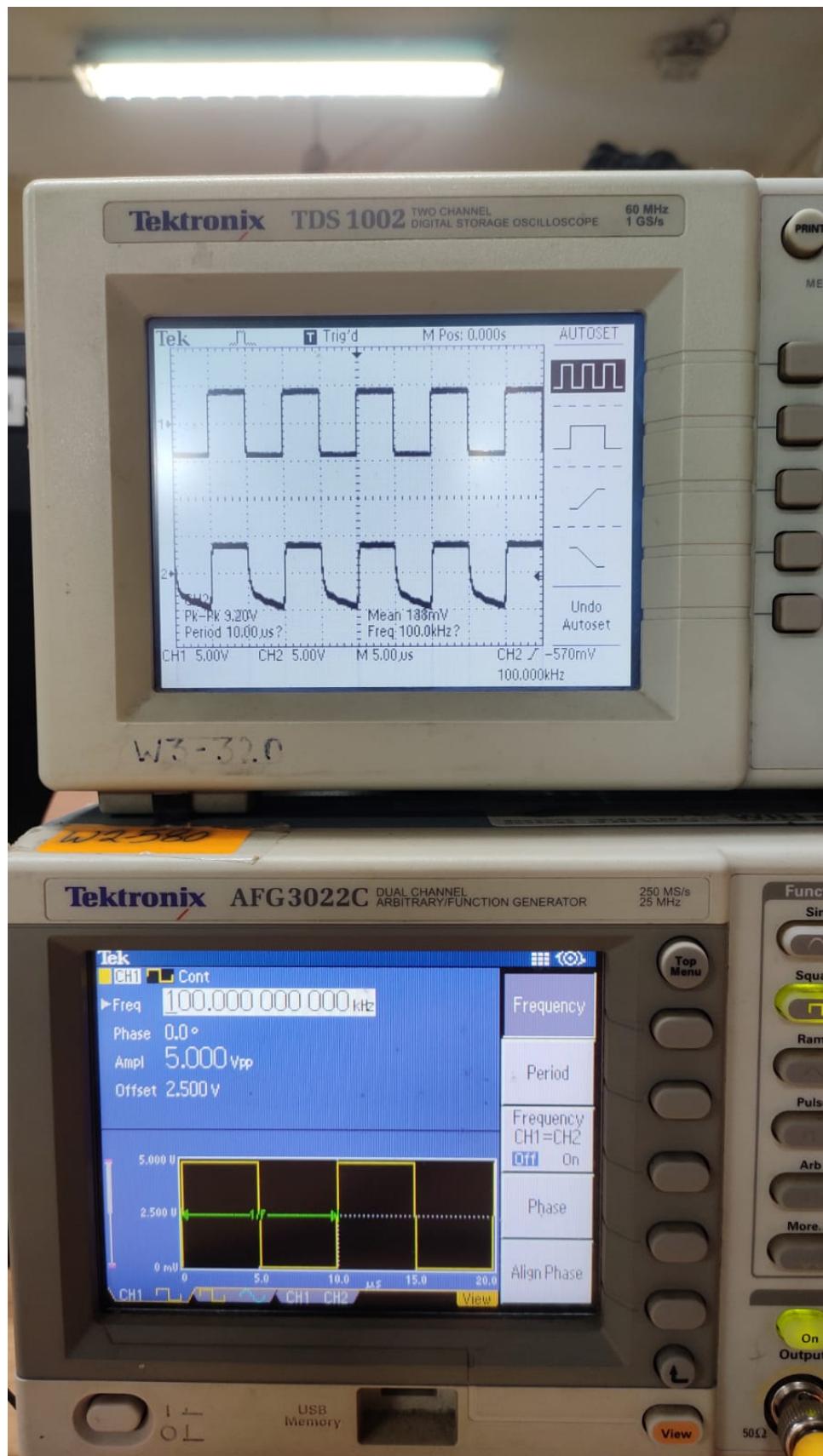
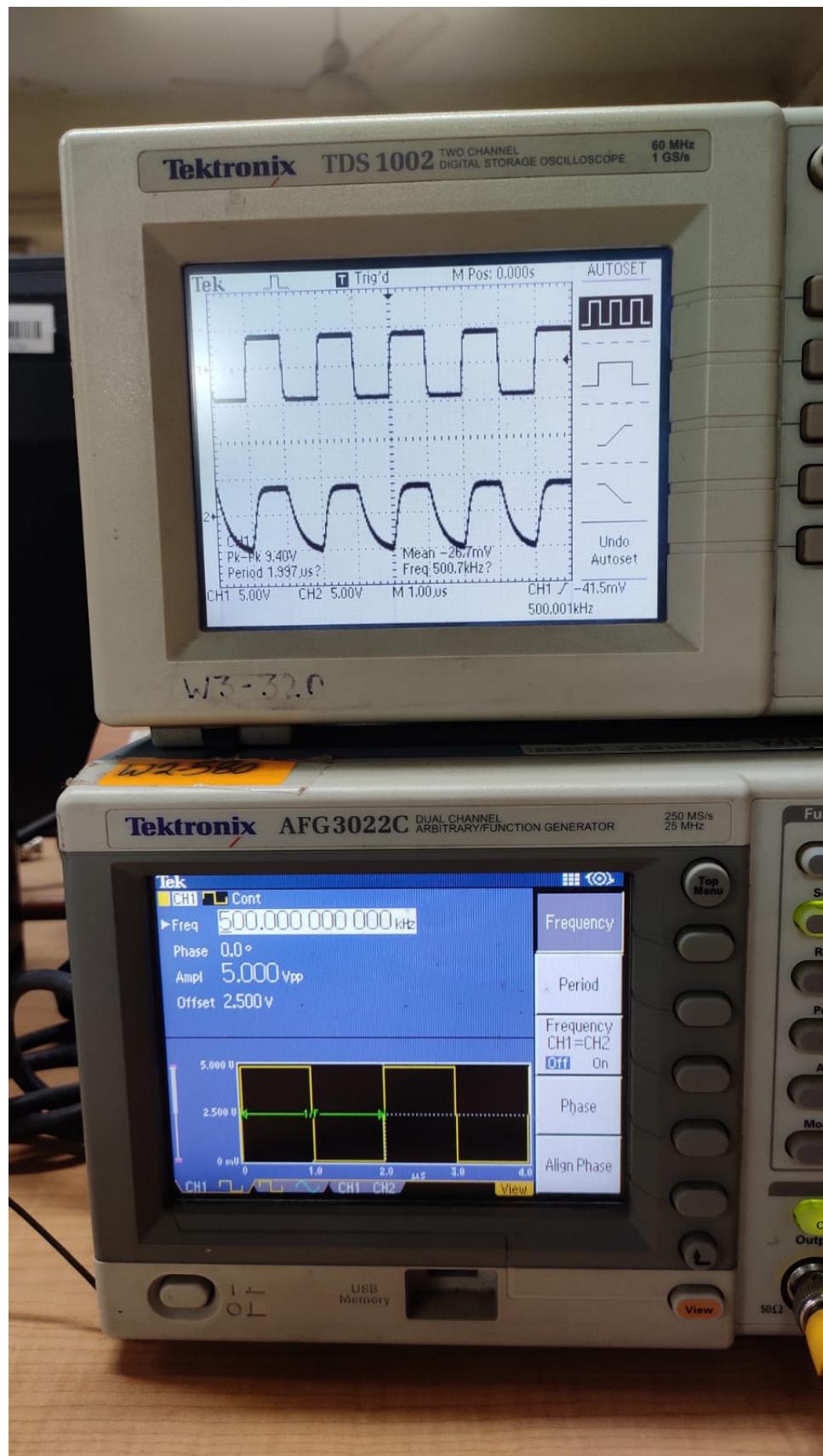


Figure 32: Input-Output waveforms for  $R_F=820k$  and  $f_{clk}=100kHz$

Figure 33: Input-Output waveforms for  $R_F=820k$  and  $f_{clk}=500\text{KHz}$

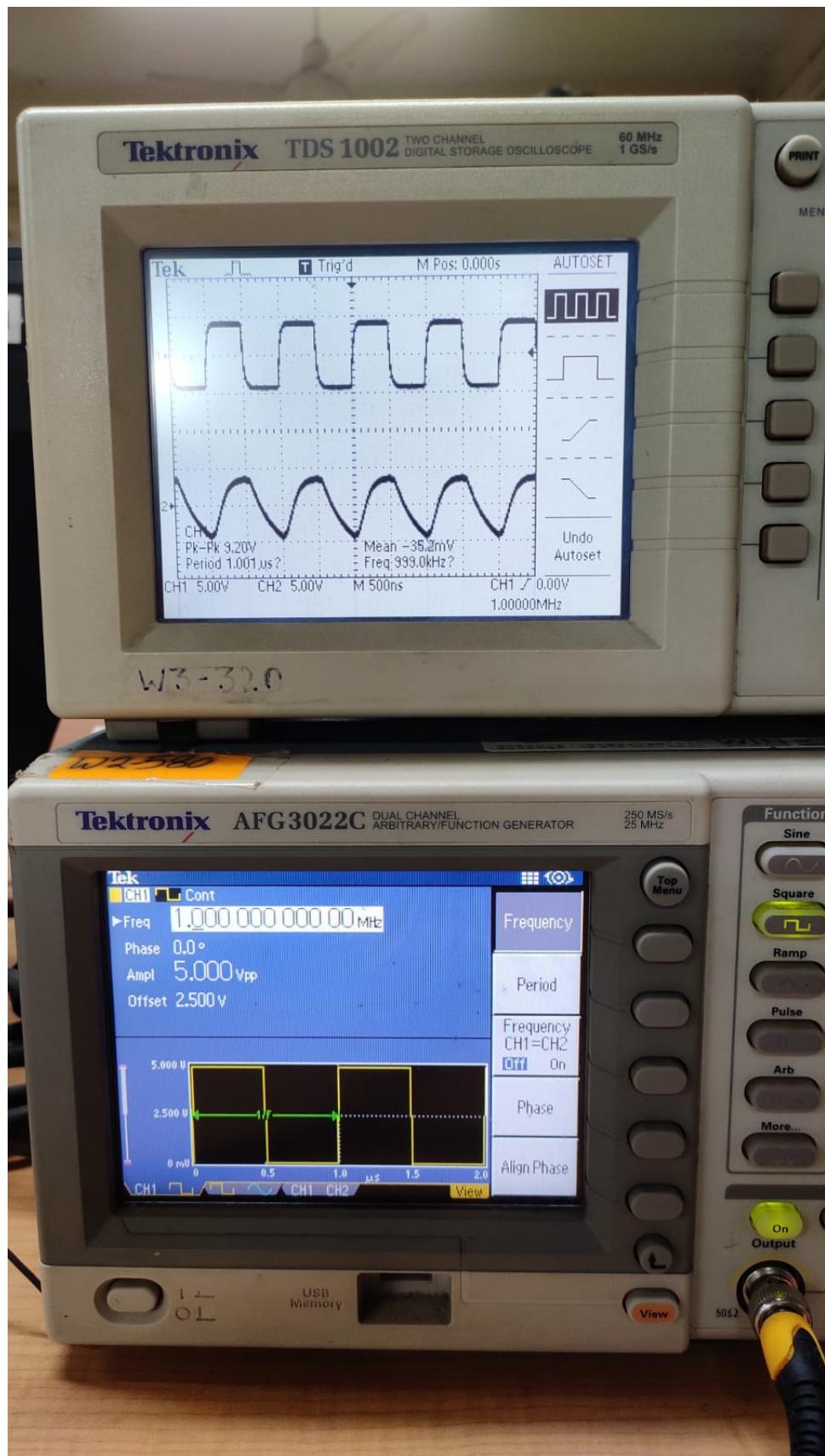


Figure 34: Input-Output waveforms for  $R_F=820k$  and  $f_{clk}=1\text{MHz}$

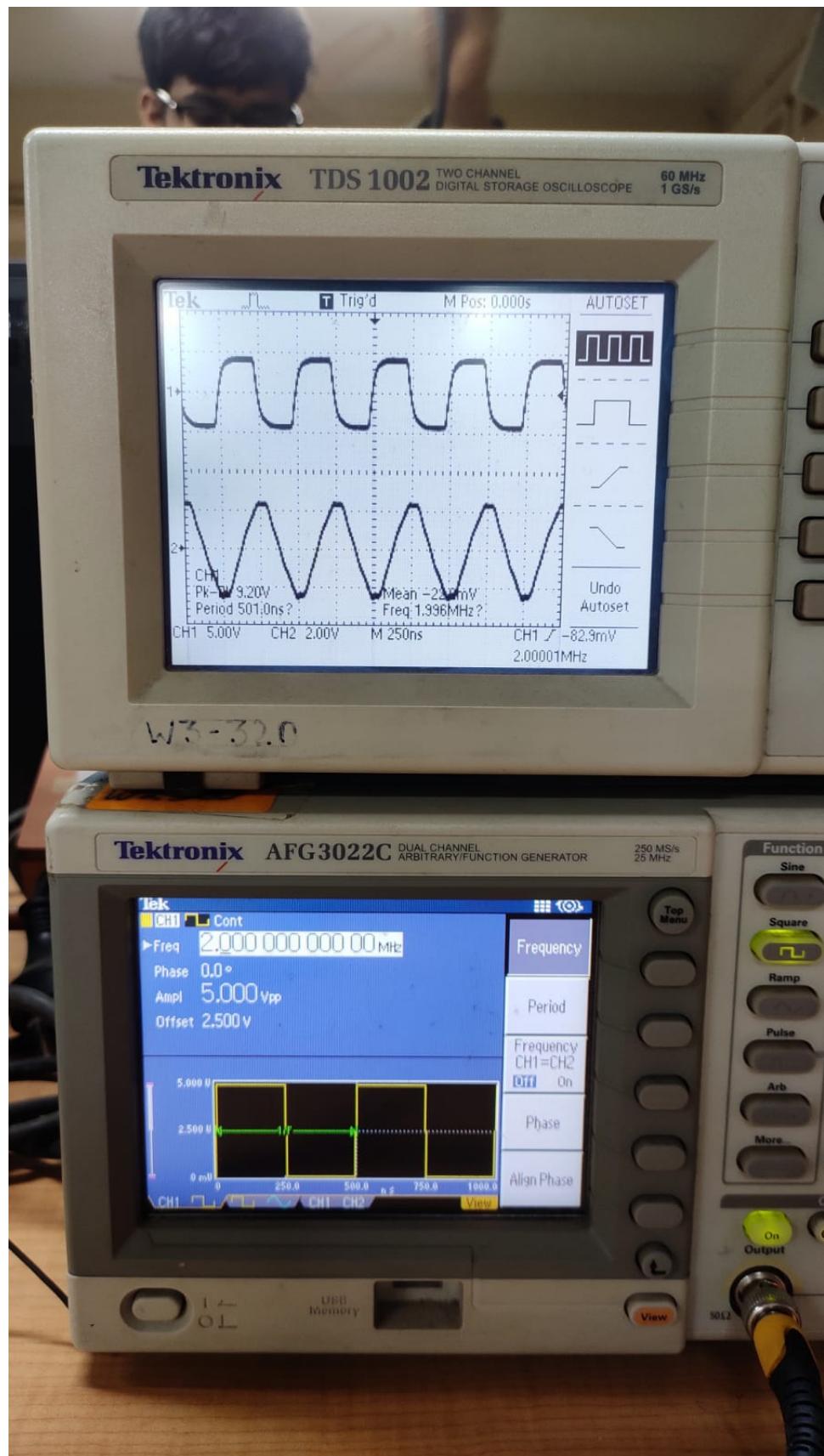


Figure 35: Input-Output waveforms for  $R_F=820k$  and  $f_{clk}=2\text{MHz}$

## 4 TIA Version 2

The circuit diagram of the design is shown below

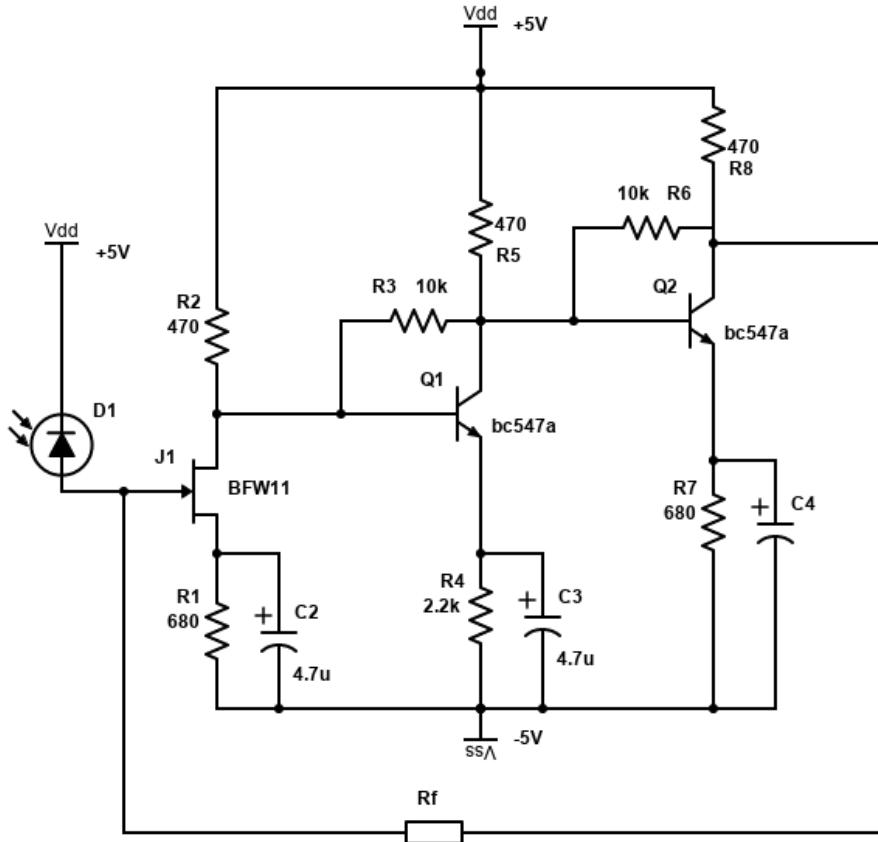


Figure 36: Circuit Diagram of our TIA Version-2 design

In this design, we incorporated collector-base biasing and did not use any coupling capacitors in order to facilitate dc gain. While analysing the stages, we also studied the 3dB bandwidth of individual stages while cascading each stage.

### 4.1 CS stage using JFET

The observed 3dB bandwidth for CS amplifier using BFW11 was **15MHz**.

### 4.2 CE stage using BJT

The observed 3dB bandwidth for CS amplifier using BC547 was around **15 MHz**, different for different emitter resistance.

- For  $R_d$  value of 470 Ohm, the bandwidth was 15 MHz
- For  $R_d$  value of 680 Ohm, the bandwidth was 6 MHz

### 4.3 Observations

- The 3db bandwidth depends on bypass capacitor values and resistance values.

- Adding a small bypass capacitor value in the third stage leads to better gain and higher bandwidth
- The circuit also acts like a high pass filter in some RC configurations
- Due to lower swing present in a  $\pm 5$  Volt supply, the third stage might go into saturation
- This configuration has a higher bandwidth as compared to the previous version
- Due to smaller resistances  $R_c$  and  $R_d$ , loading problem is not observed.
- Increasing base to collector resistance led to an increase in gain due to higher  $V_{cb}$  and higher collector current.

#### 4.4 Simulation results

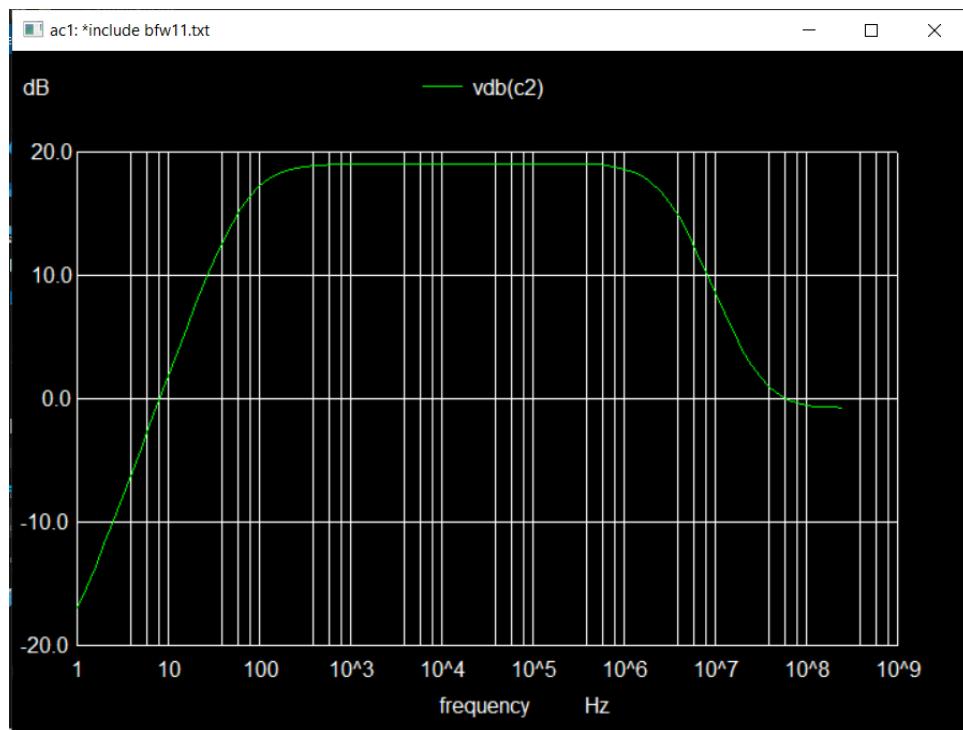


Figure 37: Bode plot (magnitude) at a high overall gain value, lower bandwidth

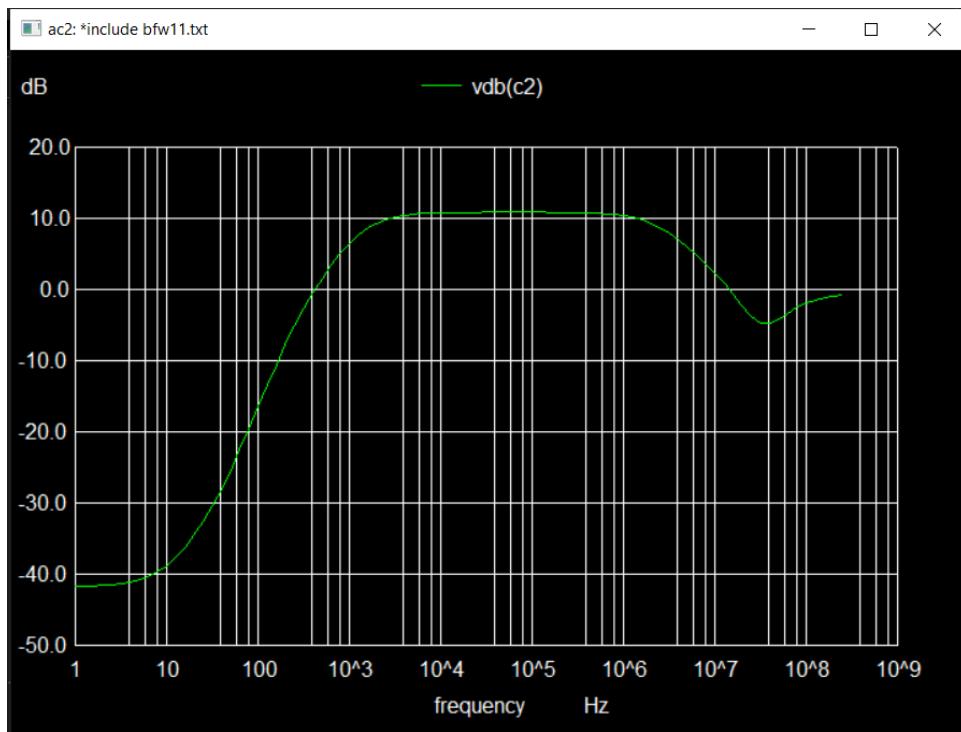


Figure 38: Bode plot (magnitude) at a low overall gain value, higher bandwidth

#### 4.5 Experimental Results

The feedback resistor we use is  $420\text{k}\Omega$  which gives The DC values for JFET stage are shown below

$$V_S = -0.32V \quad V_D = 1.45V \quad I_{DS} = 7.55mA$$

The DC values of first CE stage are

$$V_B = 1.45V \quad V_C = 2.35V \quad V_E = 0.98V$$

The DC values of second CE stage are

$$V_B = 2.35V \quad V_C = 2.52V \quad V_E = 1.6V$$

#### 4.6 Experimental results for sinusoidal input to TIA

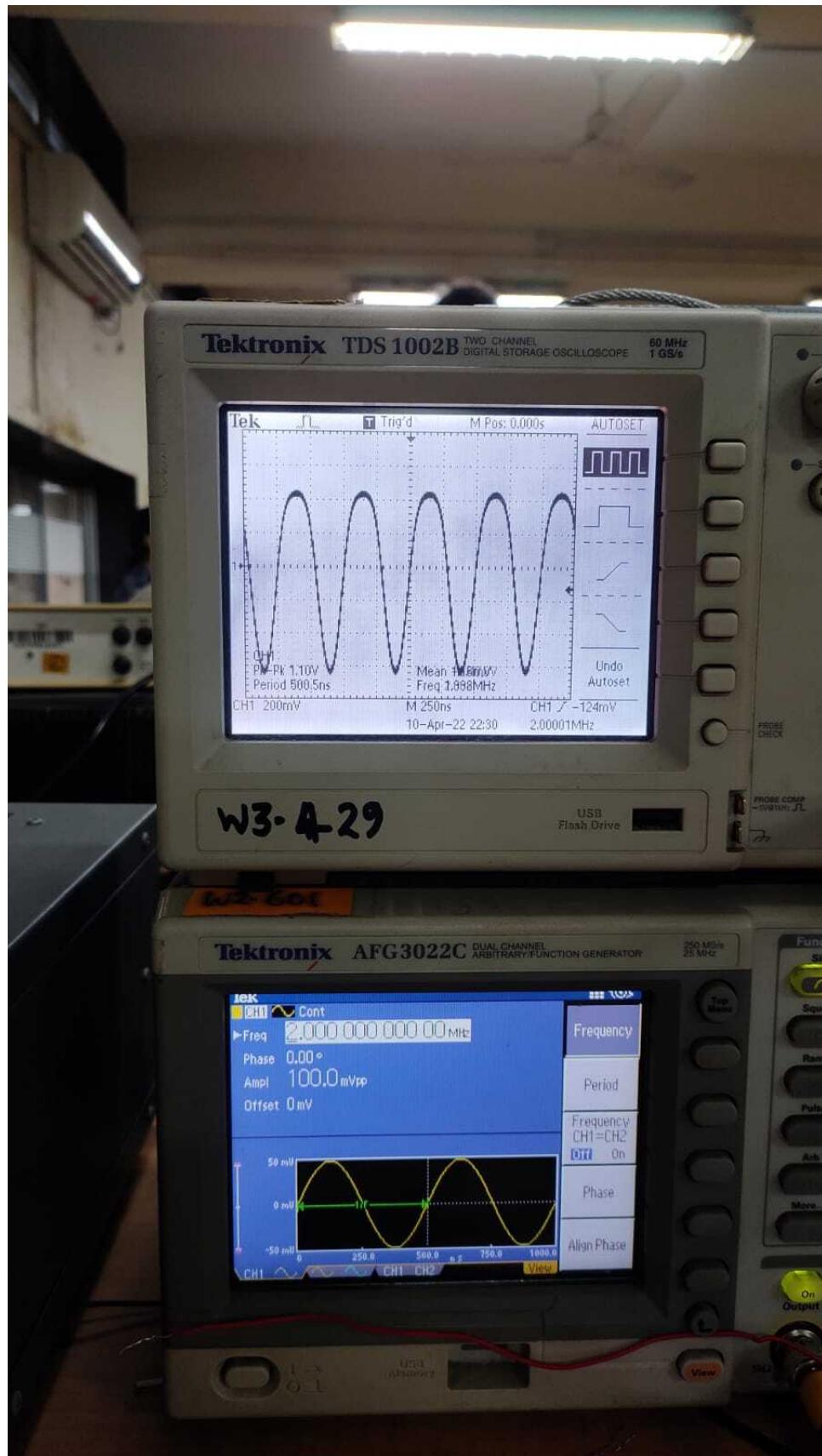
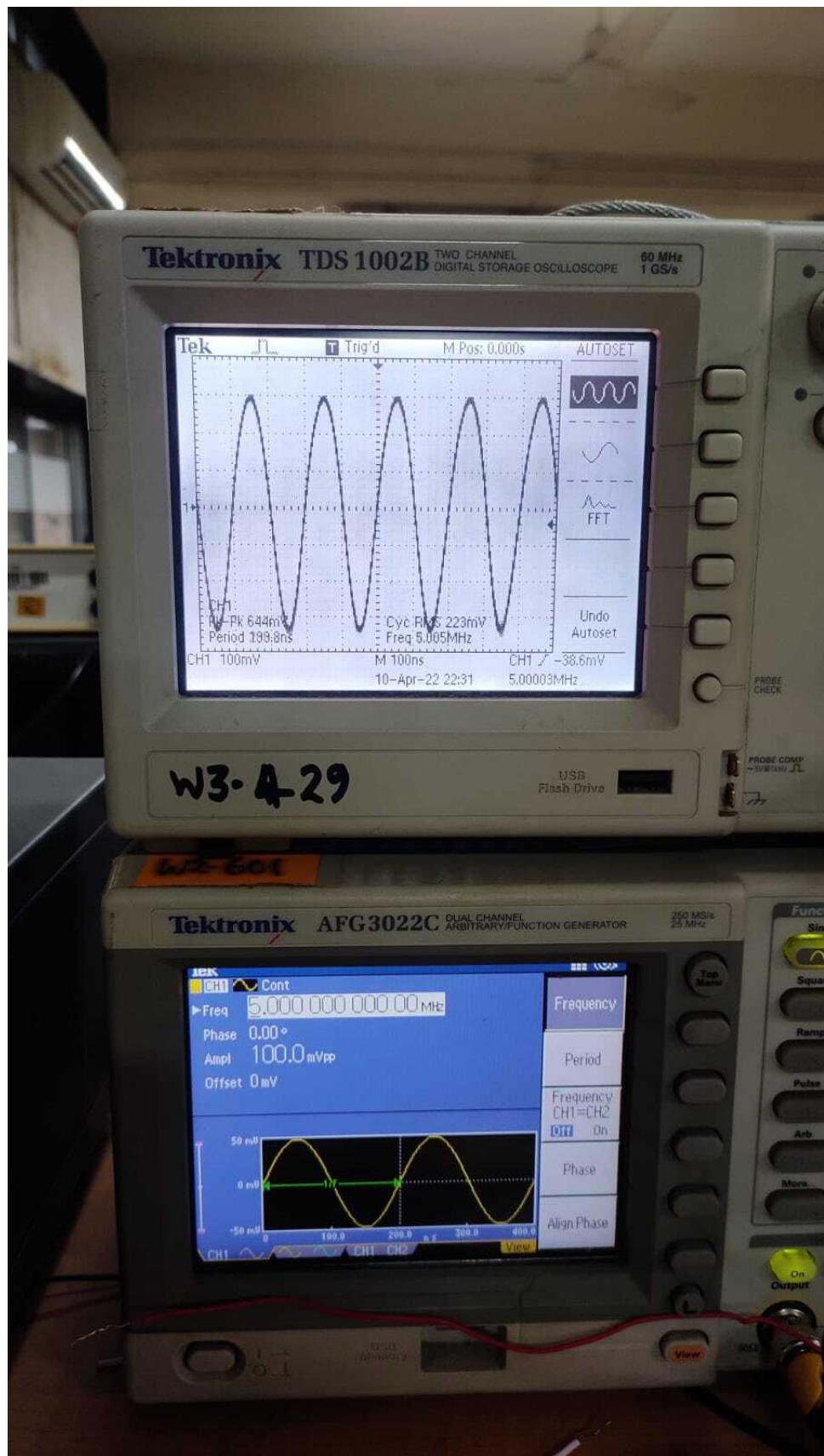
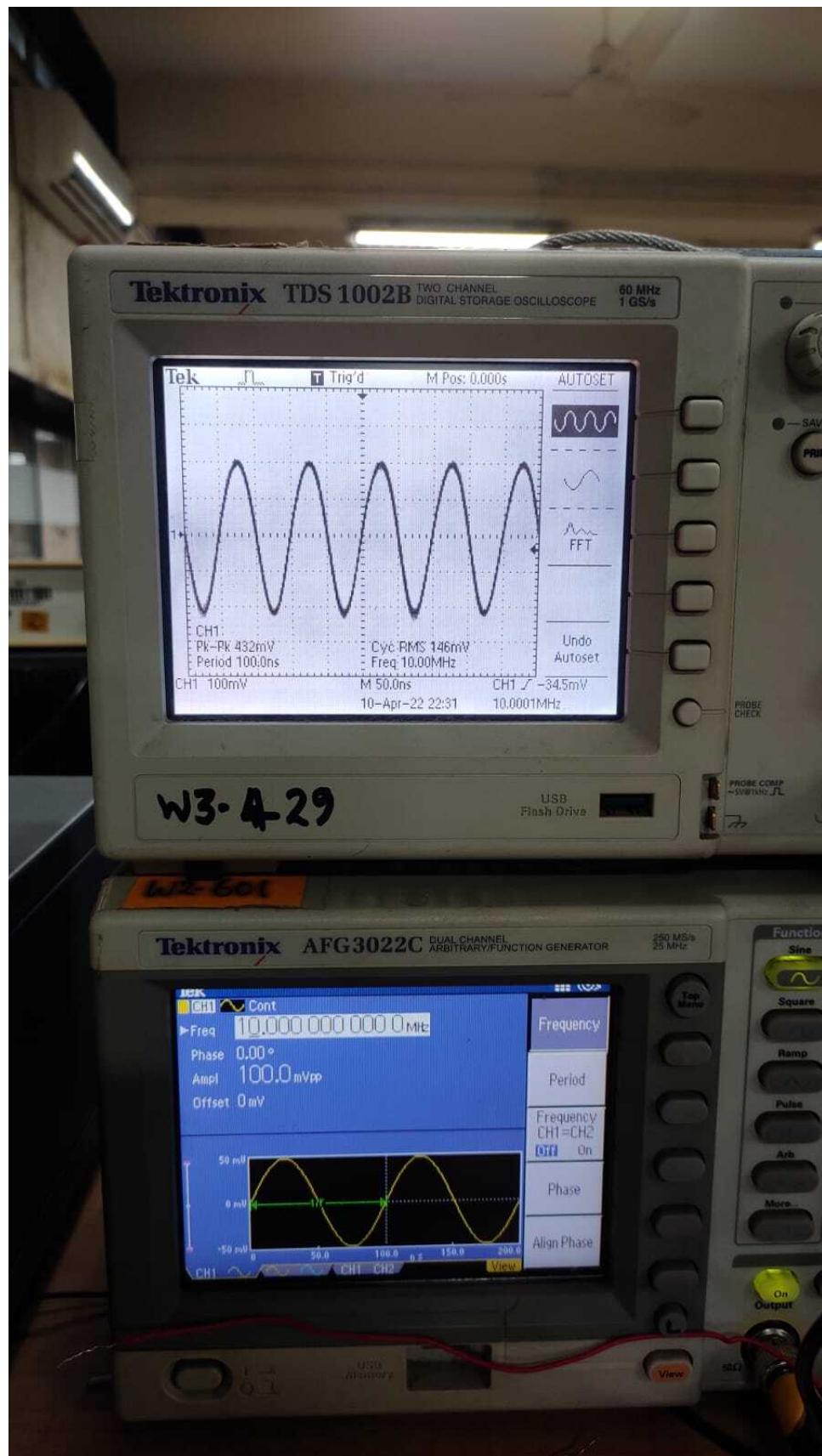
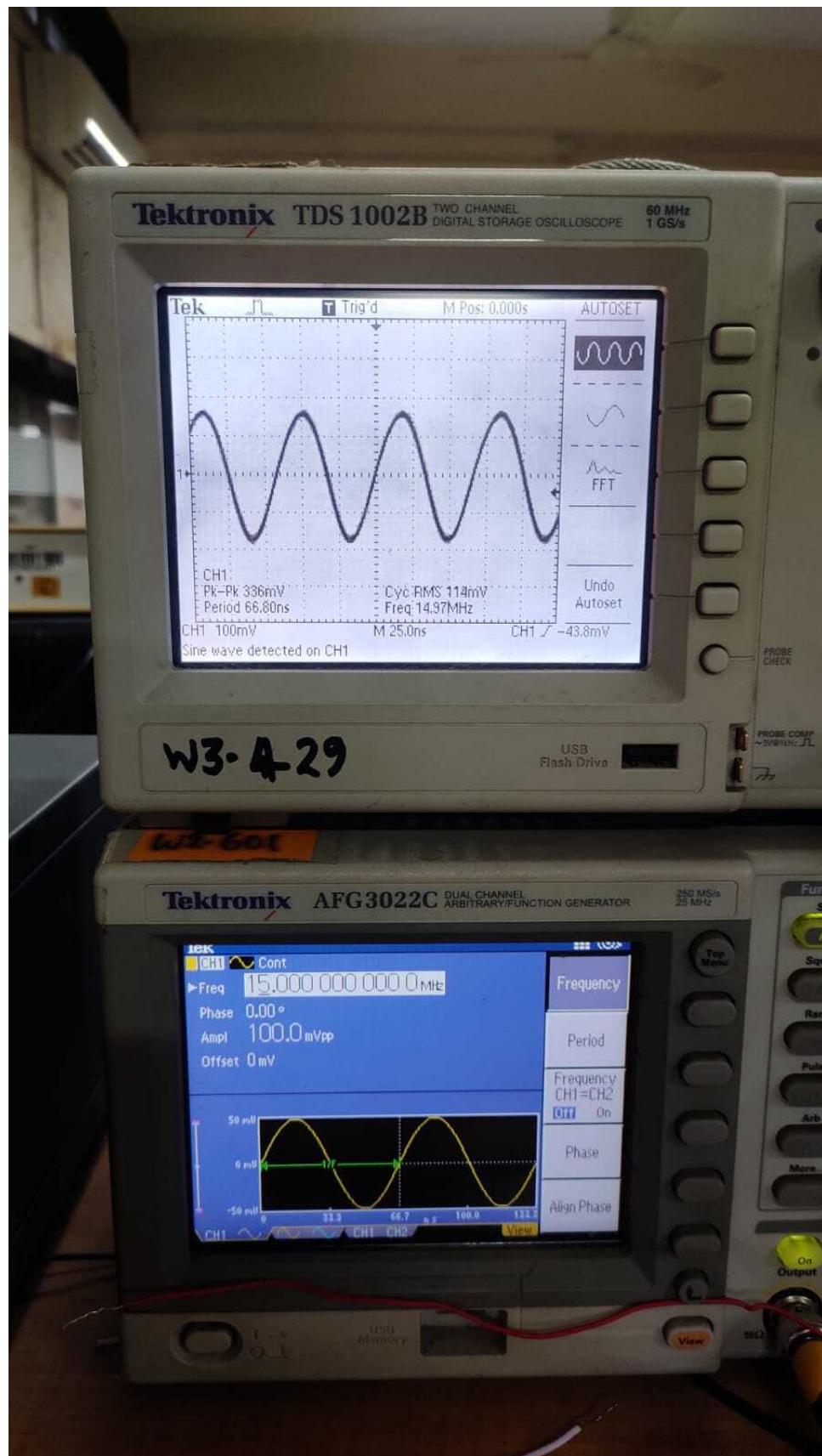
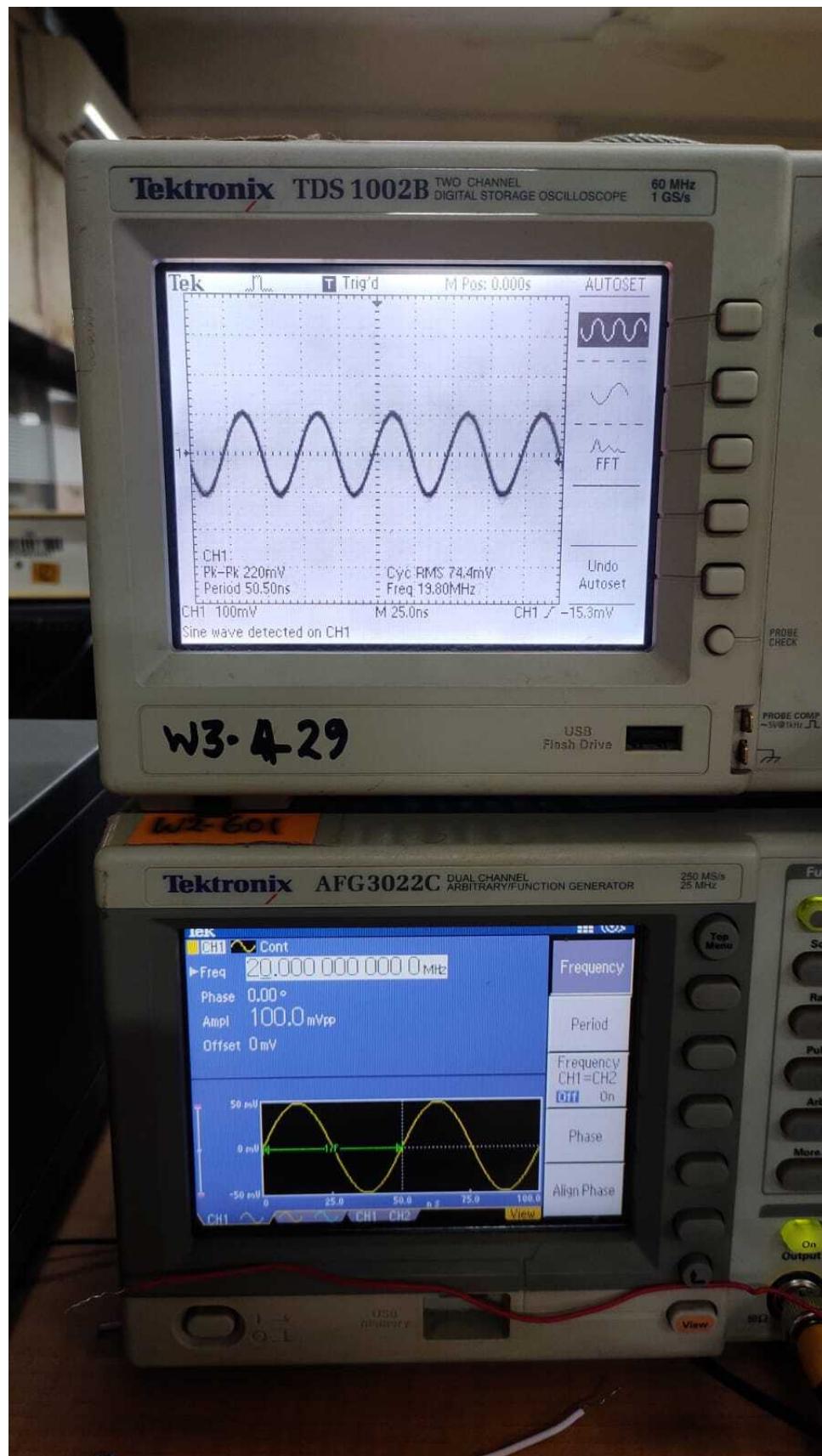


Figure 39: Input-Output waveforms for  $f_{clk}=2\text{MHz}$

Figure 40: Input-Output waveforms for  $f_{clk}=5\text{MHz}$

Figure 41: Input-Output waveforms for  $f_{clk}=10\text{MHz}$

Figure 42: Input-Output waveforms for  $f_{clk}=15\text{MHz}$

Figure 43: Input-Output waveforms for  $f_{clk}=20\text{MHz}$

#### 4.7 Experimental results using transmitter-receiver

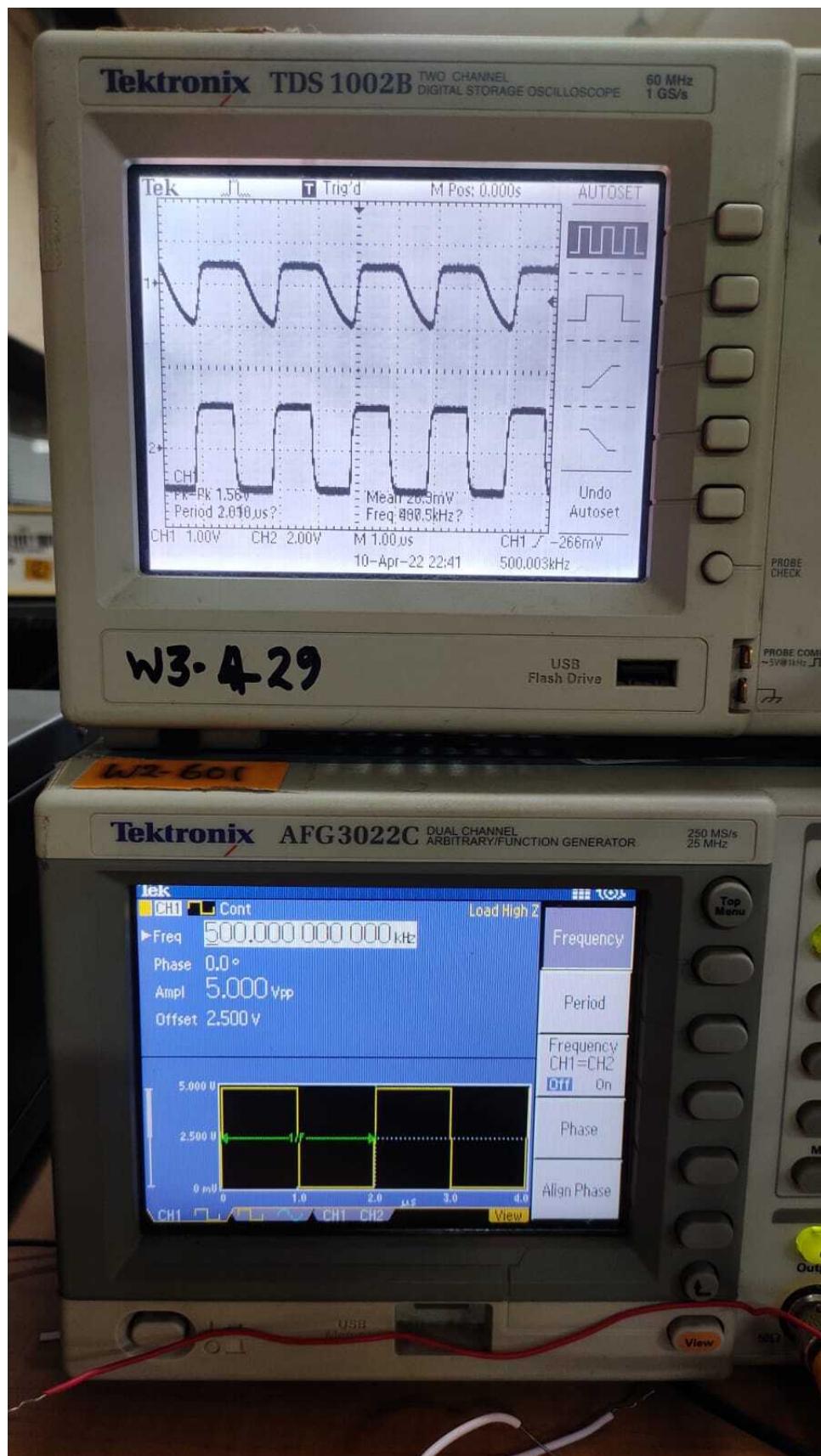
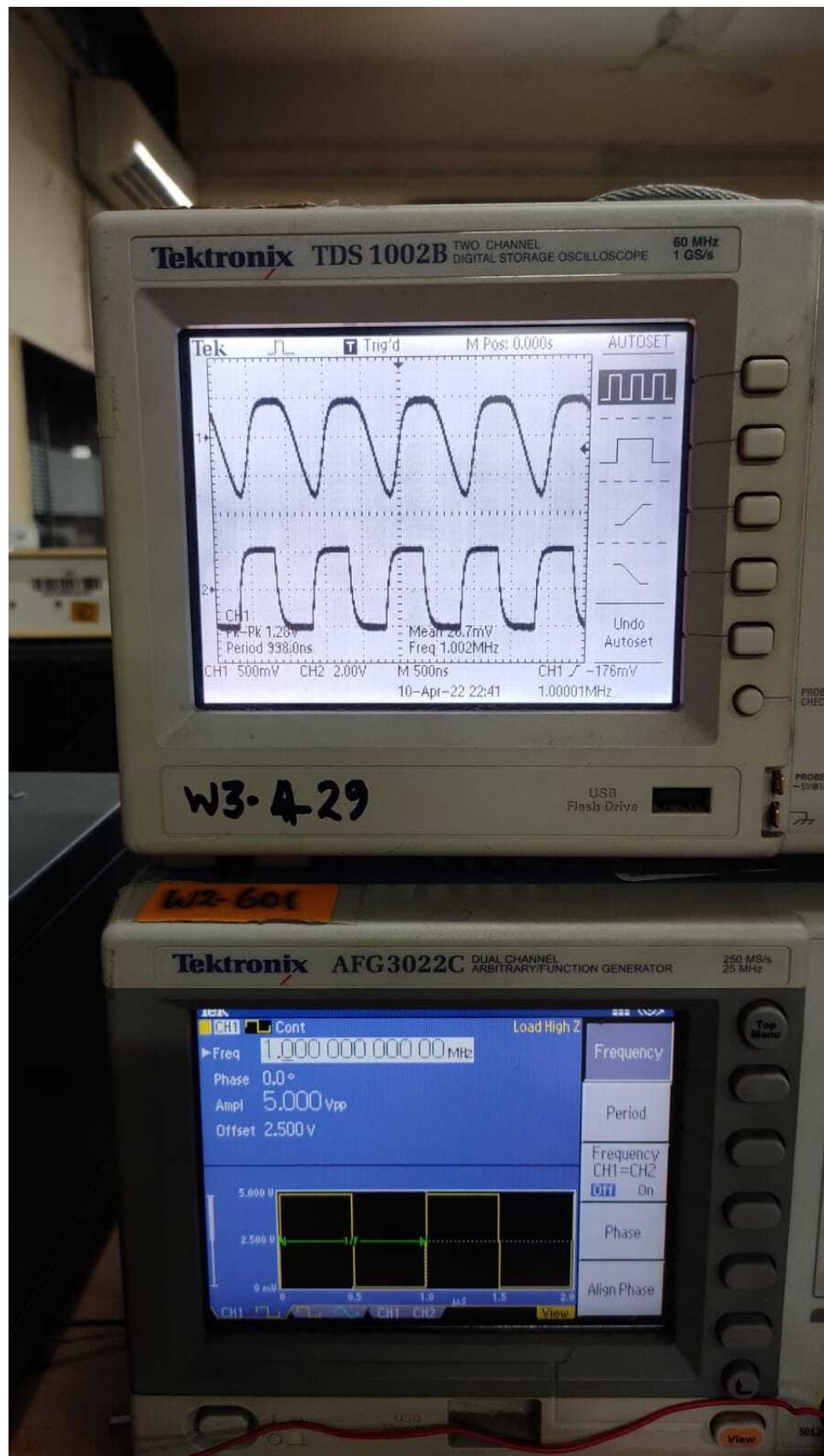
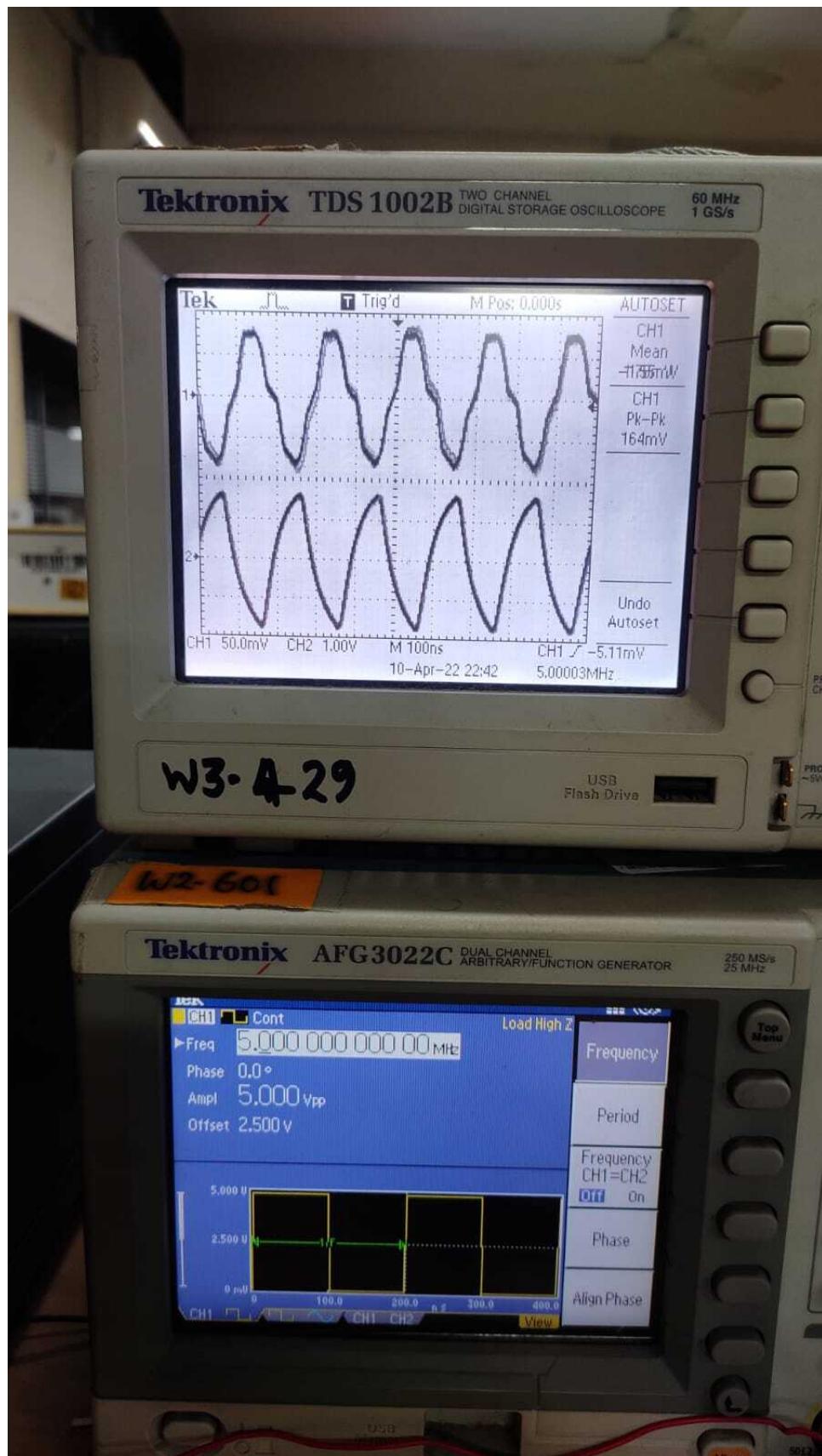
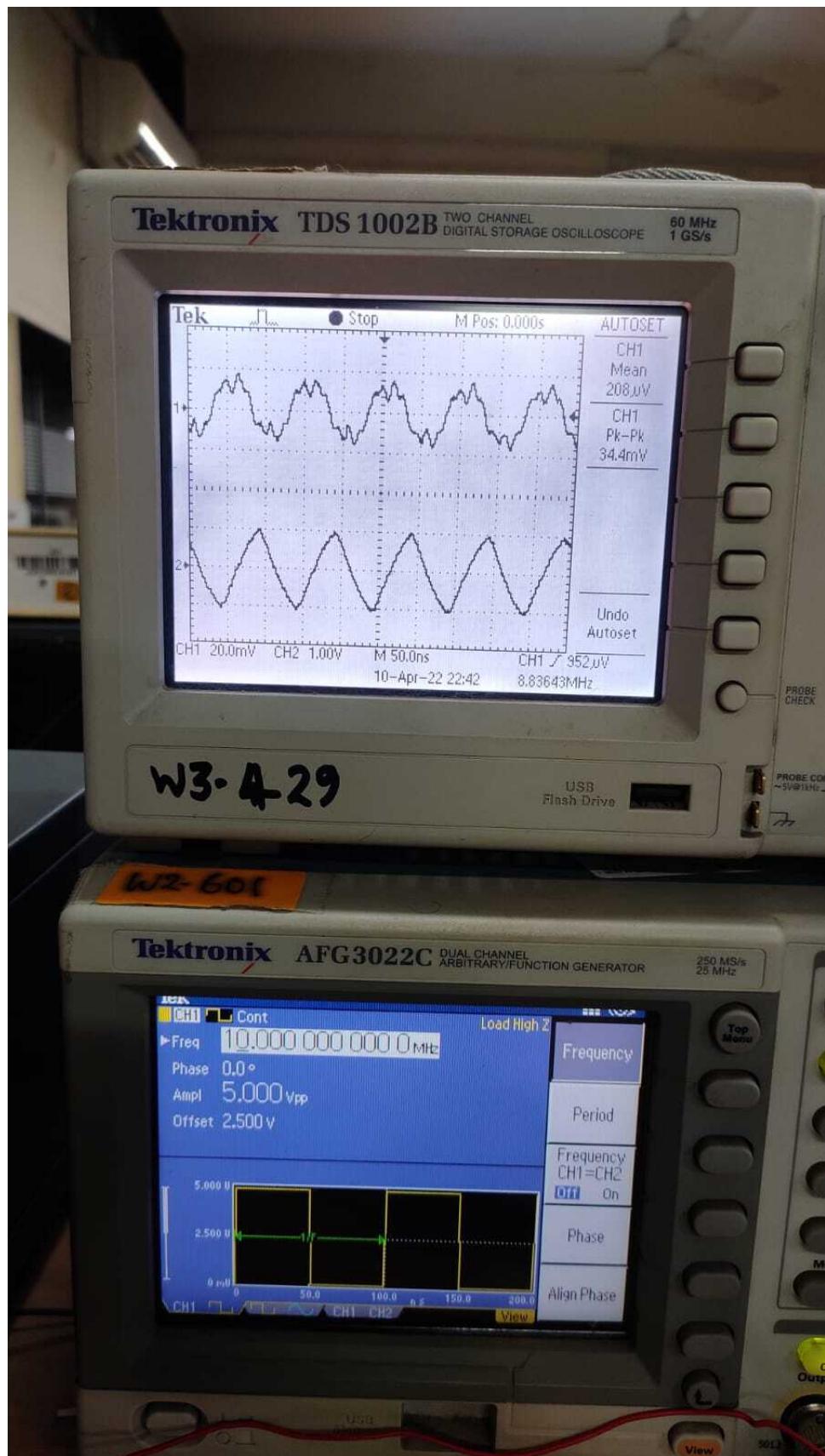
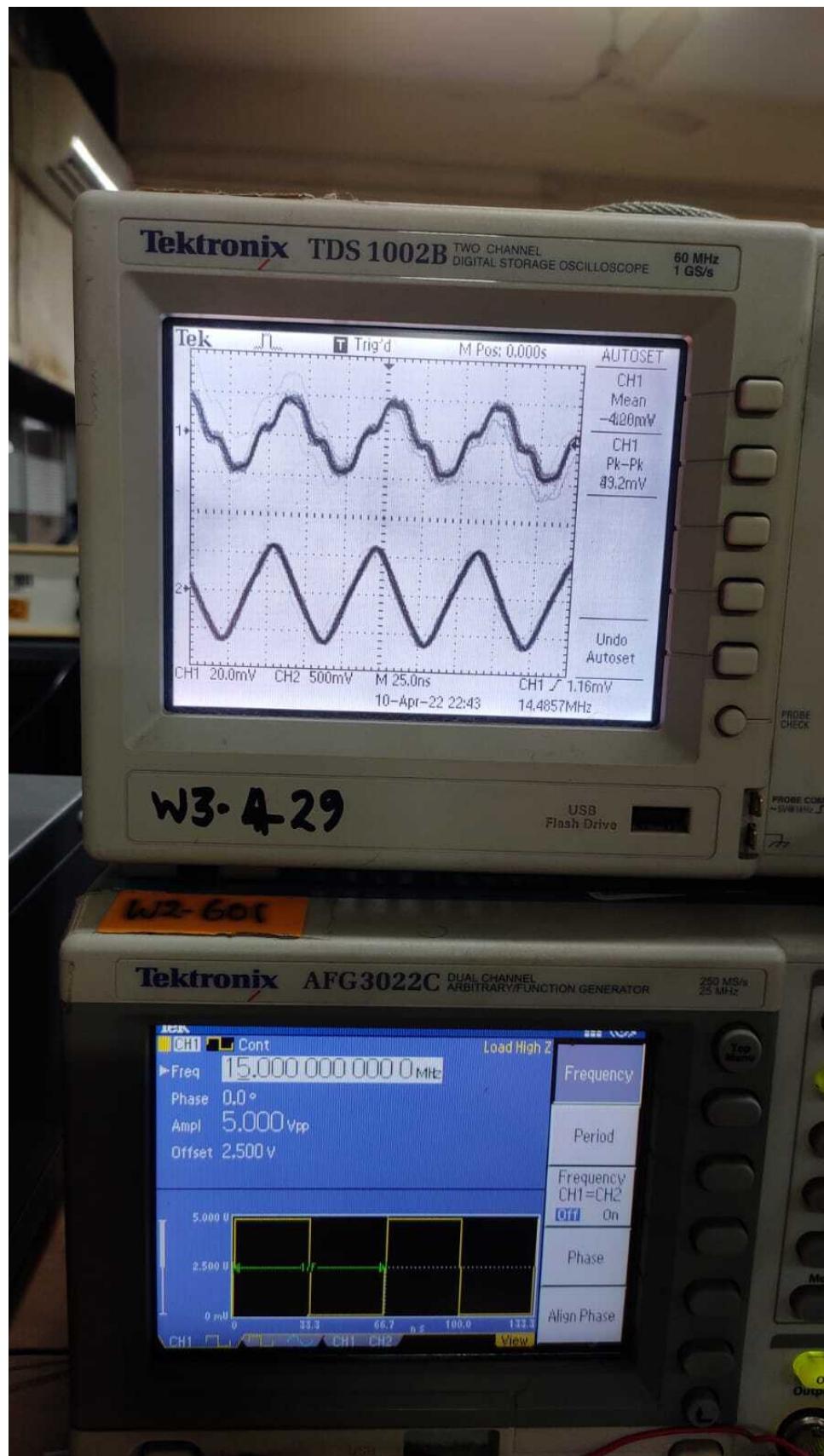


Figure 44: Input-Output waveforms for  $f_{clk}=500\text{KHz}$

Figure 45: Input-Output waveforms for  $f_{clk}=1\text{MHz}$

Figure 46: Input-Output waveforms for  $f_{clk}=5\text{MHz}$

Figure 47: Input-Output waveforms for  $f_{clk}=10\text{MHz}$

Figure 48: Input-Output waveforms for  $f_{clk}=15\text{MHz}$

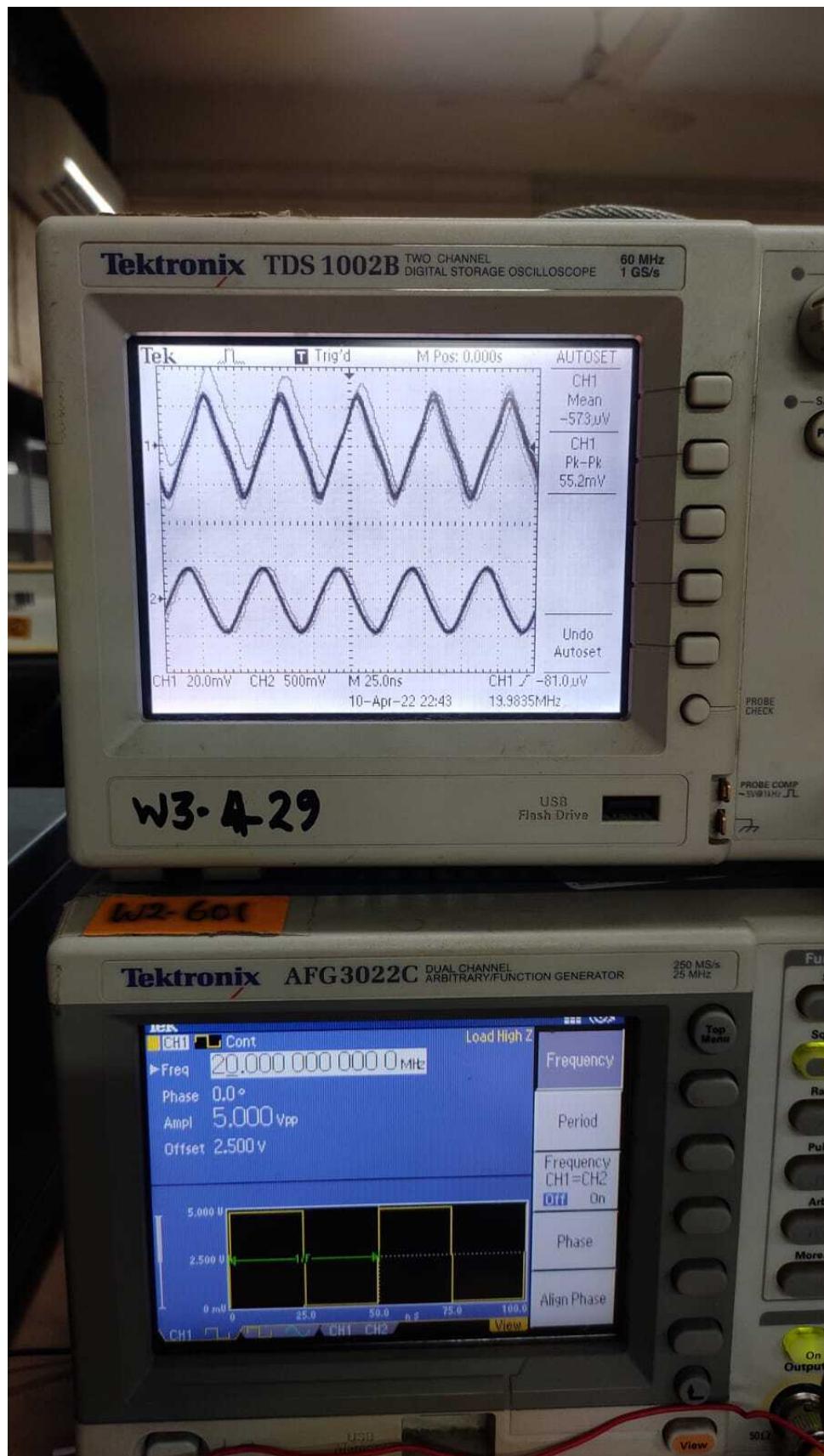


Figure 49: Input-Output waveforms for  $f_{clk}=20\text{MHz}$

We can see at very high frequencies that the input clock also becomes distorted and is not rectangular, this is due to the fact the breadboards have a large parasitic capacitance and

inductance which become comparable at high frequencies leading to distortion.

## 5 Appendix

### 5.1 NGSpice Code files

```

1 Receiver circuit
2
3 .include jfet_stg2.txt
4 .include ce_stg.txt
5
6 vddp vdd 0 dc 5V
7 Rd Vdd 1 1k
8 Id in 1 pulse(1n 10u 1n 1n 1n 1u 2u)
9
10 X1 in out1 vdd jfet_stg
11 X2 out1 out2 vdd ce_stg
12 X3 out2 out vdd ce_stg
13 Rf out in 100k
14 * Cf out in 22p
15 .tran 1n 8u
16 * .op
17 .control
18 run
19 plot V(out)
20 plot V(out1)
21 * plot V(in)
22 .endc
23 .end

```

Version 2 simulation in ngspice for 3dB bandwidth extraction

```

1 .include bfw11.txt
2 .include bc547.txt
3
4 Vp p 0 5
5 Vn n 0 -5
6 Vin in 0 dc 0 ac 1
7
8 J1 d1 in s1 BFW11
9 Rd1 p d1 680
10 Rs1 s1 n 470
11 Cs1 s1 n 2.2p
12
13 Q1 c1 d1 e1 BC547A
14 Rc1 p c1 470
15 Re1 e1 n 2.2k
16 Rcb1 c1 d1 10k
17 Ce1 e1 n 100u
18
19 Q2 c2 c1 e2 BC547A
20 Rc2 p c2 4.7k
21 Re2 e2 n 2.2k
22 Rcb2 c2 c1 10k
23 Ce2 e2 n 2.2p
24
25 Rf c2 in 480k
26 Cf c2 in 22p

```

```

27
28 .ac dec 10 1 300000k
29 .control
30 run
31 plot vdb(c2) xlog
32
33 .endc
34 .end

```

Listing 1: Version 2 simulation in ngspice

CE stage gain calculation in ngspice

```

1
2 .model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
3 + BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
4 + tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
5
6 Vc vcc 0 dc 12
7
8
9 Q out b e bc547a
10 Rcb out b 820k
11 Rc vcc out 1200
12 Re e 0 3300
13 * Vin b 0 dc 0
14 Ce e 0 100u
15 Vin b 0 sin(2.35 0.02 10k 0 0)
16 * .dc Vin 2 8 1
17 .tran 1u 0.6m 0.1u
18 .control
19 run
20 plot V(out)-avg(V(out)) V(b)-2.35
21 .endc
22 .end

```

Listing 2: CE stage gain calculation in ngspice

```

1 * Jfet DC nest sweep
2 .include bfw11.txt
3 Vdrain vdd 0 DC 5
4 Vgate g 0 DC -2
5 Vd vdd d dc 0
6 Vs s 0 dc 0
7 J1 d g s BFW11
8
9 .dc Vdrain 0 10 0.1 Vgate -2 0 0.5
10 .control
11 run
12 plot I(Vd) vs V(d)-V(s)
13 .end
14 .endc

```

Listing 3: JFET operating point calculation in ngspice

```

1 Trans-impedance Amplifier
2 .include jfet.txt
3 .include bc547.txt
4 Vdd vd 0 dc 5
5
6 vin input in jg 0

```

```

7 vin jg 0 dc 5 sin(0 10m 100k 0 0)
8
9 J1 jd jg js 2N3819
10 Rjs js 0 4k
11 Rjd vd jd 20k
12 Q1 js jd e1 bc547a
13 Rc1 vd c1 100k
14 Re1 e1 0 1k
15 Q2 out c1 e2 bc547a
16 Rc2 vd c2 10k
17 Re2 out 0 1k
18
19 * Rf out jg 480k
20 * Cf out jg 22n
21
22 .tran in 40u 1n
23 .control
24 run
25
26 * meas tran pp_out pp v(out)
27 * meas tran pp_in pp v(jg)
28 * meas tran pp_1 pp v(jd)
29 * meas tran pp_2 pp v(c1)
30 * let gain1 = pp_1/pp_in
31 * let gain2 = pp_2/pp_1
32 * let gain3 = pp_out/pp_2
33 * let gain = pp_out/pp_in
34 * print gain1, gain2, gain3, gain
35
36 meas tran pp_out pp v(out)
37 meas tran pp_in pp v(in)
38 let gain1 = pp_out/pp_in
39 print gain1
40 plot V(out) V(js) V(jg)
41 .endc
42 .end

```

Listing 4: Version 1 amplifier simulation

```

1 .subckt jfet_stg in out vdp
2
3 .include jfet2.txt
4 J1 out in s BFW10
5 Rd vdp out 2k
6 Rs s 0 470
7 C2 s 0 100u
8
9 .ends jfet_stg
10
11 .subckt ce_stg in out vdp
12
13 .model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
14 + BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
15 + tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
16
17 Q out b e bc547a
18 Rc vdp out 2k
19 Re e 0 1k
20 R1 vdp b 10k
21 R2 b 0 2.2k

```

```
22 Ce e 0 100u
23 C1 in b 10u
24
25 .ends ce_stg
26
27 Receiver circuit
28
29 .include jfet_stg2.txt
30 .include ce_stg.txt
31
32 vddp vdd 0 dc 5V
33 Rd Vdd 1 1k
34 Id in 1 pulse(1n 10u 1n 1n 1n 1u 2u)
35
36 X1 in out1 vdd jfet_stg
37 X2 out1 out2 vdd ce_stg
38 X3 out2 out vdd ce_stg
39 Rf out in 100k
40 * Cf out in 22p
41 .tran 1n 8u
42 * .op
43 .control
44 run
45 plot V(out)
46 plot V(out1)
47 * plot V(in)
48 .endc
49 .end
```