Performance Improvement of Patterned SOI over Traditonal SOI MOSFETs

EE 724 Nanoelectronics

by

GROUP - 7

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Chapter 1

A Review

1.1 SOI MOSFET vs Bulk MOSFET

MOSFET technologies form the basis of modern computing which makes the optimization and improvement of their performance an extremely happening research topic. In contrast to a conventional MOSFET, the presence of a Buried oxide (BOX) layer enhances the characterization of the MOSFET and speeds up its performance. This technology is known as Silicon-on-insulator MOSFET or SOI MOSFET.
Short channel effect (SCE) in a Silicon-on-insulator (SOI) MOSFET are significantly lower than the conventional MOSFETs and they align rather well with the theoretical calculations. The benefits of a SOI MOSFET mainly arise from the dependency on film thickness, body and substrate biases. This dependency enables a superior control of drain bias, carrier velocity saturation, channel length modulation and its effect on out conductance, as well as devices degradation due to the channel effect immunity to SOI MOSFETs. The use of SOI MOSFETs in VLSI circuits allows for added flexibility compared to the bulk MOSFET design. The short body effect in the SOI MOSFET can be split into various instances, which are the Threshold Voltage Reduction, Drain-Induced Conductivity Enchantment (DICE) and Velocity Saturation and Channel-Length Modulation
Another advantage of the SOI MOSFET over their bulk silicon counterpart is its ability to operate at very high-speed switching frequencies due to lower parasitic capacitances. In order to increase the drive current available from the transistors the threshold voltage can be set to the lowest value allowing one to obtain the highest possible speed. This enables the transistors to switch off more easily and reduces the slope of the sub threshold characteristics. This phenomenon can be demonstrated by how the change in gate voltage required reduces the drain current by an

order of magnitude. The Sub-threshold voltage swing of SOI MOSFET devices has been observed to be lower than the Bulk MOSFET devices. The low sub-threshold voltage swing is desired in order to attain faster switching speed. This makes it particularly important since the slope of the subthreshold is regarded as a crucial figure of merit for a MOSFET device.

1.2 Simulation Results and Analysis

First we study BULK MOSFET's parameters and analyse various parameters.

1.2.1 BULK MOSFET

The device parameters were set as follows:
Gate length (Lg): 22 nm
Spacer length (Lsp): 14 nm
Gate oxide thickness (Tox): 0.6 nm
HighK oxide thickness (THF): 2 nm
Metal Gate thickness (TMetal): 5 nm

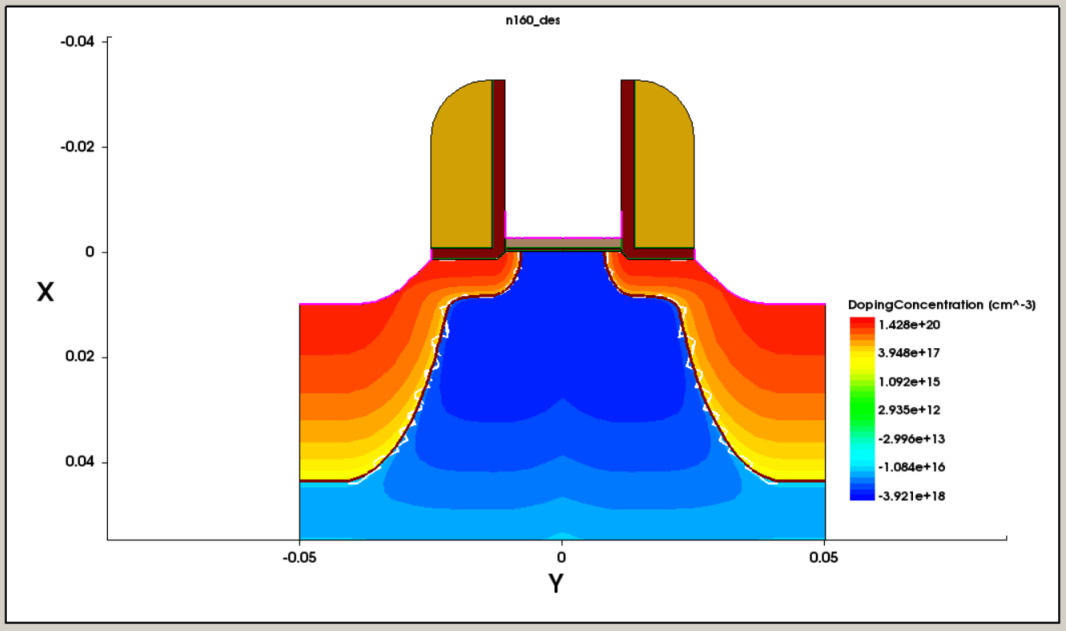

Figure 1.1: Typical BULK MOS structure

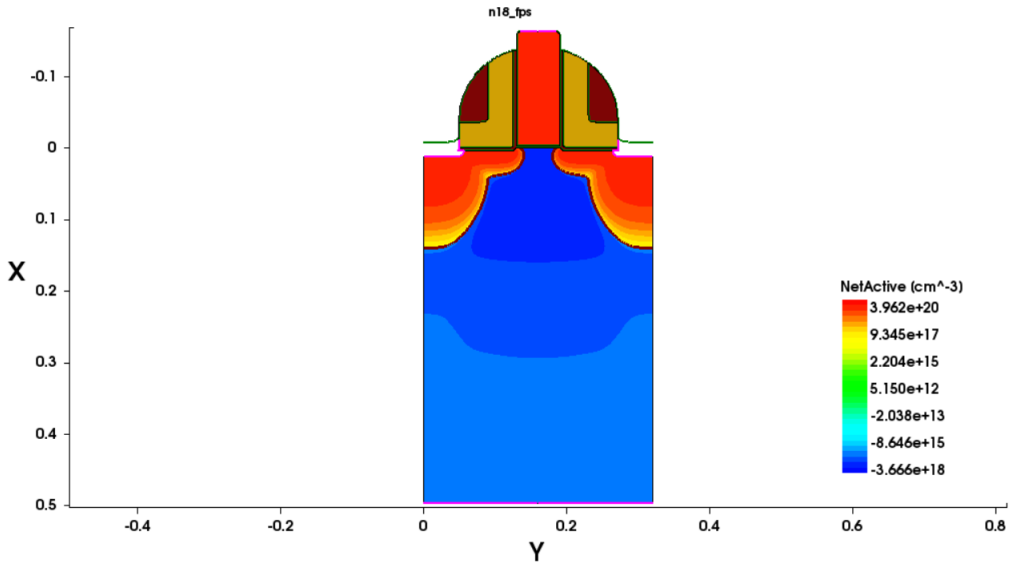

Figure 1.2: Bulk MOSFET

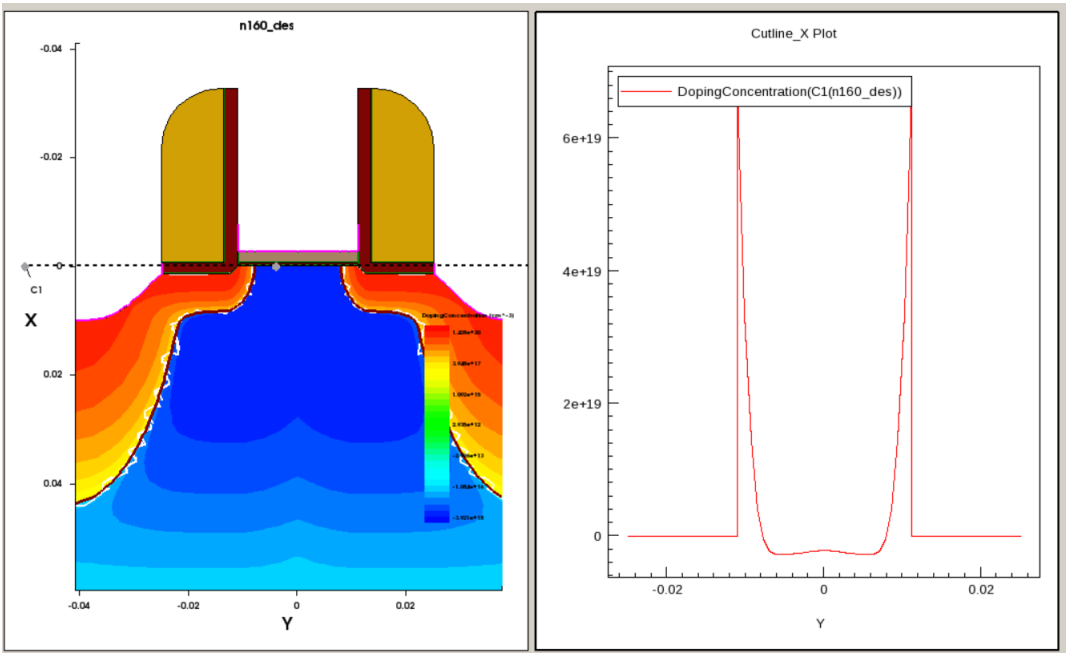

Figure 1.3: Doping profile Bulk MOSFET

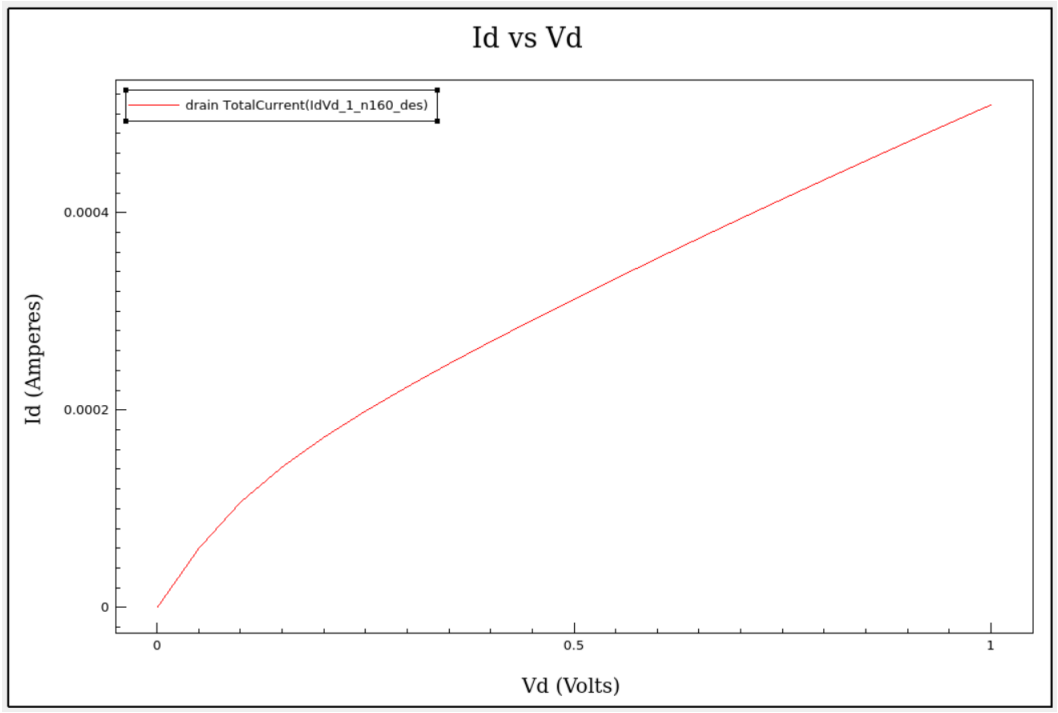

Figure 1.4: Id v/s Vd curve for Bulk MOS

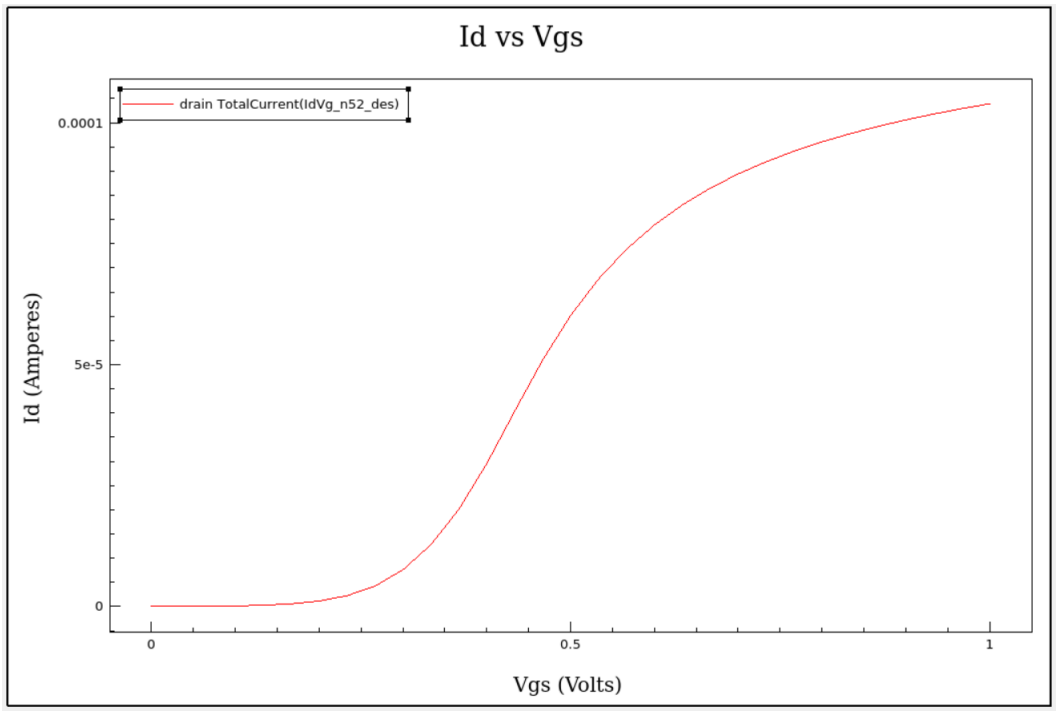

Figure 1.5: Id v/s Vgs curve for Bulk MOS

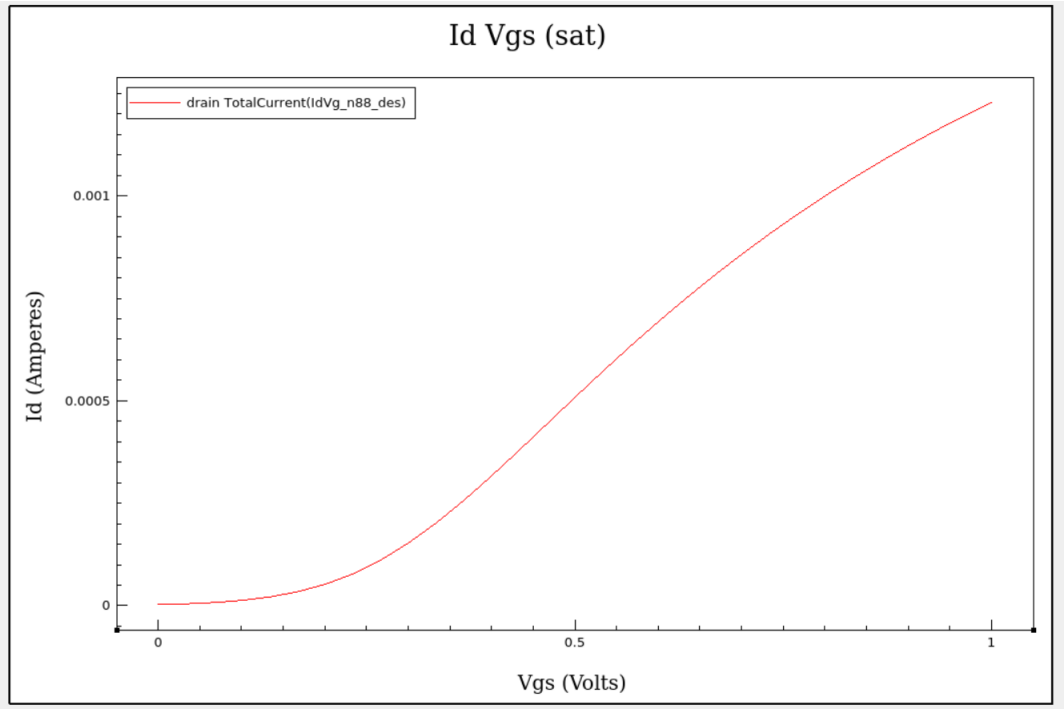

Figure 1.6: Id v/s Vgs curve for Bulk MOS in saturation

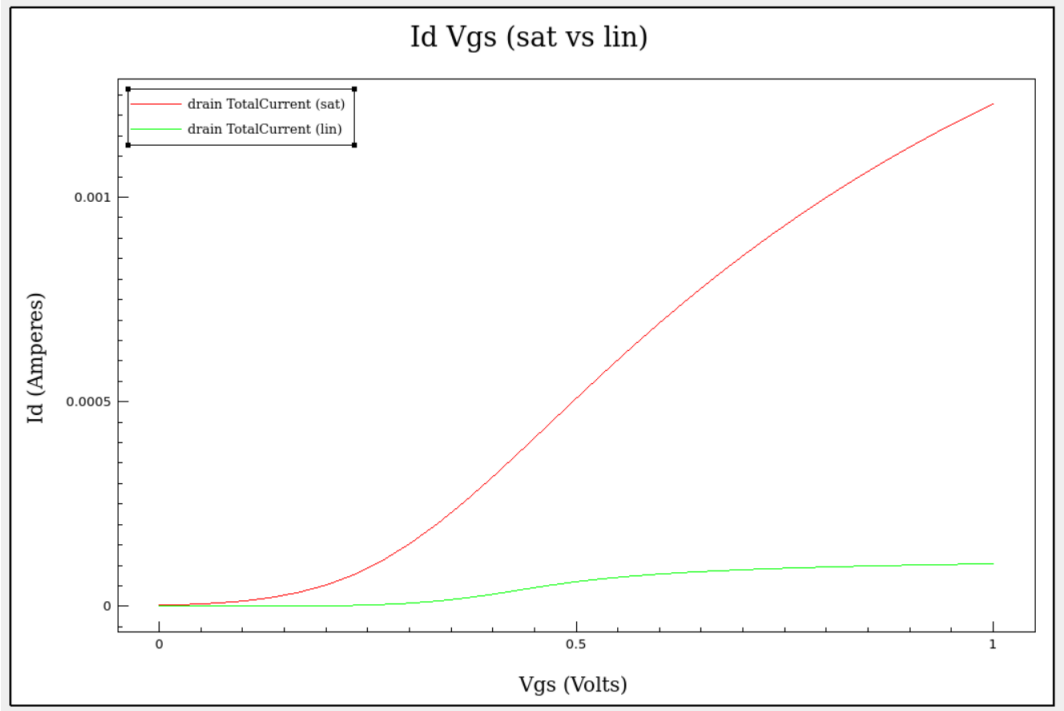

Figure 1.7: Id v/s Vgs curve for Bulk MOS (Saturation v/s Linear)

Chapter 2

PD-SOI vs FD-SOI

Silicon-on-insulator (SOI) MOSFETs are mainly available in two "flavours," Fully Depleted (FD) and Partially Depleted (PD). The names correspond to the thickness of silicon in the active region. The techniques for fabrication stay more or less the same since they share a common substrate material except that the PD material has a silicon thickness greater than about 0.15 µm. The higher thickness also makes it easier to manufacture them. PD devices display the 'kink effect' as opposed to bulk or FD-SOI MOSFETs. It has the beneficial effect of higher drive current far digital design. PD-SO1 also displays "history dependence", (different switching rates on subsequent switching edges). "pass-gate leakage" can occur in both PD and FD-SOI.

The PD-SO1 can be seen as an evolutionary process development advance from the bulk MOSFET, produced by adding just the oxide layer. In most analog and transmission-gate logic applications, floating body effects aren't allowable. Additionally, variation in the floating body voltage causes uncertainty in the gate-source threshold voltage which reduces the noise margins for dynamic and memory circuits. In these cases, a body contact can be added to PD-SOI which is something that's not possible in the case of an FD-SOI since a resistive body region does not exist for most operating conditions.

The primary benefit of the FD-SOI comes from its ability to minimize floating body effects that are apparent in case of the PD-SOI. The absence of body region that can be charged circumvents the problem of floating body effects and preclude any history or kink effects. Although, as mentioned before, the FD-SOI is more difficult to fabricate, and it is also difficult to control its threshold voltage. Devices on FD-SOI display a steeper sub-threshold slope, with low parasitic capacitances which is a crucial characteristic of SOI MOSFETs making them appropriate for

low-voltage, low-power applications. FD-SOIs also have the advantage of reduced power consumption compared to PD SOl and bulk MOSFETs.

2.1 Evaluation Metrics

Here we compare a few key aspects to compare the PD-SOI and FD-SOI MOSFETS

Response Characteristic	Bulk MOS	PD-SOI	FD-SOI
$Vtgm$	0.310	0.346	0.279
$VtiLin$	0.270	0.261	0.387
$IdLin$	103.9µA	48.67µA	37.29µA
$SSLin$	101.43	96.29	81.358
$gmLin$	327.9µmho	1.73mmho	76.8µmho
$IdSat$	1.23mA	4.87mA	100.1µA
I_{off}	2.6µA	605.4nA	5.09nA
$VtiSat$	0.034	0.111	0.359
$SSsat$	142.82	126.55	84.928
$gmSat$	1.93mmho	8.17mmho	284.9µmho
Ron	-	-	58.67kΩ

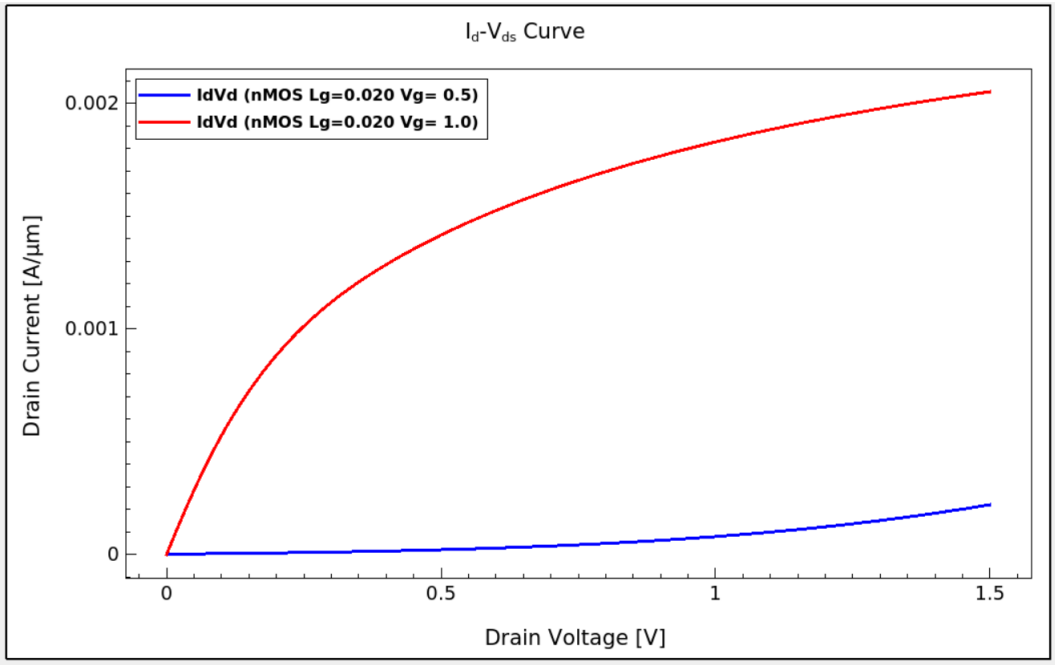

Figure 2.1: Id v/s Vd curve for PD-SOI

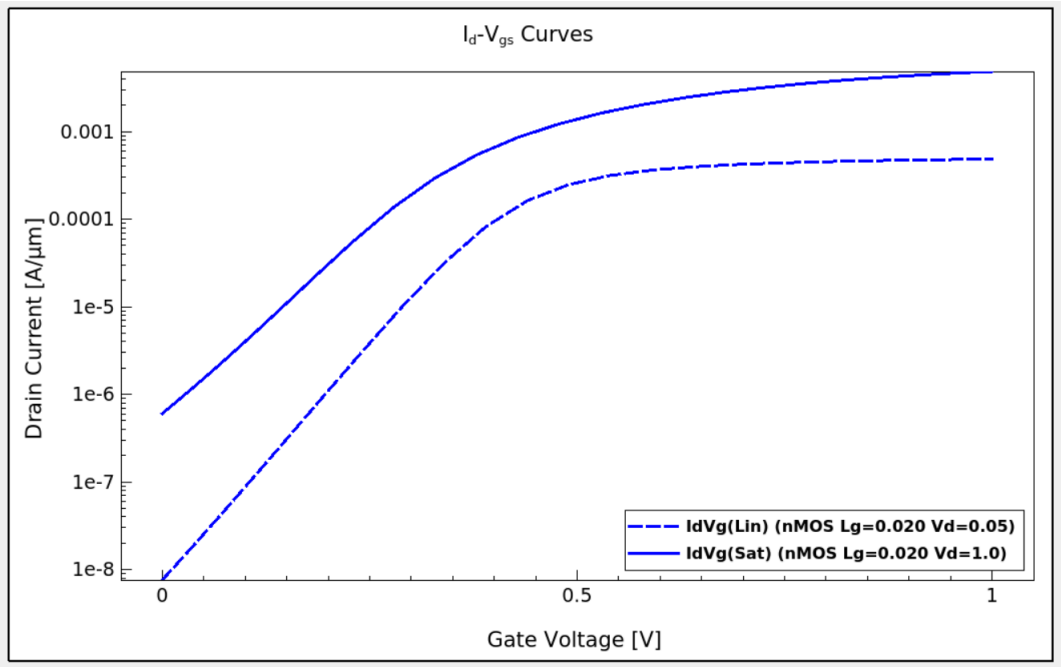

Figure 2.2: Id v/s Vgs curve for PD-SOI (Saturation v/s Linear)

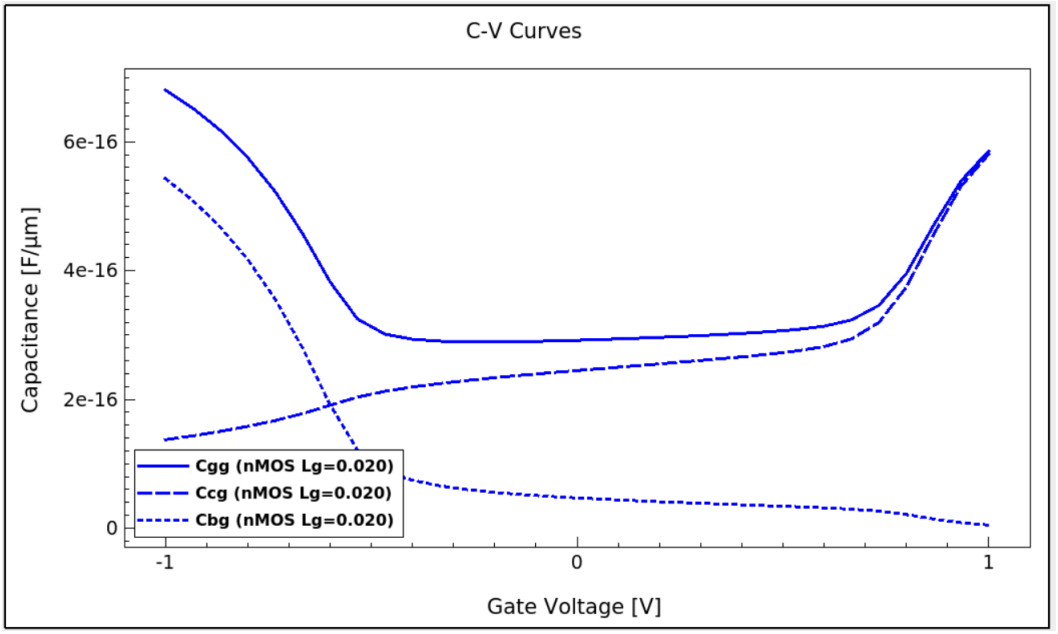

Figure 2.3: Capacitance v/s Vg curve for PD-SOI

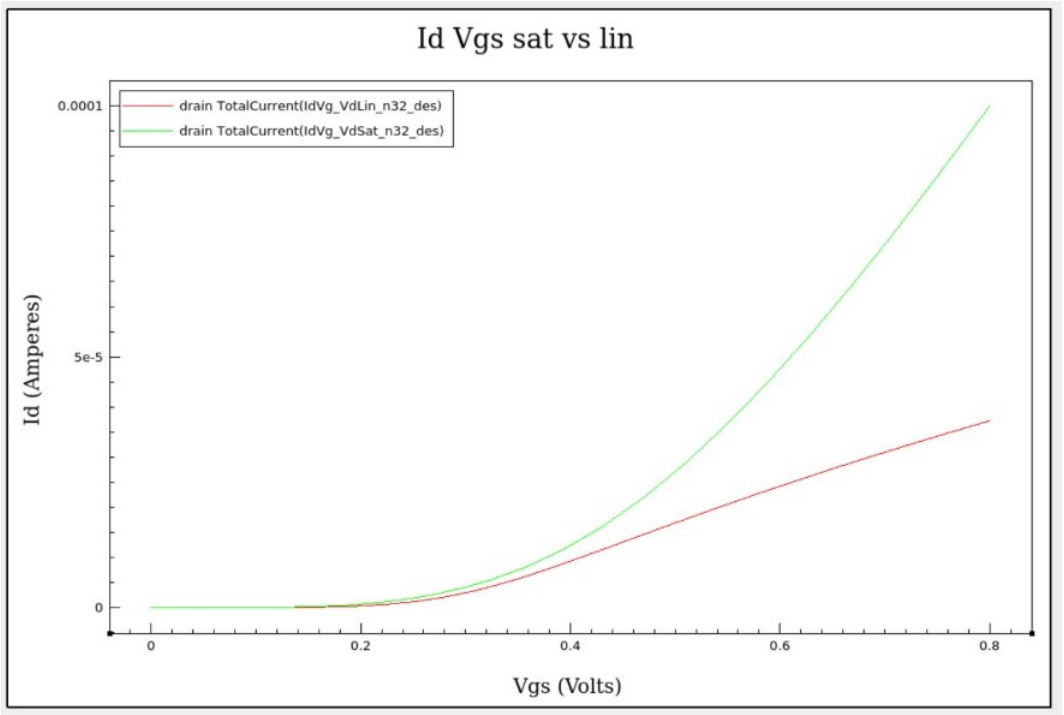

Figure 2.4: Id v/s Vgs curve for FD-SOI (Saturation v/s Linear)

Chapter 3

Patterned SOI MOSFET

As compared to an SOI MOSFET, a patterned SOI MOSFET has a layer of silicon between the buried oxide layer. The length of this silicon layer can be varied, in our analysis we kept the silicon layer length equal to the gate length. The figure below shows doping profile and depletion region marking on the patterned SOI MOSFET section.

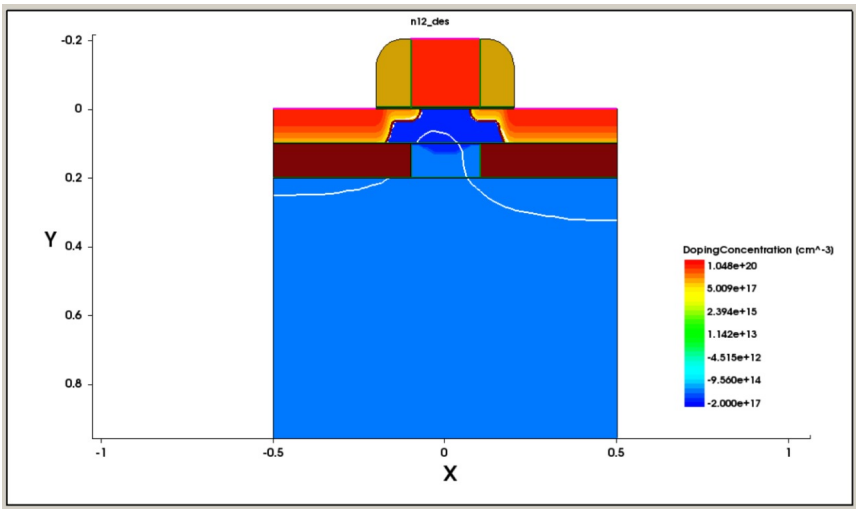

Figure 3.1: Patterned SOI MOSFET doping profile, with depletion layer

As compared to the patterned SOI MOSFET, the doping profile, structure and deletion region of an SOI MOSFET is shown below.

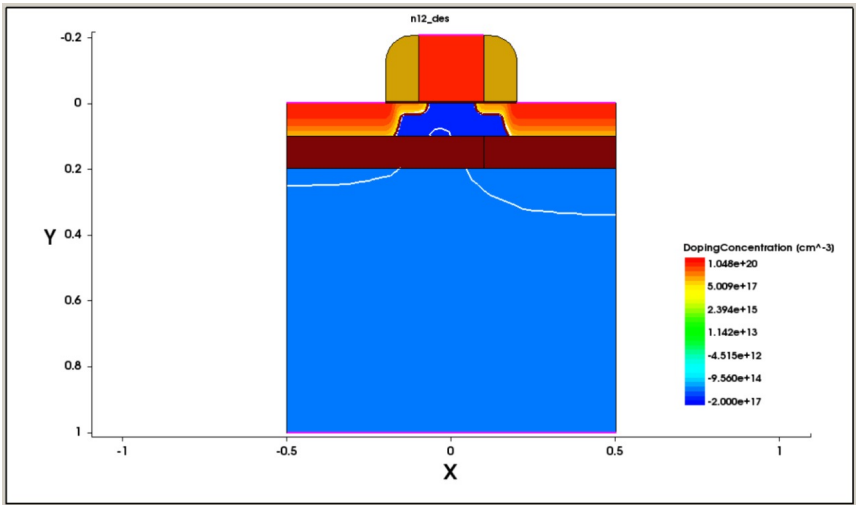

Figure 3.2: SOI MOSFET doping profile, with depletion layer

Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. Impact ionization is an efficient method to generate electron–hole pairs. In N-channel MOSFET, the electrons are collected at the drain and the holes are retained in the body by a negative back-gate voltage. Writing "1" is fast but requires a high drain voltage and consumes power.

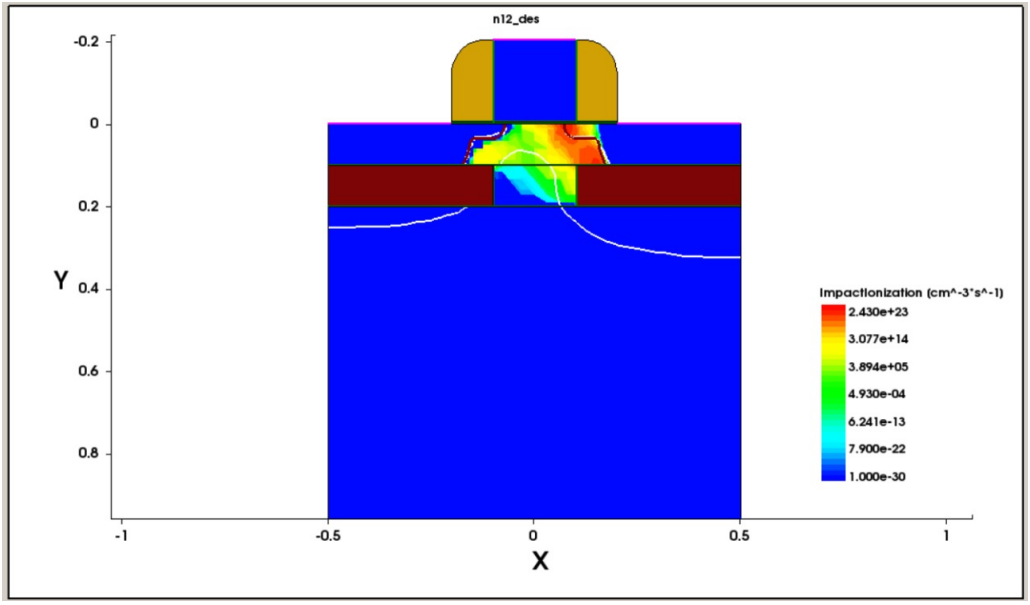

Figure 3.3: Patterned SOI MOSFET Impact Ionization in Id Vg sweep

The kink effect is caused by the injection of holes into the floating substrate of an SO1 MOSFET. These holes are generated by impact ionization in the high-electric field region near the drain. Once generated. the holes migrate towards the region where the potential is lowest, i.e., towards the floating substrate.

Larger substrate current is observed for the SOI transistor at high gate bias. The impact-ionization rate of the SOI MOSFET is larger than the bulk/patterned SOI counterpart at high gate bias.

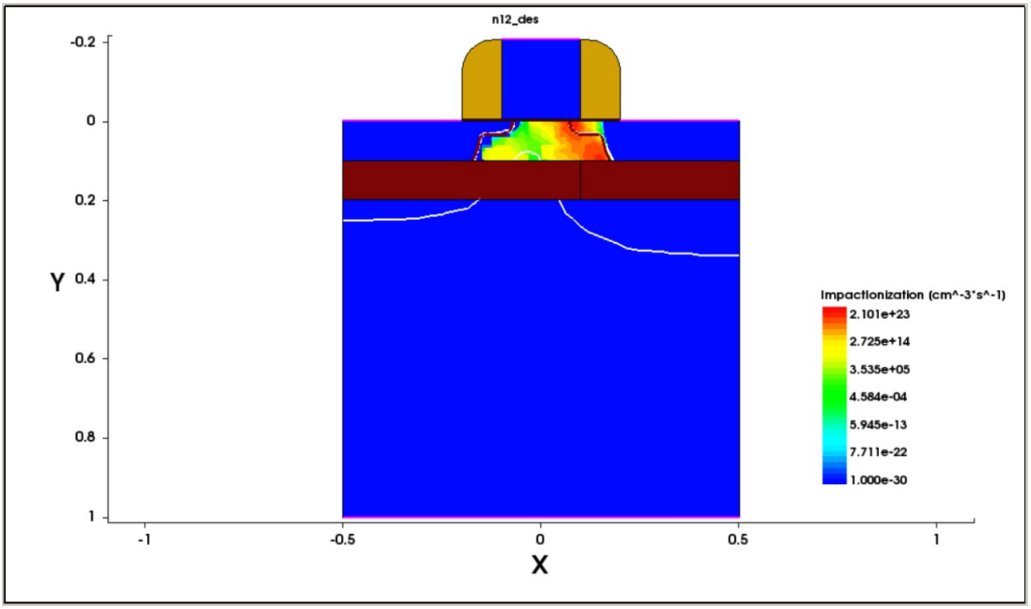

Figure 3.4: SOI MOSFET Impact Ionization in Id Vg sweep

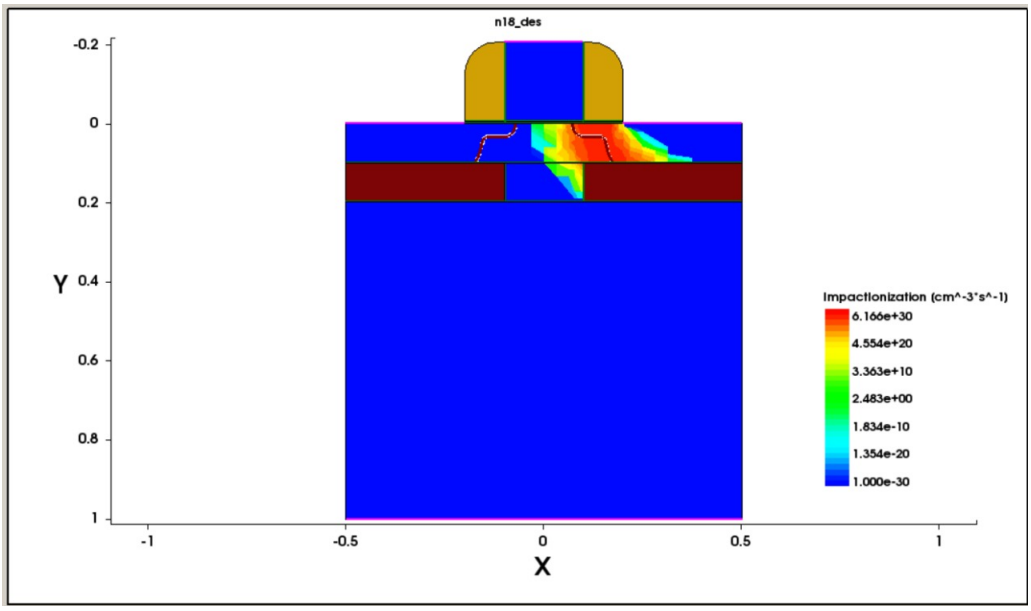

Figure 3.5: Patterned SOI MOSFET Impact Ionization in Id Vd sweep

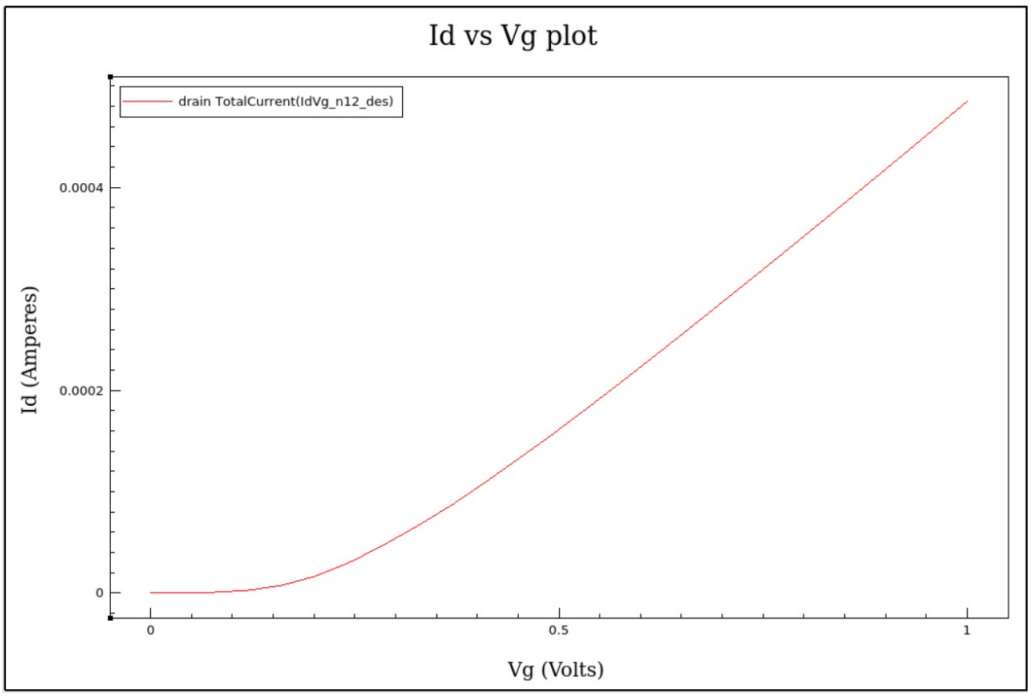

Figure 3.6: Id v/s Vgs curve for Pattered SOI mosfet

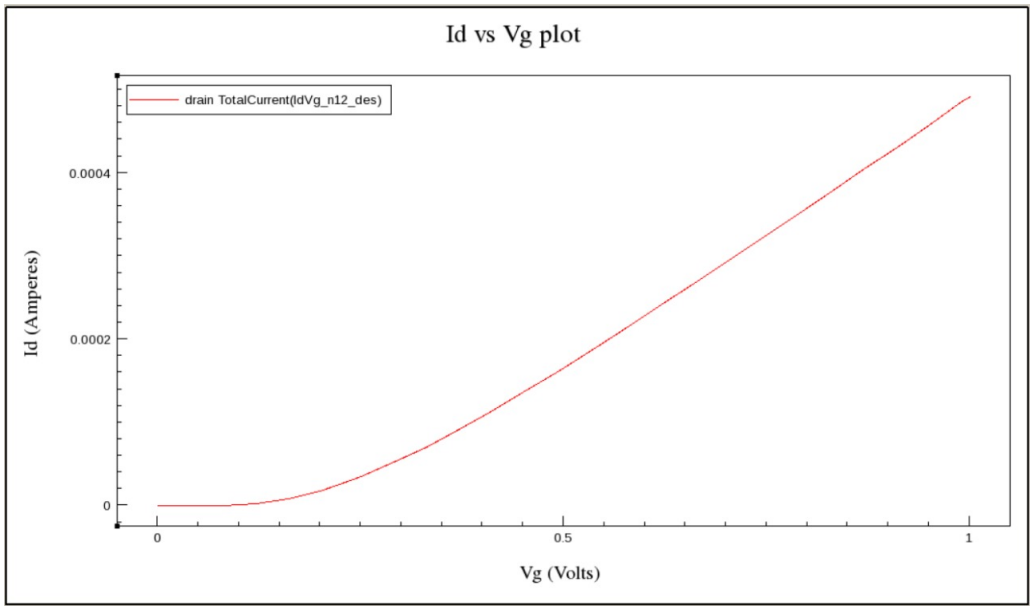

Figure 3.7: Id v/s Vgs curve for SOI mosfet

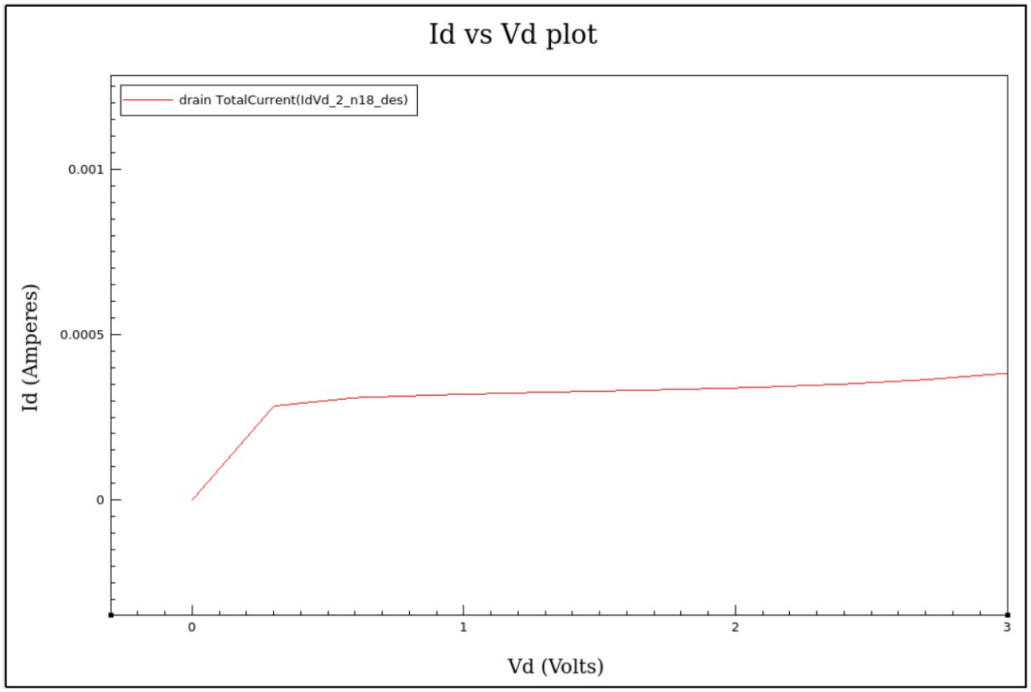

Figure 3.8: Id v/s Vd curve for Pattered SOI mosfet

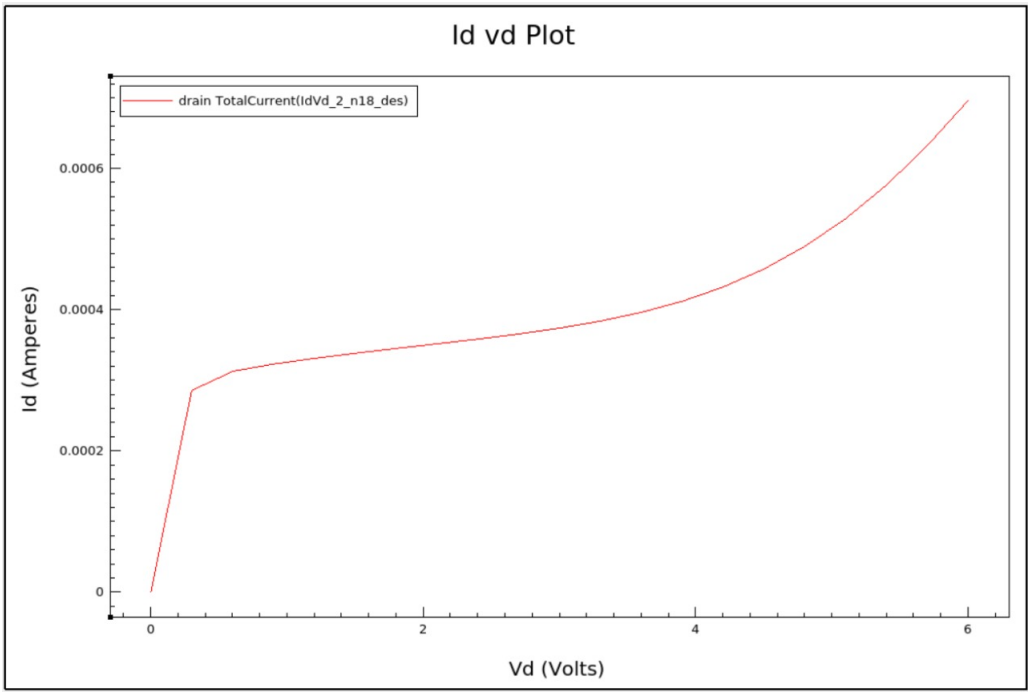

Figure 3.9: Id v/s Vd curve for SOI mosfet showing the kink effect

We observe that post 3-4V Vd, kink effect is observed in SOI mosfet.

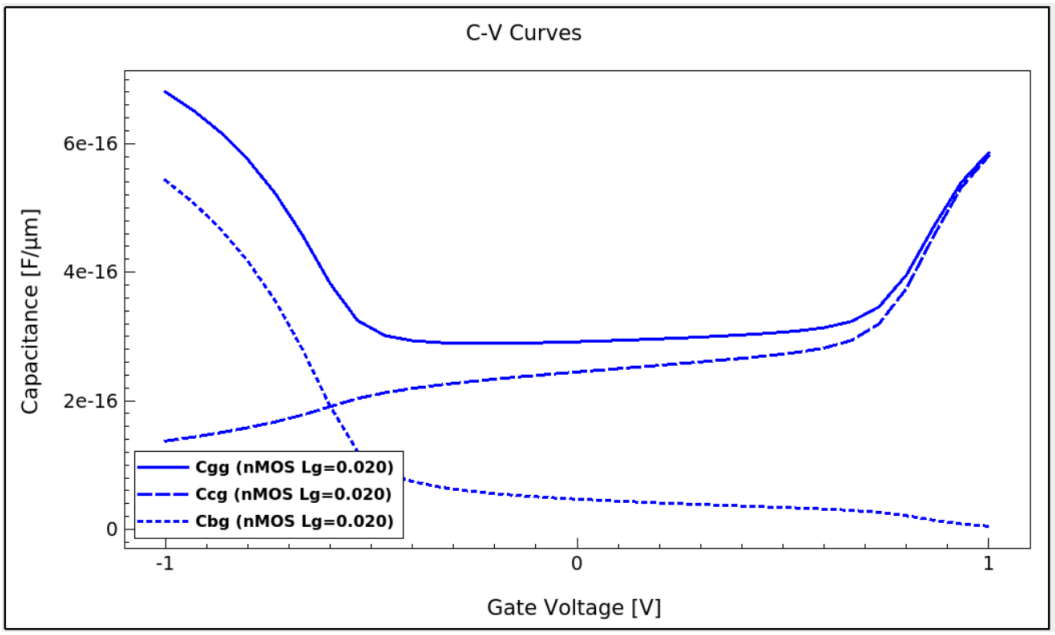

Figure 3.10: Capacitance v/s Vg curve for SOI

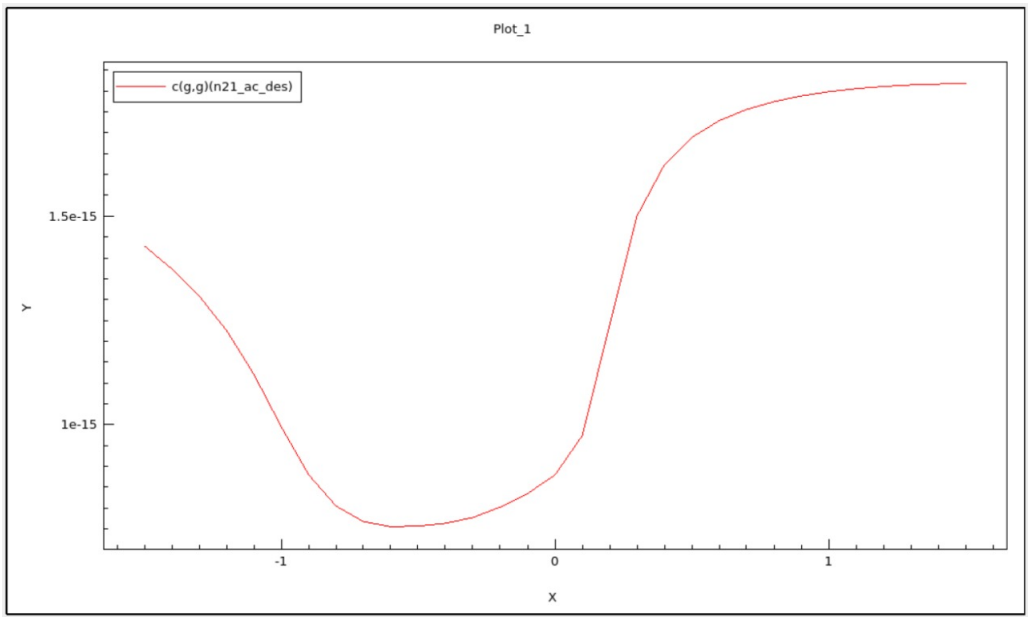

Figure 3.11: Capacitance v/s Vg curve for Patterned SOI

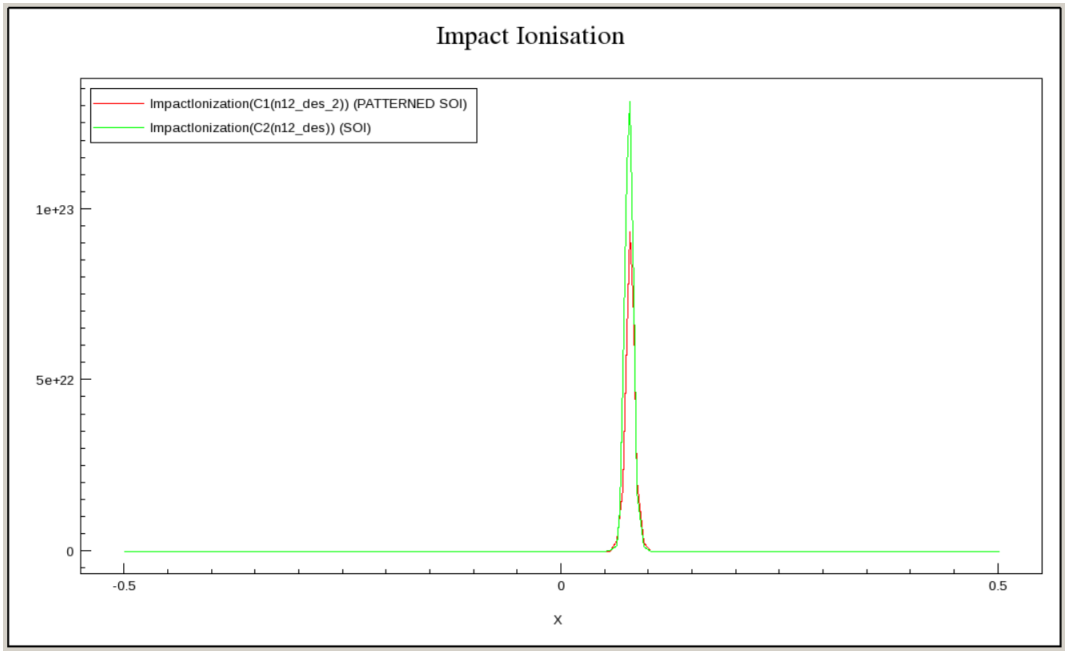

Figure 3.12: Impact Ionisation in SOI vs Patterned SOI for same Ycut

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Here we compare a few key aspects to compare the Bulk, FD-SOI and Patterned MOSFETS

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$SSsat$	142.82	74.66	84.928
$gmSat$	1.93mmho	677.4µmho	284.9µmho
Ron	-	16.7kΩ	58.67kΩ

3.2 Acknowledgements

Thanks to prof. Udayan Ganguly for such a wonderful course and introducing projects in which we actually learnt a lot. Thanks to mentor Mr. Shubham Patil for helping throughout the process of learning and experimenting in the project. Also, we would like to thank our fellow colleague Mr. Omkar Phadke for helping unconditionally during simulations.

3.3 Bibliography

1) Su, P., Goto, K. I., Sugii, T., Hu, C-M. (2002). Enhanced substrate current in SOI MOSFETs. IEEE Electron Device Letters, 23(5), 282-284. https://doi.org/10.1109/55.998877