Jay Sonawane

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Research Interest

Nanoelectronics- Physics of Nanoscale devices, Device Modelling, Characterization and Fabrication

Education

Indian Institute of Technology Bombay *Jul 2019 – Aug 2024 (expected)*

Electrical Engineering
Dual Degree (B.Tech + M.Tech)
Specialization – Integrated Circuits and Systems, CPI – 8.21

Publications

1. **Jay Sonawane**, Shubham Patil, Sandip Lashkare, Veeresh Deshpande, Udayan Ganguly, *"Design Space and Variability Analysis of SOI MOSFET for Ultra-Low Power BTBT Neuron",* (TED, to be submitted)
2. Shubham Patil, Abhishek Kadam, **Jay Sonawane**, Ajay kumar Singh, Nihar Ranjan Mohapatra, Veeresh Deshpande, and Udayan Ganguly, *"Reliability of Tunneling regime for Silicon on Insulator-based Neuron"* (Under preparation,TED,to be submitted)
3. Nishant Saurabh*, Shubham Patil*, Paritosh Meher, **Jay Sonawane**, Sandeep Kumar, Bhavesh Kumar Kamaliya, Sandip Lashkare, Rakesh G. Mote, Apurba Laha, Veeresh Deshpande, Udayan Ganguly, *"Structural and Electrical Characterization of Phase Evolution in Epitaxial Gd2O3 due to Anneal Temperature for Silicon on Insulator (SOI) Application"*, (APL, to be submitted)

Research Experience

BEOL compatible Indium Tin Oxide Transistor and HfO2 RRAM *Mar 2022 – Present*
Guide: Prof. Udayan Ganguly. Prof Veeresh Deshpande, MeLoDe Labs, IIT Bombay

- Fabricating back-end of the line (BEOL) compatible HfO2 based RRAM for **3D monolithic integration**
- Modelling dual-gated, 3nm Indium Tin Oxide channel transistor in Sentaurus TCAD and to demonstrate high drive currents (mA/μm at L_G = 60 nm
- Developing an empirical mobility model for accurate thin film modeling in TCAD to reproduce dependence of Hall mobility with respect to carrier-electron density
- Engineering fabrication process flow for BEOL fabrication of ITO MOSFET using blanket film on blanket surface using low cost RF sputtering tool optimized using TCAD experiments

SOI Device Optimisation for Operation in BTBT Regime [Report] *May 2022 – Present*
Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay
(Received **Undergraduate Research Award (URA01)** in recognition of excellent contribution to preliminary activity leading to research and developmental exposure)

- Modelled a 32nm PDSOI MOSFET for operation in **band to band tunneling** (BTBT) regime in order to exercise benefits of **lower variability**, and an **ultra-low power** current source device as compared to ON and (subthreshold) SS operation
- **Calibrated** experimental results (characterized at IIT Bombay Nanofabrication facility) with simulation results of **GF32nm PDSOI MOSFET** (fabricated at GlobalFoundries) using **Sentaurus TCAD**
- Investigated tunneling physics and demonstrated trap assisted tunneling and direct band-to-band tunneling dominant regions in BTBT regime using Hurkx and Nonlocal path models respectively
- Designed a **device design space** to achieve lower BTBT current which translates to **enhanced energy efficiency** of the integrator, **lower spiking frequency** of the neuron, and lower area of body capacitor (**lower device area**)
- Obtained the effect of variability (random dopant fluctuations and oxide thickness variation and channel-oxide traps) and investigated sensitivity of BTBT, SS and ON currents to process parameters
- Performed stress tests to check the reliability of BTBT operation in comparison to SS and ON operation

Reliability and Variability analysis of SRAM and Sense Amplifier circuits *May 2023 – Present*
Undergraduate Research Project – Guide: Prof. Souvik Mahapatra

- Integrating SRAM and sense amplifier circuit with the Circuit Aging Reliability Analysis Tool (CARAT)
- Performed noise margin (SNM) and flip time (FT) analysis for SRAM for varying activity of NBTI in Hspice
- Literature surveyed analysis of SRAM metrics for data dependent BTI degradation and process variability

Performance comparison of Patterned SOI over traditional SOI MOSFETs [Report] *Mar 2022 – Present*
Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay

- Designed a novel SOI MOSFET characterised by patterning rare buried oxide (Gd2O3) below the silicon channel
- Simulated the structure and **characterized** the behavior of traditional and patterned SOI MOSFET in Sentaurus TCAD
- Compared bulk, traditional SOI and patterned SOI on the basis of performance parameters in ON and SS operation

Reliability of Cryo-CMOS based circuits *Aug – Nov 2021*
Undergraduate Research Project – Guide: Prof. Souvik Mahapatra

- Studied a compact model used to partition the measured threshold voltage shift kinetics for different stresses into **Hot Carrier Degradation**, **Bias Temperature Instability** and electron/hole trapping subcomponents at low temperature
- Conducted ngspice simulations for **ring oscillator analysis** to calibrate the compact HCD-BTI model for circuit aging

Nanoelectronics Projects

Resonant Tunneling Diodes: NEGF-Poisson based consistent simulation *Mar – Apr 2023*
Course: Quantum Transport – Instructor: Prof. Bhaskaran Murlidharan

- Studied the **Tsu-Isaki formulation** of resonant tunneling current for generic double barrier heterostructures (RTDs)
- Simulated tunneling probability using the **Breit-Wigner function** for varying quantum well and barrier parameters
- Modelled a resonant tunneling diode heterostructure using a self consistent **NEGF-Poisson formulation** in MATLAB to study the impact of variation in quantum well and barrier parameters on transmission coefficient and I-V characteristics

Modified WKB based analytic model for direct tunneling current in MOS devices *Mar – Apr 2022*
Course: Physics of Transistors – Instructor: Prof. Souvik Mahapatra

- Studied modelling of the low-field roll-off in the current resulting from proper **modelling** of the **field dependencies** of the sheet charge, electron impact frequency on the interface, and tunneling probability
- Reproduced the results using a modified WKB approach consisting of the usual WKB tunneling probability valid for smoothly varying potentials, and a reflection coefficient for **correcting reflections** from potential discontinuities

Improving Photoluminescence in InAs Surface Quantum Dots [Report] *Mar – Apr 2021*
Course: Growth and Characterization of Nanoelectronic Materials – Instructor: Prof. S. Chakrabarti

- Demonstrated the advantages of incorporating **antimony** (Sb) as a **surfactant** into a strained InGaAs quantum well
- Simulated InAs SQDs in NextNano ++ software to observe the effects of **extended planar growth** and dot formation
- Schrutinised the effect of Sb to delay three-dimensional (3D) growth in InAs surface quantum dots to render **improvement in carrier confinement**, lower energy band gap and **achieve longer emission wavelength**

Industrial Experience

Atomberg Technologies *May – Jul 2022*
Research and Development Intern – Mentor: Gaurav Gupta, Yash Sanghvi *Pune, India*

- Integrated **PIR (pyro-electric IR)** sensors with **BLDC** smart fans for motion/presence detection based operation
- Tested and integrated Panasonic and Holtek PIR sensor modules on **STM8s** in Renesa fans and **esp32c3** based fans
- Developed firmware register transfer level (RTL) code for with GV4 and GV5 series of boards and tested the installation

Carnot Technologies *May – Jul 2021*
Data Science Intern – Mentor: Yash Sanghvi *Mumbai, (Work from Home)*

- Programmed a script that provides **time series NDVI** files using **Sentinel-hub API** and latitude-longitude boundary
- Statistically analysed sugarcane crop **NDVI** progression for around **200+** farms around the country for one crop cycle
- Developed a model using **Random Forest** regressor to predict sugar content in crop using ten **vegetation indices**

Technical Projects

Low SNR input LSM - Optimal Compression and Preprocessing [Report] *Oct – Nov 2022*
Course: Neuromorphic Engineering – Instructor: Prof. Udayan Ganguly

- Modelled the architecture of a **liquid state machine** (LSM) for speech recognition using a state space representation
- Simulated the pre-processing tool chain based on **Lyon's Auditory Cochlear** model for the input to the LSM network
- Modified the preprocessing chain, LSM reservior and output classification set of neurons to train the network for low SNR input (10dB) by achieving **similar spiking response** as compared to high SNR input (52dB)

Cascode CS-LNA Design [Report] *Mar – Apr 2022*
Course: RF Microelectronics – Instructor: Prof. Jayanta Mukherjee

- Designed a single ended **cascoded common source** Low Noise Amplifier (CS-LNA) in UMC 180nm CMOS technology
- Achieved a **noise figure (NF)** less than 2 dB and forward voltage gain greater than 15 dB for operation in **23.5-24GHz**
- Designed the amplifier to have IIP3 greater than -8dB and input-output port voltage reflection coefficients < -10dB

20 MHz Transimpedance Amplifier (TIA) for POF applications [Report] *Mar – Apr 2021*
Course: Electronic Design Lab – Instructor: Prof. Joseph John

- Designed a 3-stage closed loop transimpedance amplifier using CS JFET and 2 CE BJTs with collector-base biasing
- Engineered low noise, high gain amplifier featured with 20MHz of bandwidth for plastic optical fiber communication
- Tested the circuit on PCB, transmitted and received a pseudorandom binary sequence using an LED and PIN photodiode respectively

Operational Transconductance Amplifier with Class-B Slew Rate Boosting *Oct – Nov 2021*
Course: CMOS Analog VLSI Design – Instructor: Prof. Maryam S. Baghini

- Designed an operational transconductance amplifier with slew rate boosting (> **900** μVs) in PTM 130nm technology
- Engineered the amplifier to have a DC gain greater than **70dB** with the gain bandwidth product greater than **1GHz**
- Achieved the total static power consumption of Class B and the main pseudo class AB amplifier less than **4.25mW**

Leaf Nitrogen Content Estimation *Aug – Nov 2021*
Undergraduate Research Project – Guide: Prof. J Adinarayan

- Conducted literature review of **hyper-spectral** based crop physiological stress estimation for agricultural applications
- Implemented **Savitzky-Golay** convolution smoothing to denoise the reflectance, first and second derivative of data
- Performed **partial least squares** regression with to estimate leaf nitrogen and water content for maize crop for a cycle
- Achieved **28.57% increase** in the validation set correlation coefficient on incorporating 3 **feature selection** techniques

Academic Achievements

2023: Received **Undergraduate Research Award (URA01)** for excellent contribution to research

2019: Achieved **All India Rank 1446** in Joint Entrance Exam-Main out of 0.94 million candidates

2019: Secured **All India Rank 2487** in Joint Entrance Exam-Advanced out of 0.25 million candidates

Skills

Characterisation Tools: CV and IV measurement (Agilent B1500), Four probe sheet resistance and Hall measurement

Fabrication Tools: RF/DC magnetron Sputter, Atomic Layer Deposition (ALD), Optical lithography, Annealing furnace, Wet bench processes (Lift-off, Al, HfO2 and SiO2 etching)

Programming: Python, MATLAB, C++, VHDL, Verilog, Assembly, Embedded-C, LaTeX

Softwares: Sentaurus TCAD, HSpice, Cadence Virtuoso, Quartus Prime

Specialisation Courses

Nanoelectronics
Quantum Transport in Nanoscale Devices
Physics of Nanoscale Devices - I
Physics of Transistors
Microelectronics Technology Lab
Neuromorphic Engineering
CMOS Analog VLSI Design
Growth and Characterization of Nanoelectronic Materials
VLSI Design (Theory and Lab)
Radio Frequency Microelectronics Chip Design

Position of Responsibility

Sept 2023 – Present: **Coordinator, SEMIX, IIT Bombay** (Centre for Semiconductor Technologies)

Jul 2023 – Nov 2023: **Teaching Assistant, Neuromorphic Engineering**, Electrical Engineering, IIT Bombay

Jun 2022 – May 2023: **Department Academic Mentor**, Student Mentorship Program, IIT Bombay

Jun 2020 – Apr 2021: **Convener, Electronics and Robotics Club**, Institute Technical Council IIT Bombay

References

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