

Jay Sonawane

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Research Interest

Nanoelectronics- Physics of Nanoscale devices, Device Modelling, Characterization and Fabrication

Education

Indian Institute of Technology Bombay

Jul 2019 – Aug 2024 (expected)

Electrical Engineering

Dual Degree (B.Tech + M.Tech)

Specialization – Integrated Circuits and Systems, CPI – 8.21

Academic Achievements

2023: Received **Undergraduate Research Award (URA01)** for excellent contribution to research

2019: Achieved **All India Rank 1446** in Joint Entrance Exam-Main out of 0.94 million candidates

2019: Secured **All India Rank 2487** in Joint Entrance Exam-Advanced out of 0.25 million candidates

2016: Achieved **All India Rank 195** in Technothon, organised by Techniche, IIT Guwahati

Research Experience

SOI Device Optimisation for Operation in BTBT Regime [\[Report\]](#)

May 2022 – Present

Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay

(Received **Undergraduate Research Award (URA01)** in recognition of excellent contribution to preliminary activity leading to research and developmental exposure)

- Modelled a 32nm PDSOI MOSFET for operation in **band to band tunneling** (BTBT) regime in order to exercise benefits of **lower variability**, and an **ultra-low power** current source device as compared to ON and (subthreshold) SS operation
- **Calibrated** experimental results (characterized at IIT Bombay Nanofabrication facility) with simulation results of GF32nm PDSOI MOSFET (fabricated at GlobalFoundries) using **Sentaurus TCAD**
- Investigated the presence of trap assisted tunneling and direct tunneling dominant regions in BTBT regime using Hurkx and Nonlocal path models respectively, and obtained process parameter dependency of direct tunneling dominant
- Designed a **device design space** to achieve lower BTBT current (**7.5x**) which translates to **enhanced energy efficiency** of the leaky integrator, **lower spiking frequency** of the neuron, and lower area of body capacitor (**lower device area**)
- Performed variability analysis (metal grain granularity, random dopant fluctuations and Tox variations) in TCAD

Performance comparison of Patterned SOI over traditional SOI MOSFETs [\[Report\]](#)

Mar 2022 – Present

Guide: Prof. Udayan Ganguly, MeLoDe Labs, IIT Bombay

- Designed a novel SOI MOSFET- patterned SOI characterised by a **discontinuous buried oxide stack** below the channel
- Simulated the structure and **characterised** the behavior of traditional and patterned SOI MOSFET in Sentaurus TCAD
- Compared bulk, traditional SOI and patterned SOI on the basis of performance parameters in ON and SS operation

Reliability of Cryo-CMOS based circuits

Aug – Nov 2021

Undergraduate Research Project – Guide: Prof. Souvik Mahapatra

- Studied a compact model used to partition the measured threshold voltage shift kinetics for different stresses into **Hot Carrier Degradation**, **Bias Temperature Instability** and electron/hole trapping subcomponents at low temperature
- Conducted ngspice simulations for **ring oscillator analysis** to calibrate the compact HCD-BTI model for circuit aging

Industrial Experience

Atomberg Technologies

May – Jul 2022

Research and Development Intern – Mentor: Gaurav Gupta

Pune, India

- Integrated **PIR (pyro-electric IR)** sensors in existing low price HVAC technologies like fans for motion/presence detection based operation to enhance user experience and reduce energy consumption
- Tested and integrated Panasonic and Holtek PIR sensor modules on **STM8s** in Renesa fans and **esp32c3** based fans
- Developed firmware register transfer level (RTL) code for with GV4 and GV5 series of boards and tested the installation

Carnot Technologies

May – Jul 2021

Data Science Intern – Mentor: Yash Sanghvi

Mumbai, (Work from Home)

- Programmed a script that provides **time series NDVI** files using **Sentinel-hub API** and latitude-longitude boundary
- Statistically analysed sugarcane crop **NDVI** progression for around **200+** farms around the country for one crop cycle
- Developed a model using **Random Forest** regressor to predict sugar content in crop using ten **vegetation indices**
- Performed feature selection on indices and **ensemble-stacking** to achieve **94.2%** accuracy on cross validation set

Nanoelectronics Projects

Resonant Tunneling Diodes: NEGF-Poisson based consistent simulation

Mar – Apr 2023

Course: Quantum Transport – Instructor: Prof. Bhaskaran Murlidharan

- Studied the **Tsu-Isaki formulation** of resonant tunneling current for generic double barrier heterostructures (RTDs)
- Simulated tunneling probability using the **Breit-Wigner function** for varying quantum well and barrier parameters
- Modelled a resonant tunneling diode heterostructure using a self consistent **NEGF-Poisson formulation** in MATLAB to study the impact of variation in quantum well and barrier parameters on transmission coefficient and I-V characteristics

Performance comparison of Patterned SOI over traditional SOI MOSFETs [\[Report\]](#)

Mar – Apr 2022

Course: Nanoelectronics – Instructor: Prof. Udayan Ganguly

- Designed a novel SOI MOSFET- patterned SOI characterised by a **discontinuous buried oxide stack** below the channel
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Modified WKB based analytic model for direct tunneling current in MOS devices

Mar – Apr 2022

Course: Physics of Transistors – Instructor: Prof. Souvik Mahapatra

- Studied modelling of the low-field roll-off in the current resulting from proper **modelling** of the **field dependencies** of the sheet charge, electron impact frequency on the interface, and tunneling probability
- Reproduced the results using a modified WKB approach consisting of the usual WKB tunneling probability valid for smoothly varying potentials, and a reflection coefficient for **correcting reflections** from potential discontinuities

Improving Photoluminescence in InAs Surface Quantum Dots [\[Report\]](#)

Mar – Apr 2021

Course: Growth and Characterization of Nanoelectronic Materials – Instructor: Prof. S. Chakrabarti

- Demonstrated the advantages of incorporating **antimony** (Sb) as a **surfactant** into a strained InGaAs quantum well
- Simulated InAs SQDs in NextNano ++ software to observe the effects of **extended planar growth** and dot formation
- Schrutinised the effect of Sb to delay three-dimensional (3D) growth in InAs surface quantum dots to render **improvement in carrier confinement**, lower energy band gap and **achieve longer emission wavelength**

Technical Projects

Low SNR input LSM - Optimal Compression and Preprocessing [\[Report\]](#)

Oct – Nov 2022

Course: Neuromorphic Engineering – Instructor: Prof. Udayan Ganguly

- Modelled the architecture of a **liquid state machine** (LSM) for speech recognition using a state space representation
- Simulated the pre-processing tool chain based on **Lyon's Auditory Cochlear** model for the input to the LSM network
- Modified the preprocessing chain, LSM reservoir and output classification set of neurons to train the network for low SNR input (10dB) by achieving **similar spiking response** as compared to high SNR input (52dB)

Cascode CS-LNA Design [\[Report\]](#)

Mar – Apr 2022

Course: RF Microelectronics – Instructor: Prof. Jayanta Mukherjee

- Designed a single ended **cascoded common source** Low Noise Amplifier (CS-LNA) in UMC 180nm CMOS technology
- Achieved a **noise figure (NF)** less than 2 dB and forward voltage gain greater than 15 dB for operation in **23.5-24GHz**
- Designed the amplifier to have IIP3 greater than -8dB and input-output port voltage reflection coefficients < -10dB

20 MHz Transimpedance Amplifier (TIA) for POF applications [\[Report\]](#)

Mar – Apr 2021

Course: Electronic Design Lab – Instructor: Prof. Joseph John

- Designed a 3-stage closed loop transimpedance amplifier using CS JFET and 2 CE BJTs with collector-base biasing
- Engineered low noise, high gain amplifier featured with 20MHz of bandwidth for plastic optical fiber communication
- Tested the circuit on PCB, transmitted and received a pseudorandom binary sequence using an LED and PIN photodiode respectively

Gaussian Elimination System [\[Report\]](#)

Oct – Nov 2022

Course: Algorithmic Design of Digital Systems – Instructor: Prof. M.P. Desai

- Implemented single precision floating point divider using **Newton-Raphson** by subtraction and multiplication only
- Designed a circuit for solving **16 linear equations** using Gaussian elimination method which used the above single precision floating point divider and simulated on software and hardware testbench in AA language
- Studied the impact of **loop unrolling** on the performance of a FIR filter by doing two-level and four-level unrolling

Operational Transconductance Amplifier with Class-B Slew Rate Boosting

Oct – Nov 2021

Course: CMOS Analog VLSI Design – Instructor: Prof. Maryam S. Baghini

- Designed an operational transconductance amplifier with slew rate boosting ($> 900 \mu V/s$) in PTM 130nm technology
- Engineered the amplifier to have a DC gain greater than **70dB** with the gain bandwidth product greater than **1GHz**
- Achieved the total static power consumption of Class B and the main pseudo class AB amplifier less than **4.25mW**

Temperature Monitor [\[Code\]](#)

Mar – Apr 2021

Course: Microprocessors Lab – Instructor: Prof. S Saravanan

- Programmed a temperature monitor on the **Atmel AT89C51** micro-controller (PT-51) integrated with an **LCD module**
- Integrated LM35 temperature sensor using **ADC** MCP3008 with the board and used SL100 as an **amplifier** for speaker
- Used timer **interrupts** to play an audio alarm in case of sudden temperature shoot or fall and used **SPI** for interfacing

16 Bit Arithmetic Logic Unit [\[Code\]](#)

Nov – Dec 2020

Course: Digital Systems – Instructor: Prof. Virendra Singh

- Designed and implemented a 16 bit signed **Kogge Stone** fast adder and subtractor using structural VHDL in Quartus
- Integrated an adder, subtractor, XOR (using ROBDD) and NAND into an ALU using MUX circuit for controlling operation

Leaf Nitrogen Content Estimation

Aug – Nov 2021

Undergraduate Research Project – Guide: Prof. J Adinarayan

- Conducted literature review of **hyper-spectral** based crop physiological stress estimation for agricultural applications
- Implemented **Savitzky-Golay** convolution smoothing to denoise the reflectance, first and second derivative of data
- Performed **partial least squares** regression with to estimate leaf nitrogen and water content for maize crop for a cycle
- Achieved **28.57% increase** in the validation set correlation coefficient on incorporating 3 **feature selection** techniques

Planet and Atmosphere Renderer [\[Code\]](#)

Apr – Jun 2020

Seasons of Code, WnCC IIT Bombay

- Developed a real-time engine capable of rendering the earth along with atmospheric scattering using **GLFW** library
- Studied the **graphics** and **modelling-viewing** pipeline, vao and vbo code, and GLSL planet specific shaders in **OpenGL**
- Integrated **normalised cube sphere** mesh with day, night and normal shaders maps with different types of lighting

Skills

Programming: Python, C++, VHDL, Assembly, Embedded-C, \LaTeX

Softwares: MATLAB, Sentaurus TCAD, NGSpice, Cadence Virtuoso, Quartus Prime, Eagle, GNURadio

Specialisation Courses

Nanoelectronics
Quantum Transport in Nanoscale Devices
Physics of Nanoscale Devices - I
Neuromorphic Engineering
CMOS Analog VLSI Design
Radio Frequency Microelectronics Chip Design
Microprocessors (Theory and Lab)

Physics of Transistors
Microelectronics Technology Lab
Growth and Characterization of Nanoelectronic Materials
VLSI Design (Theory and Lab)
Foundations of VLSI CAD
High Speed Interconnects: Signaling and Synchronization
Algorithmic Design of Digital Systems

Position of Responsibility

Department Academic Mentor, Electrical Engineering

Jun 2022 – May 2023

Student Mentorship Program, IIT Bombay

- Part of 40-membered team, selected from **100+ applicants** on the basis of interviews and extensive peer review
- Mentoring twelve sophomores to help them with academic issues, time management and extra-curricular endeavours
- Gathered essential resources and compiled **course reviews** for the DAMP website to aid students for course selection

Convener, Institute Technical Council

Jun 2020 – Apr 2021

Electronics and Robotics Club, IIT Bombay

- A **core member** of an **fifteen-member** group aimed to organize 20+ events, competitions and hackathons
- Conducted a session to consolidate **Linux terminal commands** for ROS introduction, attended by 100+ enthusiasts
- Conducted fully virtual Club Orientation program and a two day **Arduino boot-camp** addressing about 200 freshmen

Extra Curriculars

2022: Mentored four teams in XLR8, a bot making competition

2022: Participated in Hip Hop dance in the Annual Insync Dance Show (AIDS)

2020: Represented IIT Bombay in **UMANG**, an **inter-college dance competition** in solo dance

2020: Completed year-long training in **Table Tennis** under the **National Sports Organisation**, IITB

2019: Finalist in the **Freshiezza solo dance** competition organized by Insync, IIT Bombay for freshmen

2019: Assembled a miniature **aircraft** in the RC-Plane competition organised by the Aeromodelling Club

2019: Engineered a **bluetooth controlled bot** capable of negotiating obstacles in the XLR8 competition

2012: Qualified the first four professional **tabla** exams conducted by the **ABGMV** Mandal, Mumbai