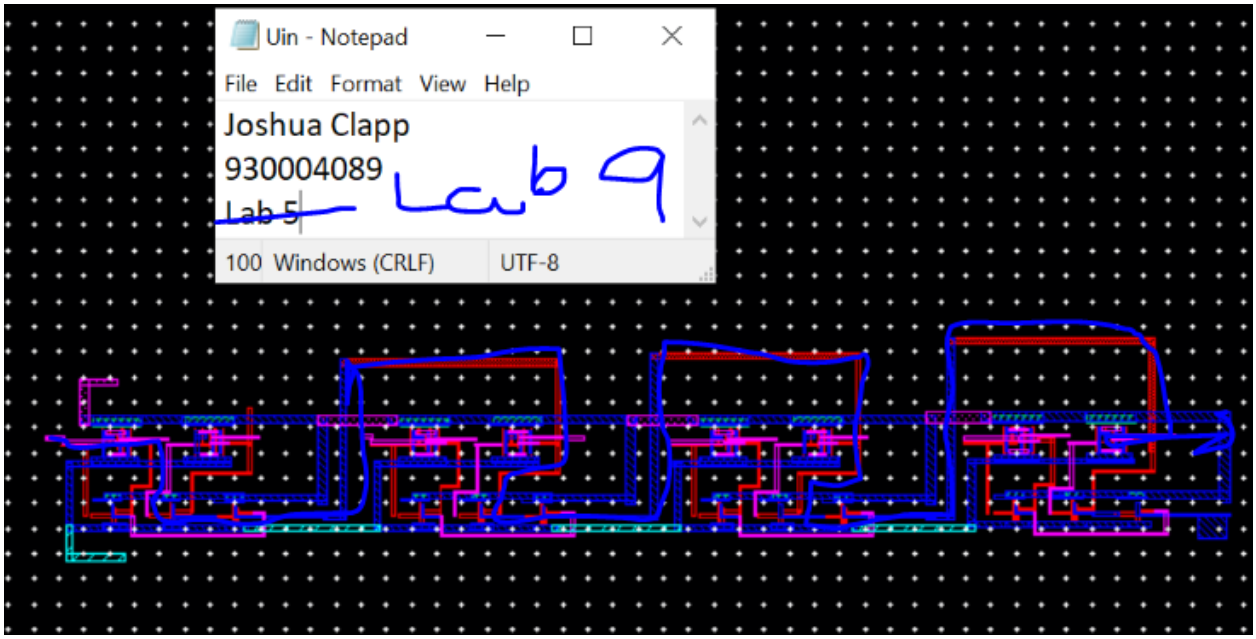
Joshua Clapp

Instead of recreating the whole lab using transistor level, I modified the symbols with the shown transistors and resimulated. This LAYOUT not schematic best showed the actual work I did since the shows nmos and pmos paths, not the recalculated values.

Layout:



Critical path is: xor0 -> nand0 -> nand0 -> nand1 -> nand1 -> nand2 -> nand2 -> xor3

Critical path:
adder0 = (4 * 4/3 * 4/3) path xor -> nand -> nand
adder1 = (4/3 * 4/3) path nand -> nand
adder2 = (4/3 * 4/3) path nand -> nand
adder3 = (4) path xor

Unused Brach paths:
adder0 = (4) path xor
adder1 = (4) path xor
adder2 = (4) path xor
adder3 = (4/3) path nand

G (Logical Effort Path) = 89.898

H (Electrical Effort Path) = 30 fF / 9.85 fF = 3.05
B (Branching Effort Path) = 85.333
F (Logical * Electrical * Branching) = 23364.35
N = 8
f(hat) = (GBH)^(1/N) = 3.52

Delays:

Case	Pins	Non Optimized	Optimzed	Improvement
A=0000	Sum 0	6600	921	12.24571201
B=1111	Sum 1	9451	970	9.308127819
Carry In=1	Sum 2	1021	1062	50.98415747
	Sum 3	1061	1074	50.30444965
	Carry	985	981	49.8982706
A=1010	Sum 0	662	921	58.18066961
B=0101	Sum 1	1112	1065	48.92053284
Carry In=0	Sum 2	1025	1002	49.4326591
	Sum 3	1023	1000	49.43153732
	Carry	985	993	50.20222447
A=1010	Sum 0	663	921	58.14393939
B=0101	Sum 1	945	982	50.96004152
Carry In=1	Sum 2	1025	1014	49.73025993
	Sum 3	1063	1032	49.2601432
	Carry	1258	1086	46.33105802
A=1100	Sum 0	702	923	56.8
B=1000	Sum 1	709	952	57.31487056
Carry In=0	Sum 2	1036	1052	50.38314176
	Sum 3	750	931	55.38370018
	Carry	1584	1071	40.33898305

Power consumptions:

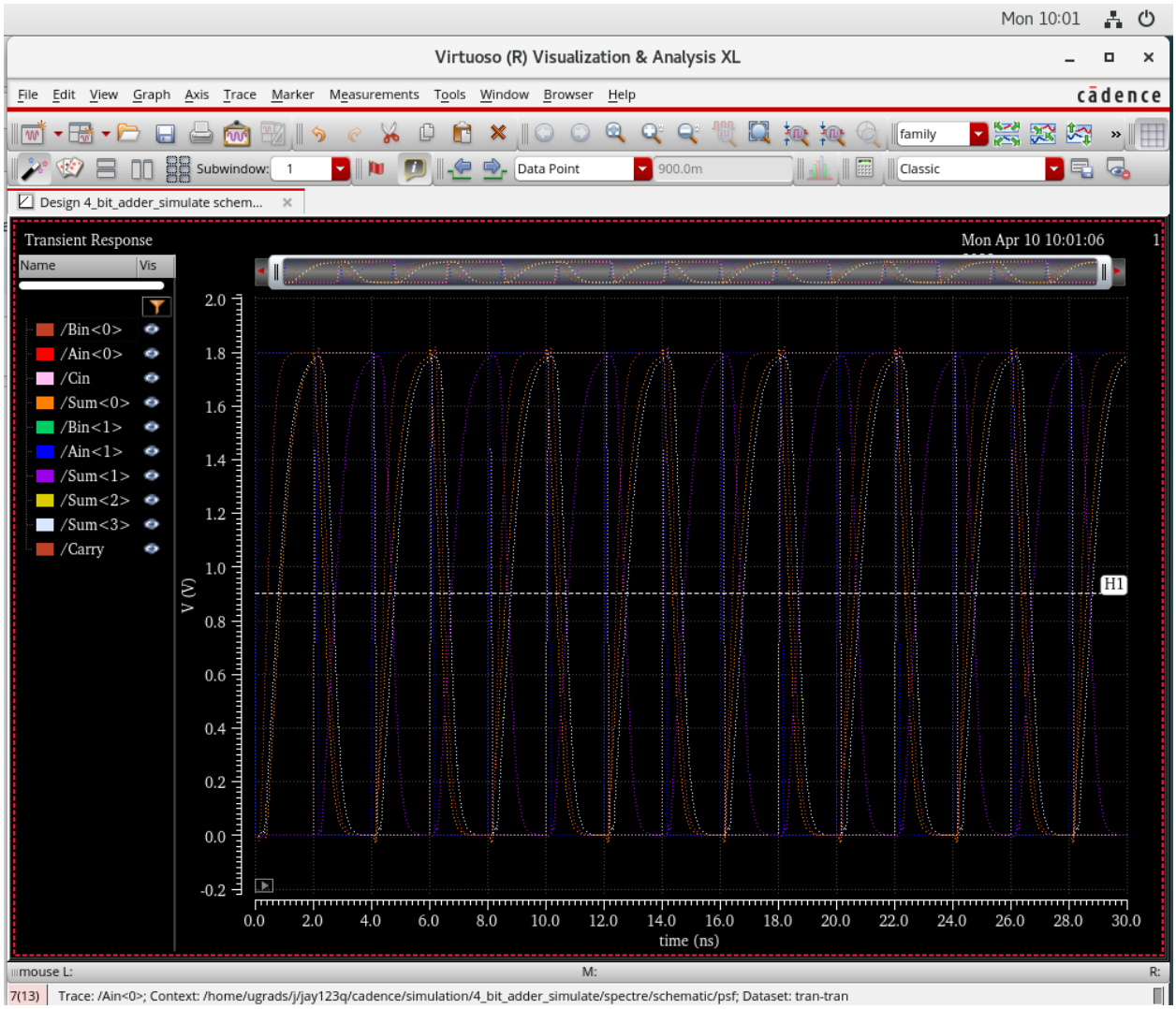
Case	Non-optimized (uW)	Optimized (uW)	Improvement
A=0000, B=1111, Carry In= 1	-330.8	-87.6	20.93690249
A=1010,B= 0101, Carry In= 0	-472	-86.2	15.44249373
A=1010, B=0101, Carry In=1	-330.8	-86.47	20.7227934
A=1100, B=1000, Carry In=0	-457.625	-88.9	16.2664105

Area:

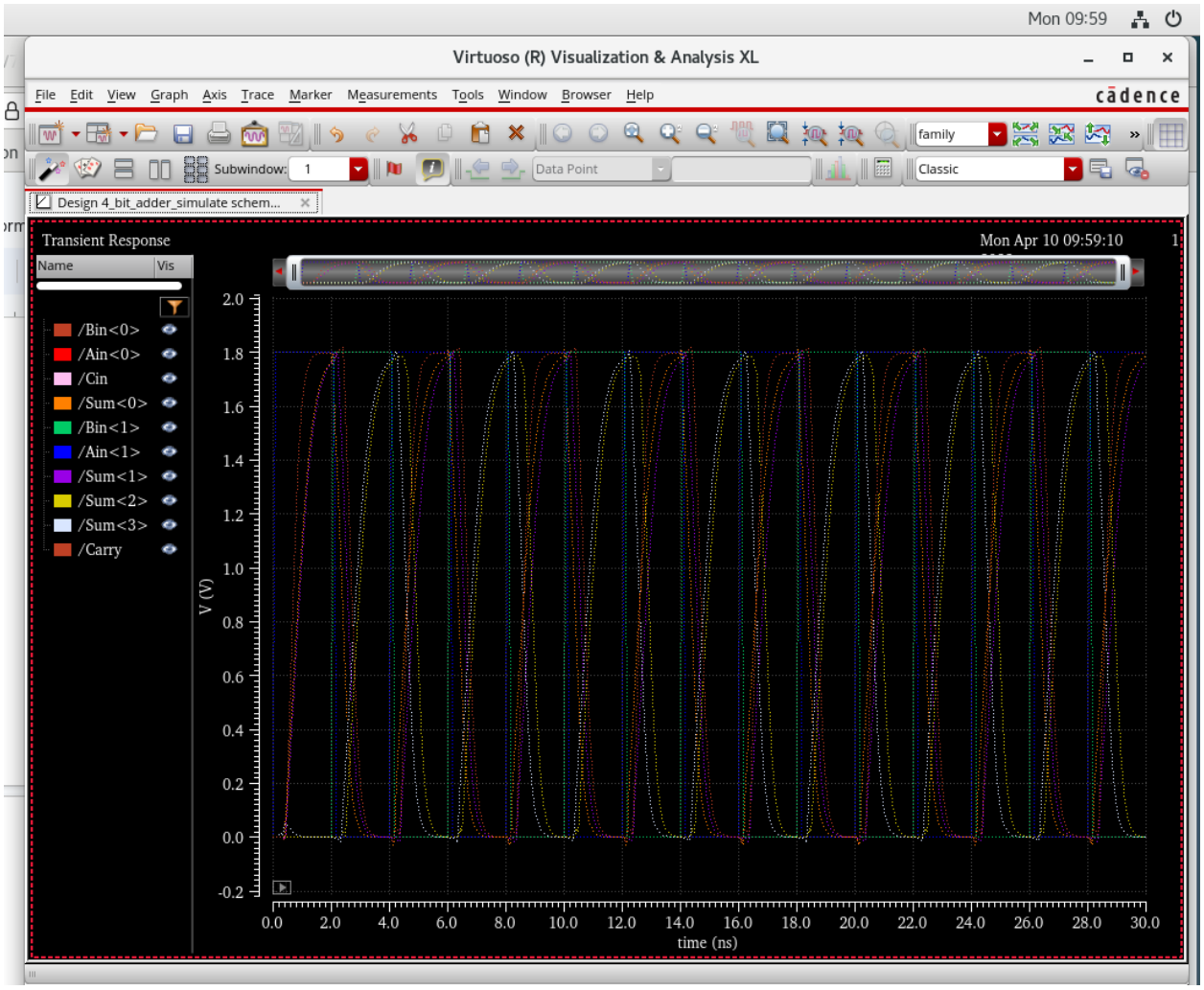
Non-optimized (u^2 m^2)	Optimized (u^2 m^2)
8800000	17440000

Proof

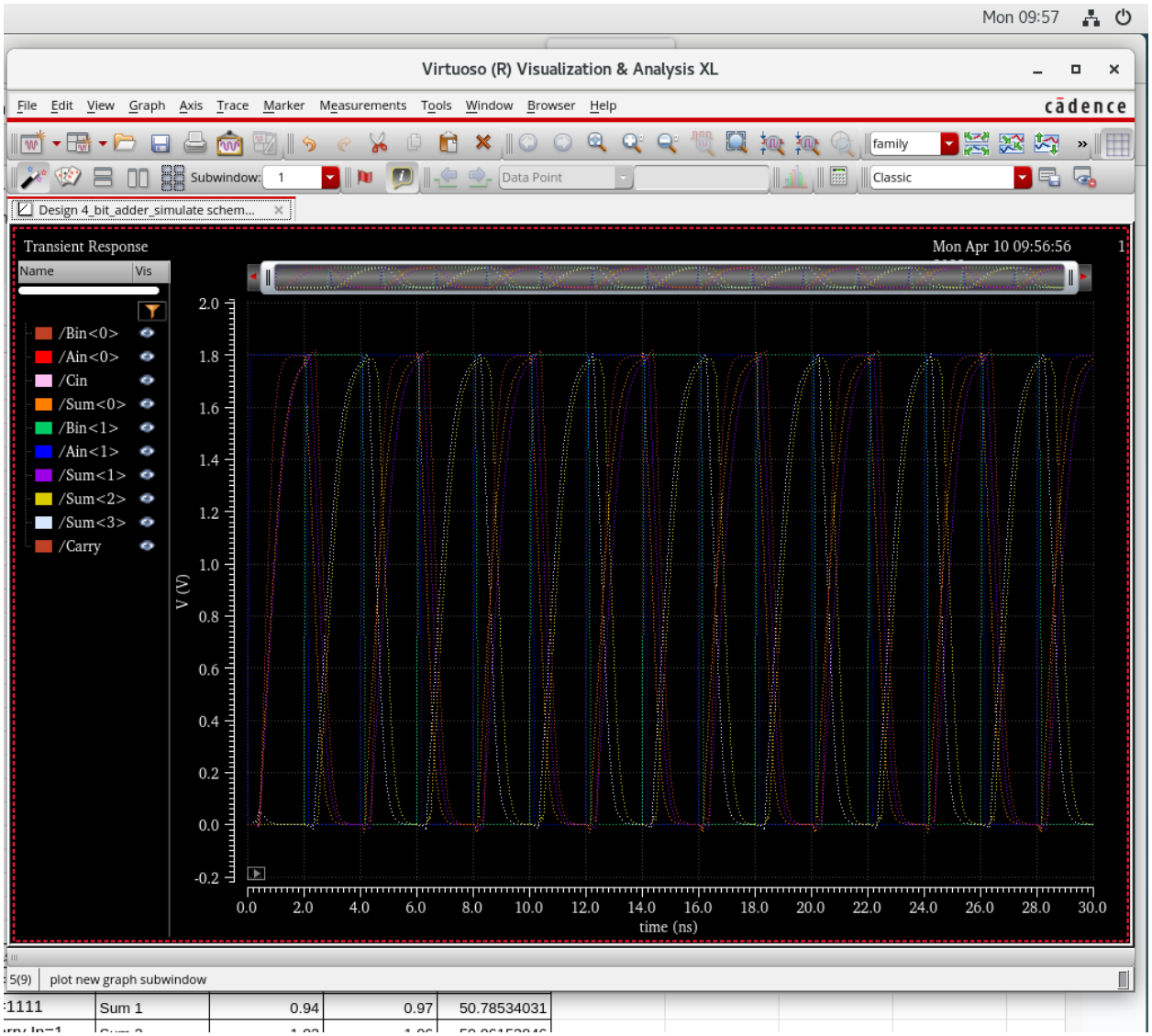
Case 1 screenshot



Case 2 screen shot



Case 3 screenshot


Mon 09:57
Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
Data Point
Classic
Design 4_bit_adder_simulate schem...
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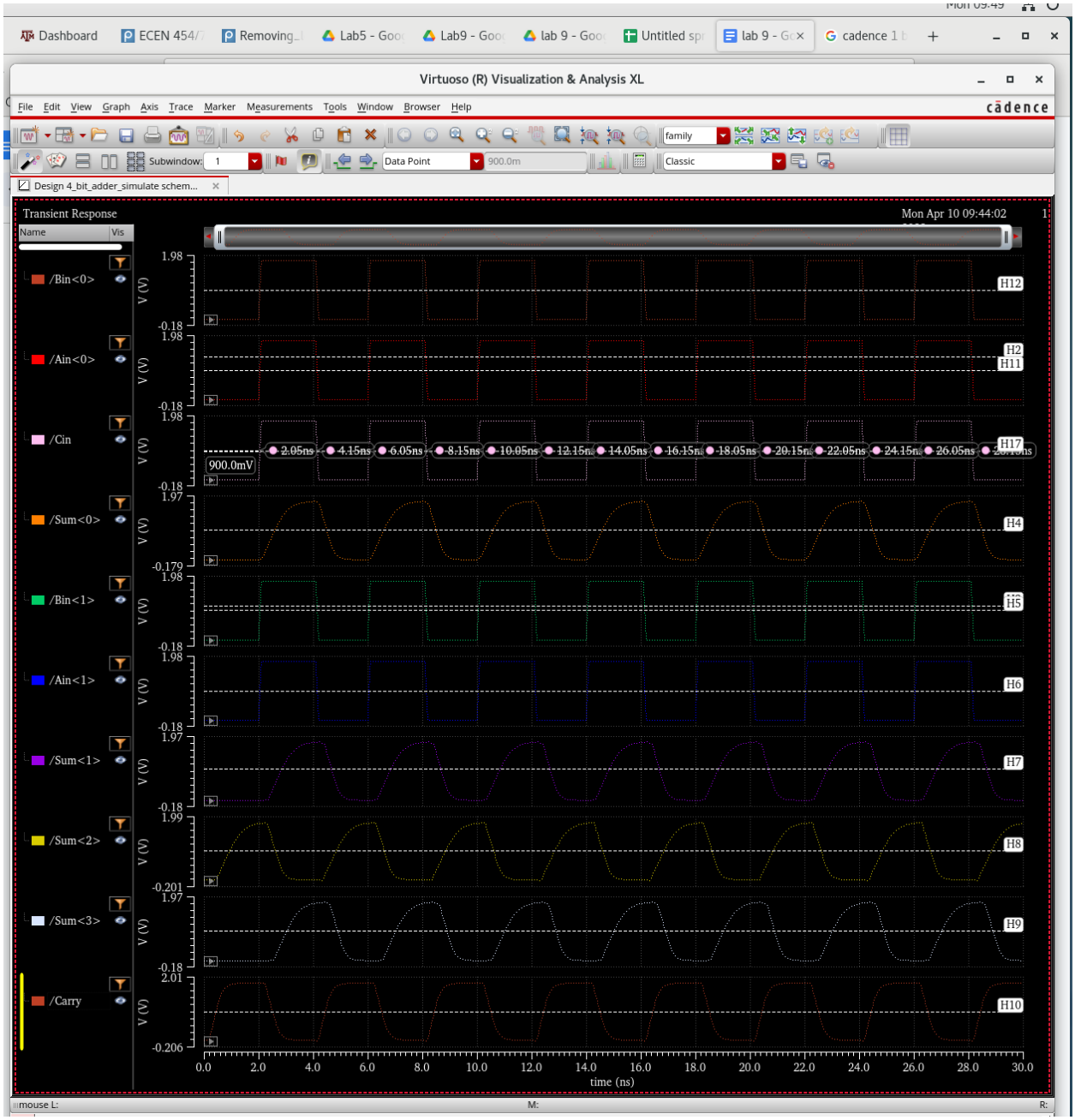
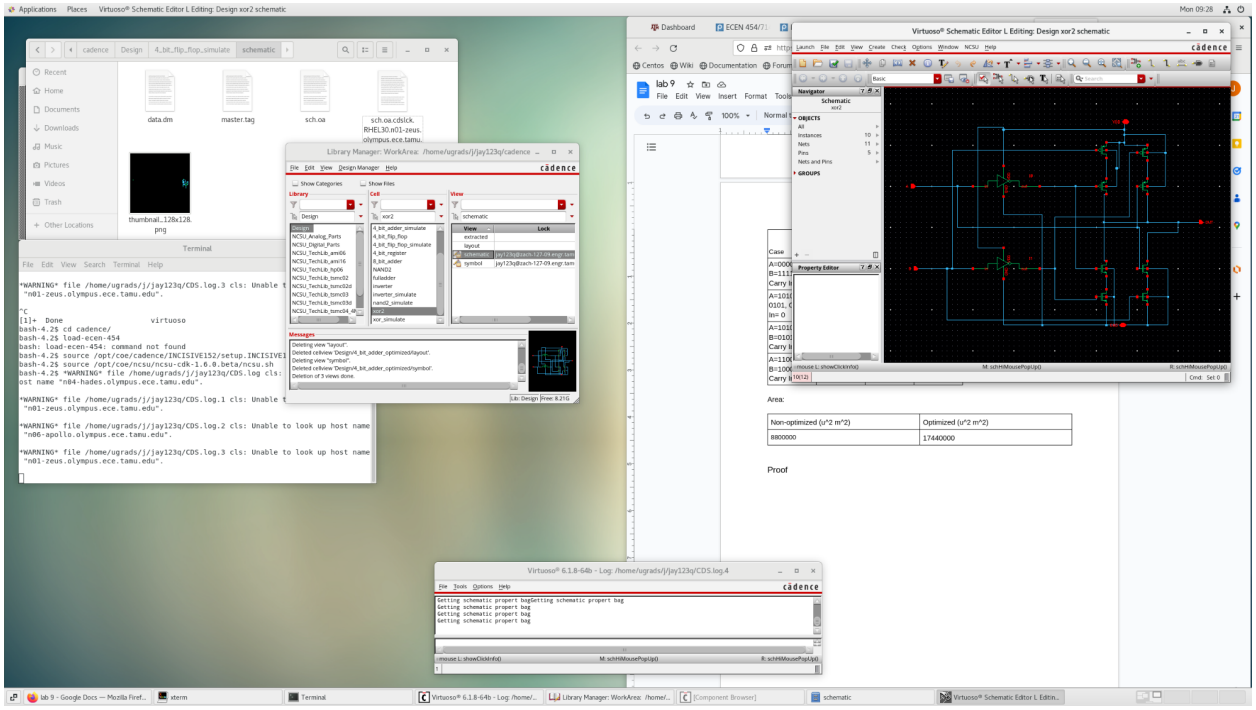
Name
Vis
/Bin<0>
/Ain<0>
/Cin
/Sum<0>
/Bin<1>
/Ain<1>
/Sum<1>
/Sum<2>
/Sum<3>
/Carry
V (V)
time (ns)
plot new graph subwindow
Sum 1
0.94
0.97
50.78534031

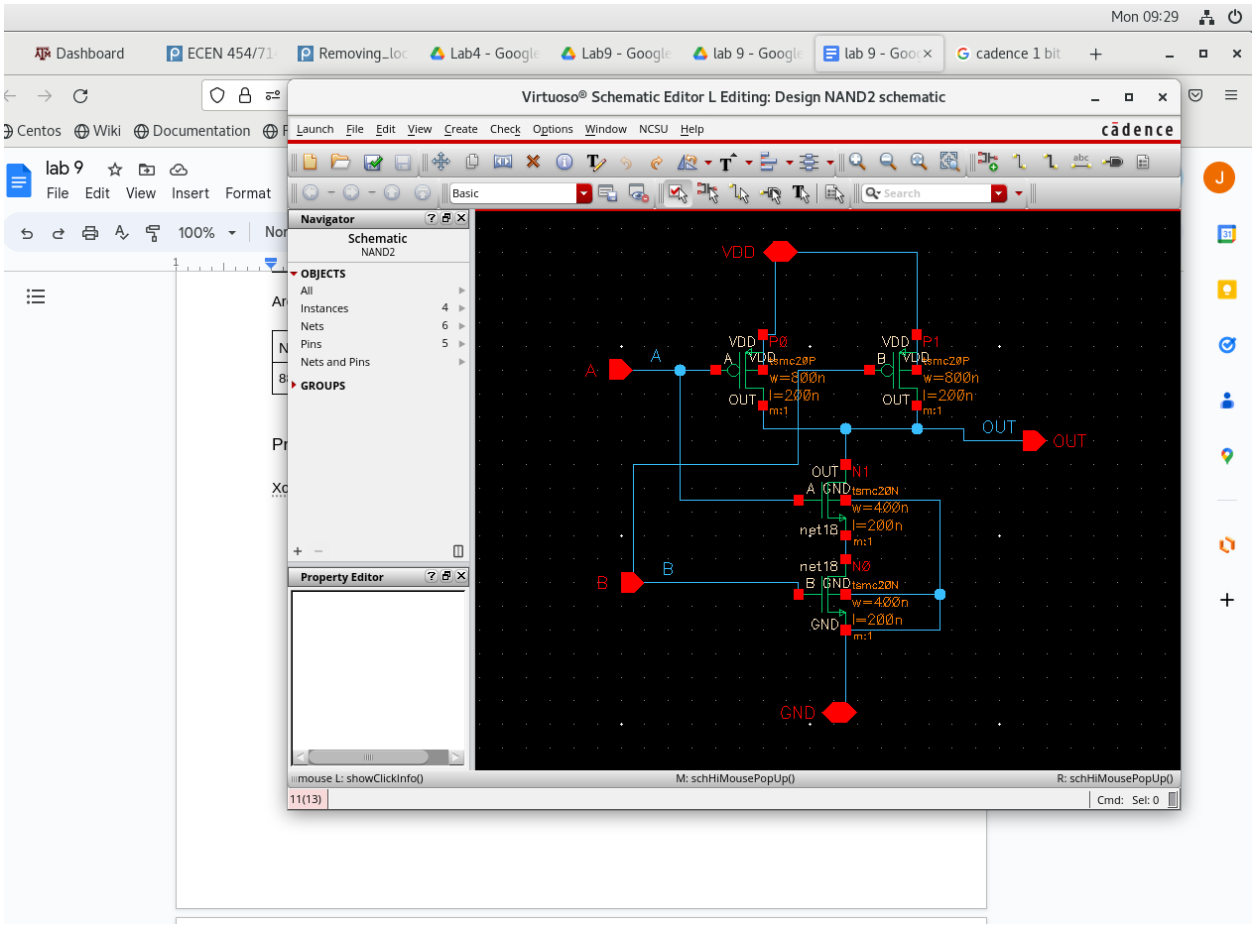
Case 4 screenshot



Xor


Virtuoso® Schematic Editor L Editing: Design xor2 schematic
Area:
Non-optimized (u^2 m^2)
Optimized (u^2 m^2)
8800000
17440000
Proof

Nand


Mon 09:29
Dashboard
ECEN 454/71
Removing_loc
Lab4 - Google
Lab9 - Google
lab 9 - Google
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cadence 1 bit
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lab 9
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100%
Virtuoso® Schematic Editor L Editing: Design NAND2 schematic
Launch File Edit View Create Check Options Window NCSU Help
cadence
Basic
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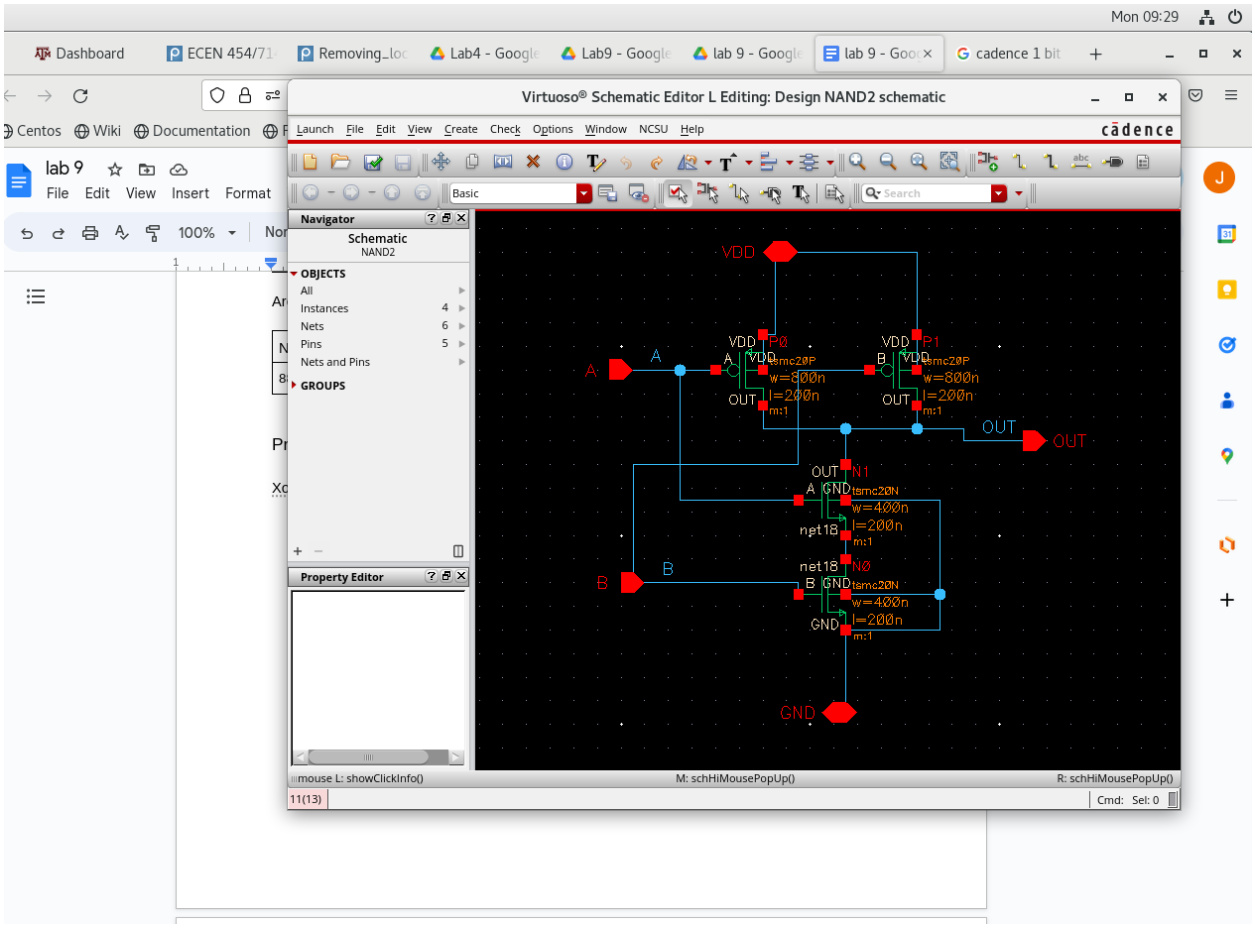
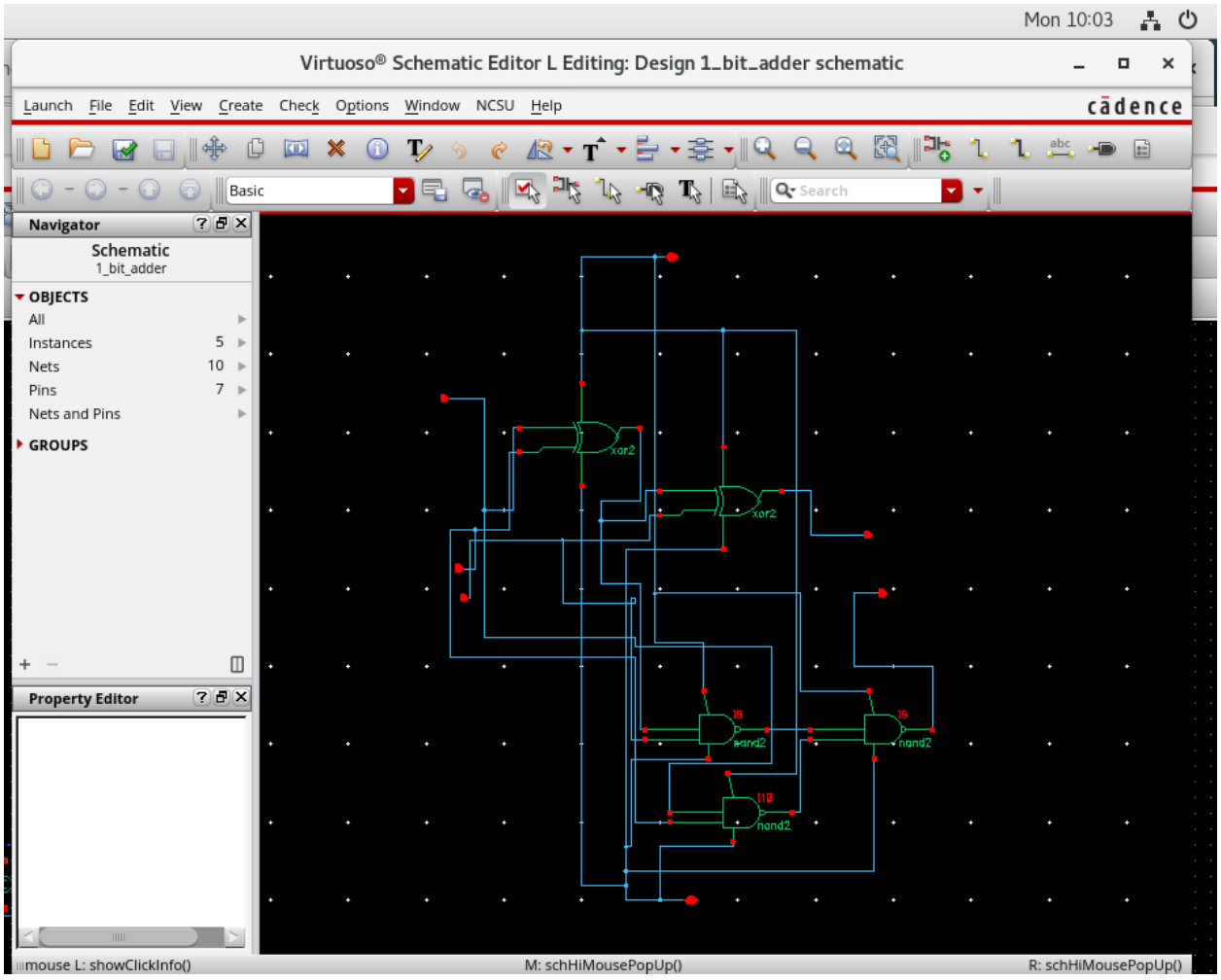
NAND2
OBJECTS
All
Instances 4
Nets 6
Pins 5
Nets and Pins
GROUPS
Property Editor
VDD
A
B
OUT
GND
P0
P1
N1
N0
tsmc20P
tsmc20N
w=800n
w=400n
l=200n
m:1
net18
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
11(13)
Cmd:
Sel: 0

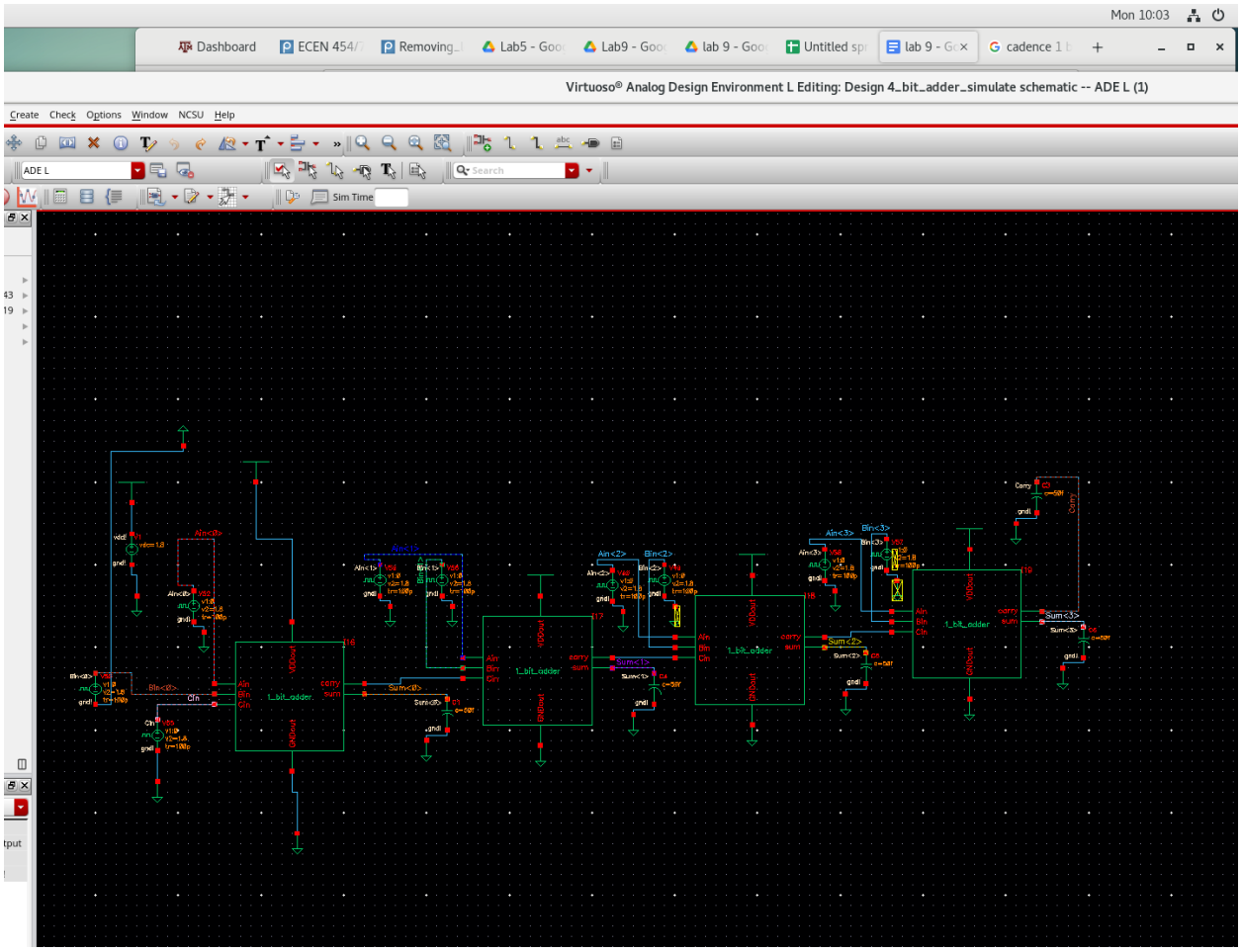
Inverter



Schematic whole

MODIFIED NAND, INVERTER, AND XOR TRANSISTOR GATES TO BUILD GET PLOTS RATHER THAN REBUILD TRANSISTOR LEVEL GATES


Mon 10:03
Virtuoso® Schematic Editor L Editing: Design 1_bit_adder schematic
Launch File Edit View Create Check Options Window NCSU Help
cadence
Basic
Search
Navigator
Schematic
1_bit_adder
OBJECTS
All
Instances 5
Nets 10
Pins 7
Nets and Pins
GROUPS
Property Editor
xor2
xor2
nand2
nand2
nand2
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()


Mon 10:03
Dashboard
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lab 9 - Goo
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cadence 1 L
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Options
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Search
Sim Time
1_bit_adder
Ain<3>
Bin<3>
Sum<3>
Sum<2>
Sum<1>
Sum<0>
carry
sum
Cin
Cout
VDDout
GNDout