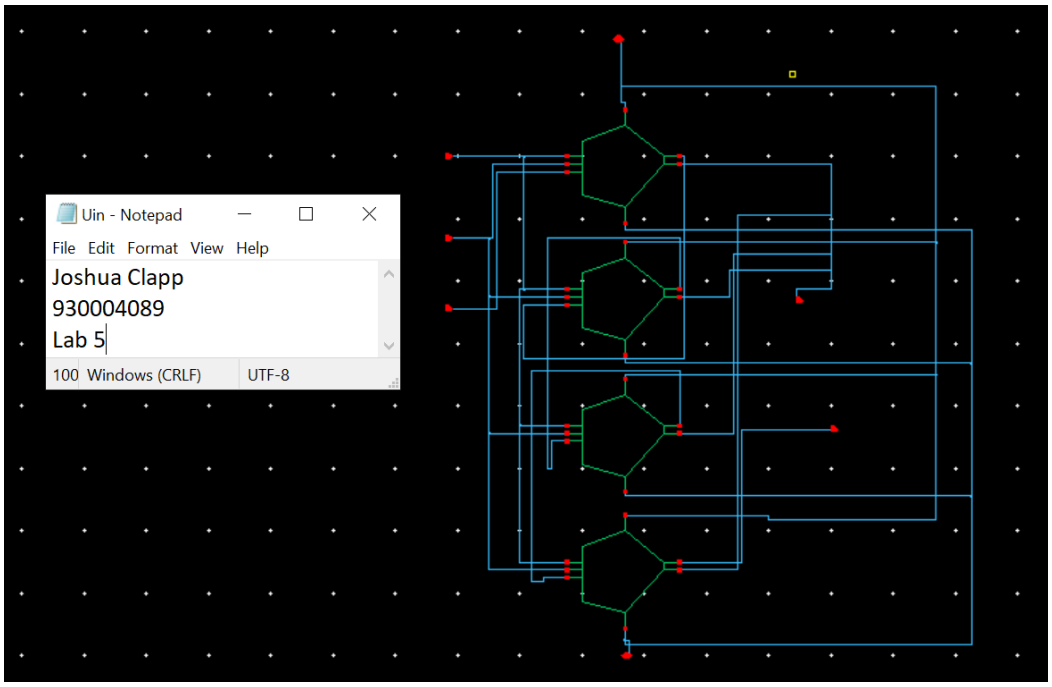
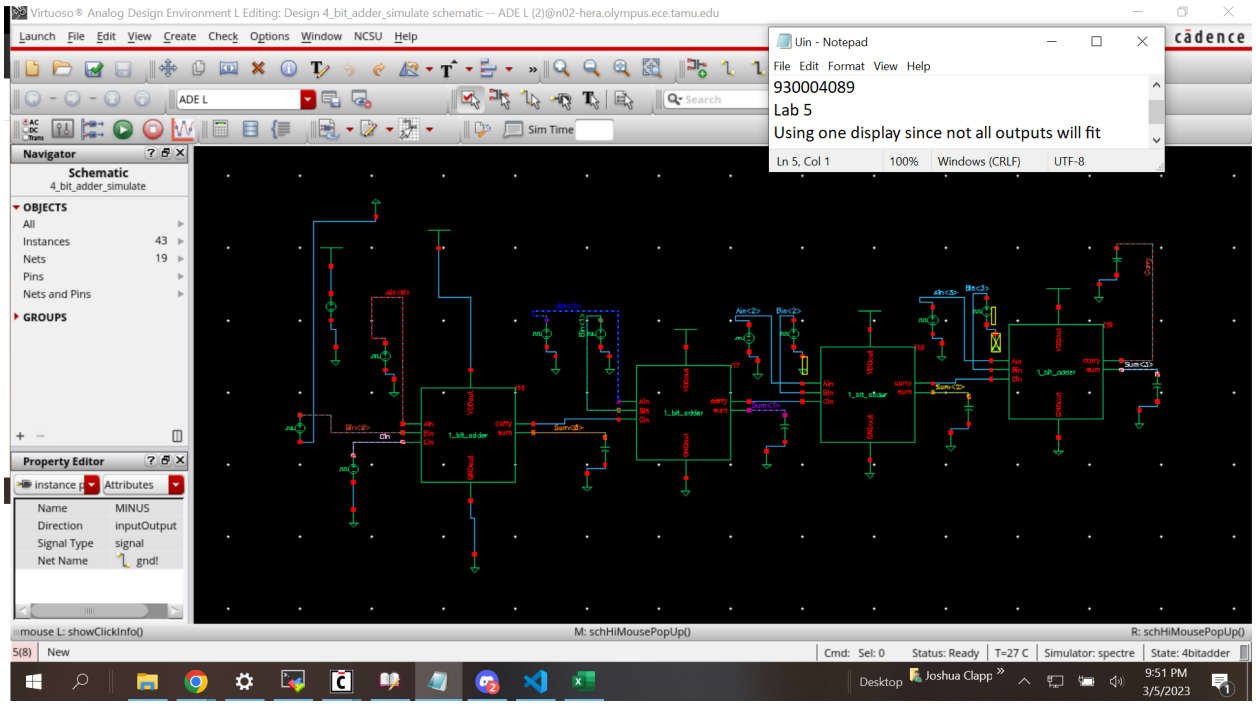
Joshua Clapp

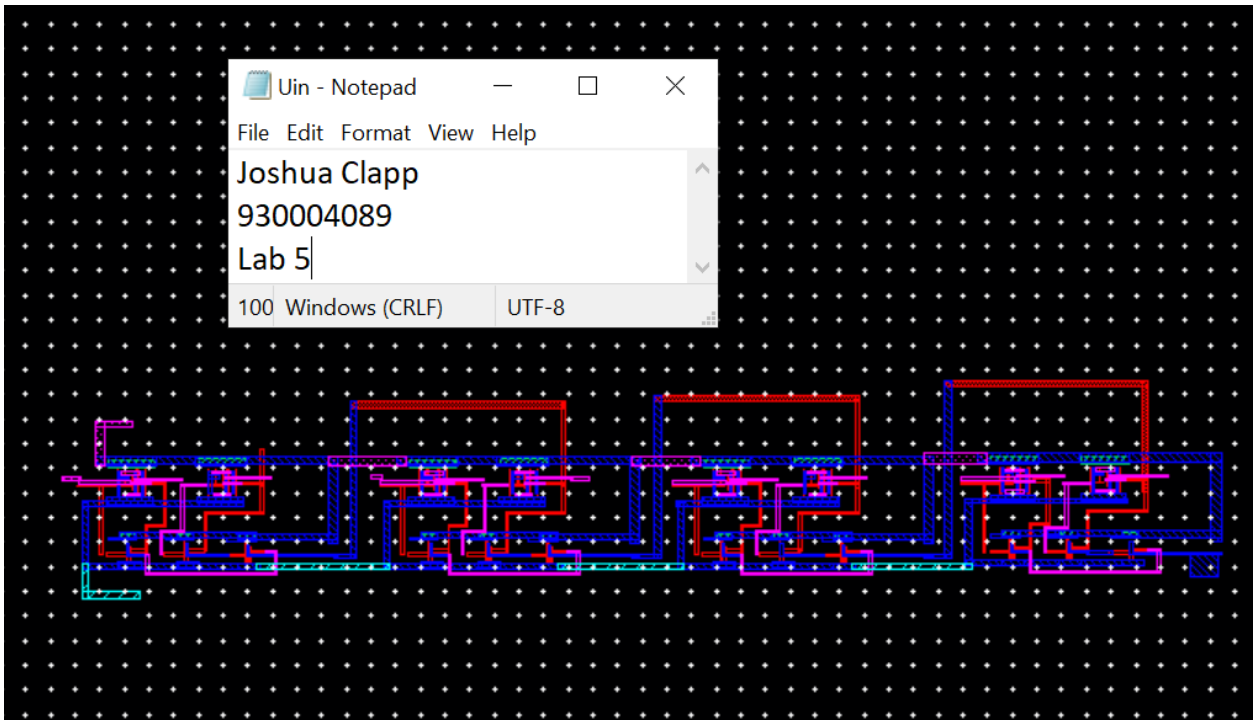
4 bit adder schematic



4 Bit Full Adder Pulse Schematic



4 Bit Full Adder Layout



LVS

@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/j/jay123q/cadence/LVS -l -s -t /home/ugrads/j/jay123q/cadence/LVS/layout /home/ugrads/j/jay123q/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/ugrads/j/jay123q/cadence/LVS/layout/netlist

count	
91	nets
16	terminals
72	pmos
72	nmos

Net-list summary for /home/ugrads/j/jay123q/cadence/LVS/schematic/netlist

count	
91	nets
16	terminals
72	pmos

72 nmos

Terminal correspondence points

N87	N8	Ain<0>
N85	N10	Ain<1>
N83	N11	Ain<2>
N82	N12	Ain<3>
N77	N4	Bin<0>
N75	N1	Bin<1>
N86	N7	Bin<2>
N84	N17	Bin<3>
N90	N9	Carry
N78	N13	Cinput
N80	N18	GND
N81	N16	Sum<0>
N79	N14	Sum<1>
N76	N5	Sum<2>
N89	N3	Sum<3>
N88	N0	VDD

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout instances	schematic
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	144	144
total	144	144

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	91	91
total	91	91

	terminals	
un-matched	0	0
matched but different type	14	14
total	16	16

Probe files from /home/ugrads/j/jay123q/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal Ain<0>'s type in the schematic: input, in the layout: inputOutput
? Terminal Ain<1>'s type in the schematic: input, in the layout: inputOutput
? Terminal Ain<2>'s type in the schematic: input, in the layout: inputOutput
? Terminal Ain<3>'s type in the schematic: input, in the layout: inputOutput
? Terminal Bin<0>'s type in the schematic: input, in the layout: inputOutput
? Terminal Bin<1>'s type in the schematic: input, in the layout: inputOutput
? Terminal Bin<2>'s type in the schematic: input, in the layout: inputOutput
? Terminal Bin<3>'s type in the schematic: input, in the layout: inputOutput
? Terminal Carry's type in the schematic: output, in the layout: inputOutput
? Terminal Cinput's type in the schematic: input, in the layout: inputOutput
? Terminal Sum<0>'s type in the schematic: output, in the layout: inputOutput
? Terminal Sum<1>'s type in the schematic: output, in the layout: inputOutput
? Terminal Sum<2>'s type in the schematic: output, in the layout: inputOutput
? Terminal Sum<3>'s type in the schematic: output, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/ugrads/j/jay123q/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

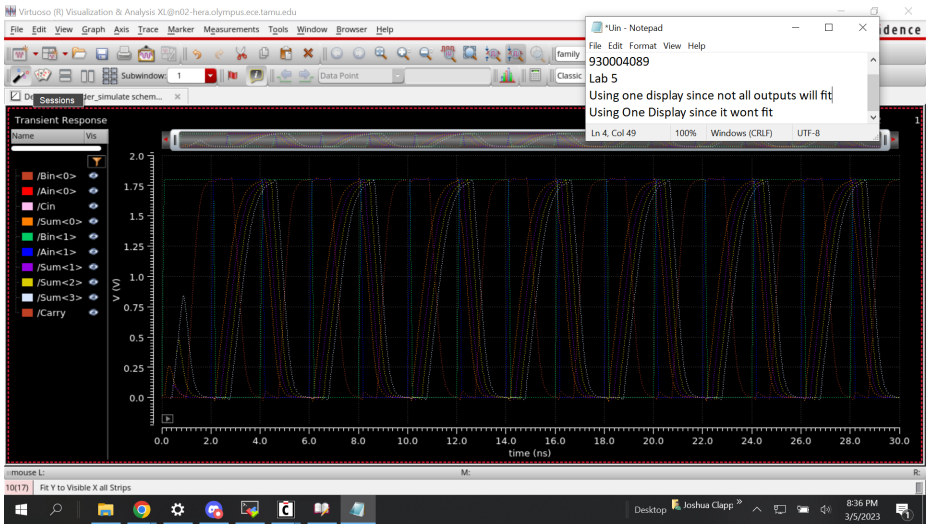
termbad.out:
? Terminal Ain<0>'s type in the layout: inputOutput, in the schematic: input
? Terminal Ain<1>'s type in the layout: inputOutput, in the schematic: input
? Terminal Ain<2>'s type in the layout: inputOutput, in the schematic: input
? Terminal Ain<3>'s type in the layout: inputOutput, in the schematic: input
? Terminal Bin<0>'s type in the layout: inputOutput, in the schematic: input
? Terminal Bin<1>'s type in the layout: inputOutput, in the schematic: input
? Terminal Bin<2>'s type in the layout: inputOutput, in the schematic: input
? Terminal Bin<3>'s type in the layout: inputOutput, in the schematic: input
? Terminal Carry's type in the layout: inputOutput, in the schematic: output
? Terminal Cinput's type in the layout: inputOutput, in the schematic: input
? Terminal Sum<0>'s type in the layout: inputOutput, in the schematic: output
? Terminal Sum<1>'s type in the layout: inputOutput, in the schematic: output
? Terminal Sum<2>'s type in the layout: inputOutput, in the schematic: output
? Terminal Sum<3>'s type in the layout: inputOutput, in the schematic: output

prunenet.out:

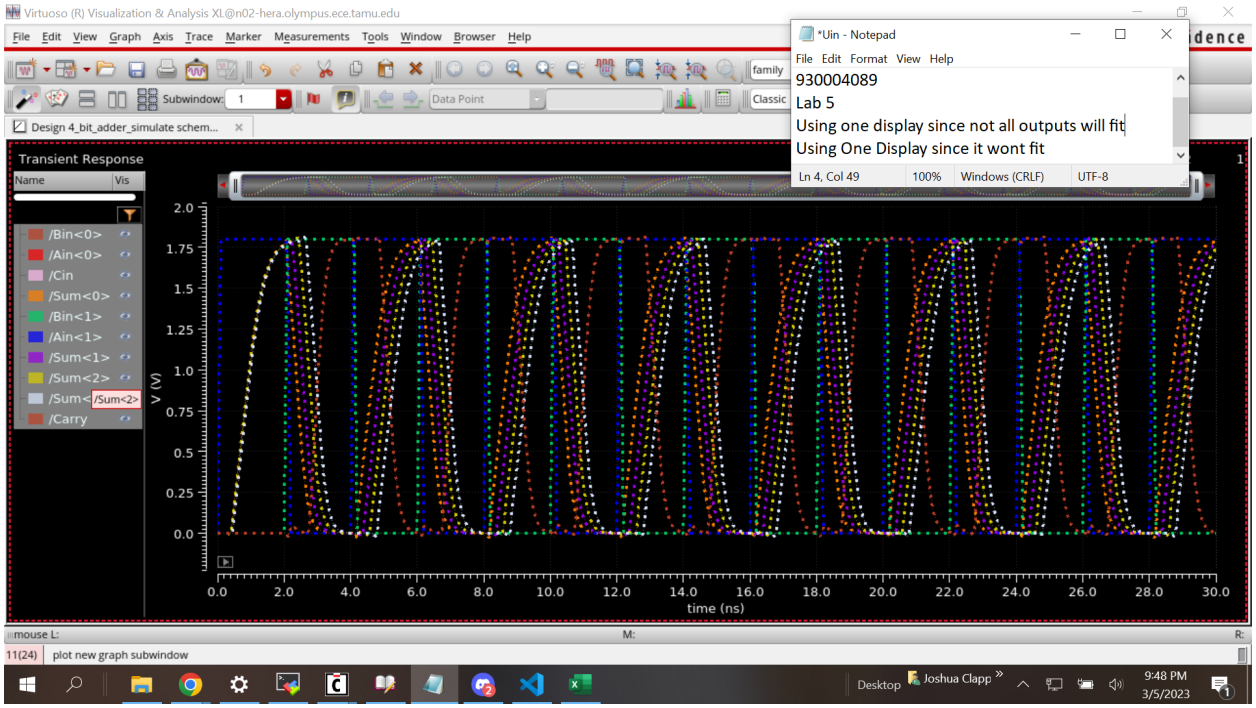
prunedev.out:

Audit.out:

4 Bit Adder Waveform 1

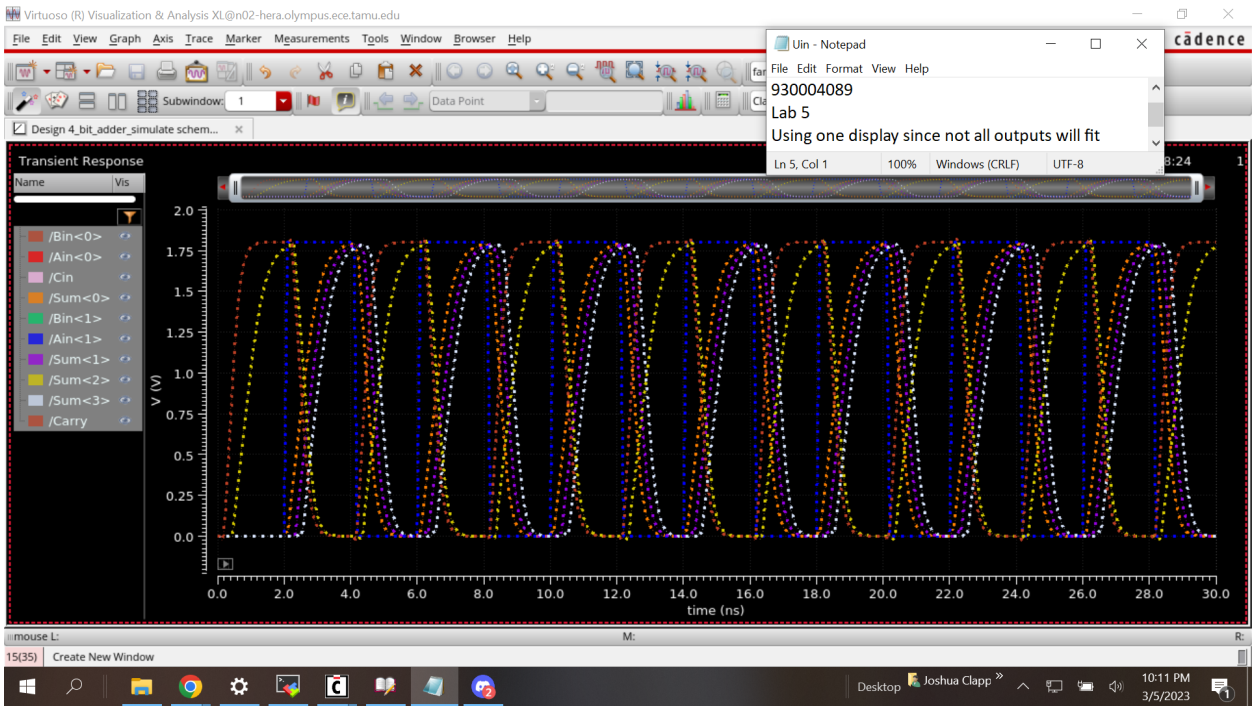


4 Bit Adder Waveform 2



4 Bit Adder Waveform 3

4 Bit Adder Waveform 4



Delay Table Falling and Rising Ratios:

Delay	Sample 1	Sample 2	Sample 3	Sample 4
Sum 0	26.703%	45.8%	31.90%	30.03%
Sum 1	9.17%	13.17%	4.16%	28.45%
Sum 2	2.39%	2.26%	1.64%	3.11%
Sum 3	3.32%	2.02%	6.11%	24.93%
Cout	25.14%	2.31%	26.06%	6.17%

Power Consumption Table:

Power	VDD
Sample 1	-330.8u
Sample 2	-472u
Sample 3	-330.8u
Sample 4	-457.625u