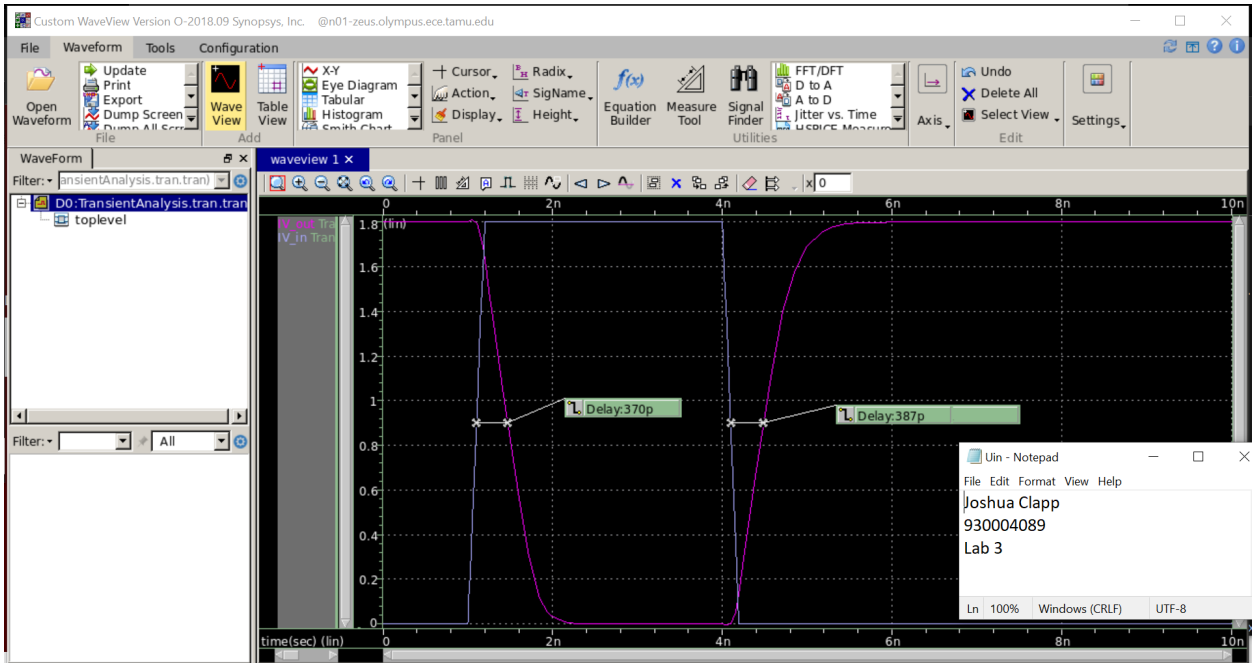
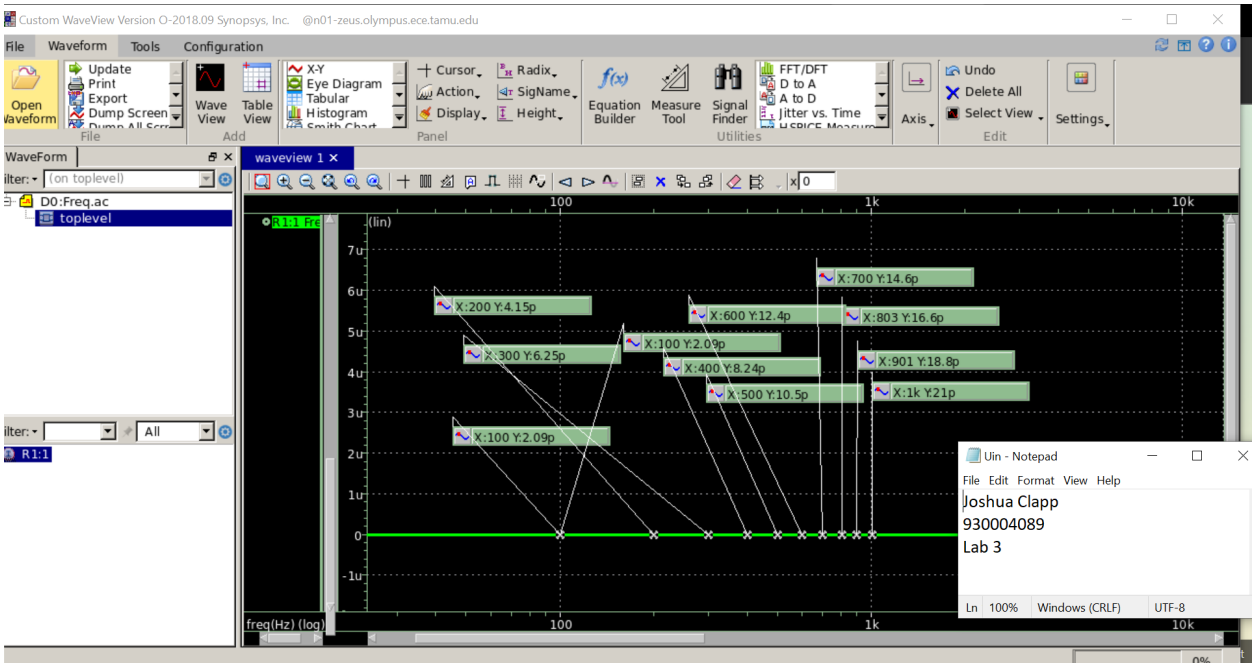
Joshua Clapp

Inverter



AC Inverter



Inverter				C= I / 2*pi*f	
C (fF)	**Delay R (ps)**	**Delay F (ps)**	**Error (%)**	**Y (uA)**	**X (MHz)**
1	-26.4	-43.8	39.73%	2.09	100
2	-34.2	-50.7	32.54%	4.15	200
5	-53	-69.2	23.41%	6.25	300
10	-77.7	-92.7	16.18%	8.24	400
15	-98.3	-111	11.44%	10.5	500
20	-116	-129	10.08%	12.4	600
25	-134	-147	8.84%	14.6	700
30	-152	-165	7.88%	16.6	800
40	-189	-203	6.90%	18.8	900
50	-225	-238	5.46%	21	1000
60	-260	-275	5.45%	**Average**	**Average**
70	-296	-311	4.82%	13.215	550
80	-334	-351	4.84%		
90	-370	-387	4.39%	**Sink Capacitance (F)**	
100	-405	-421	3.80%	3.82E-15	

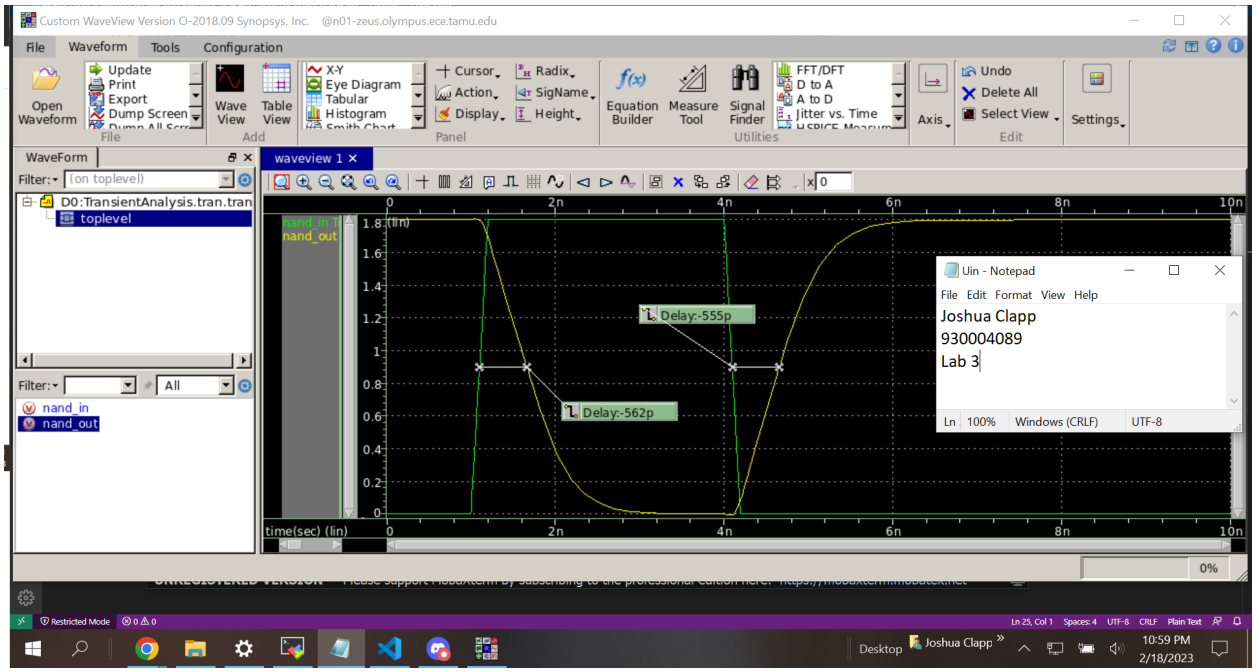
Inverter.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.6u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

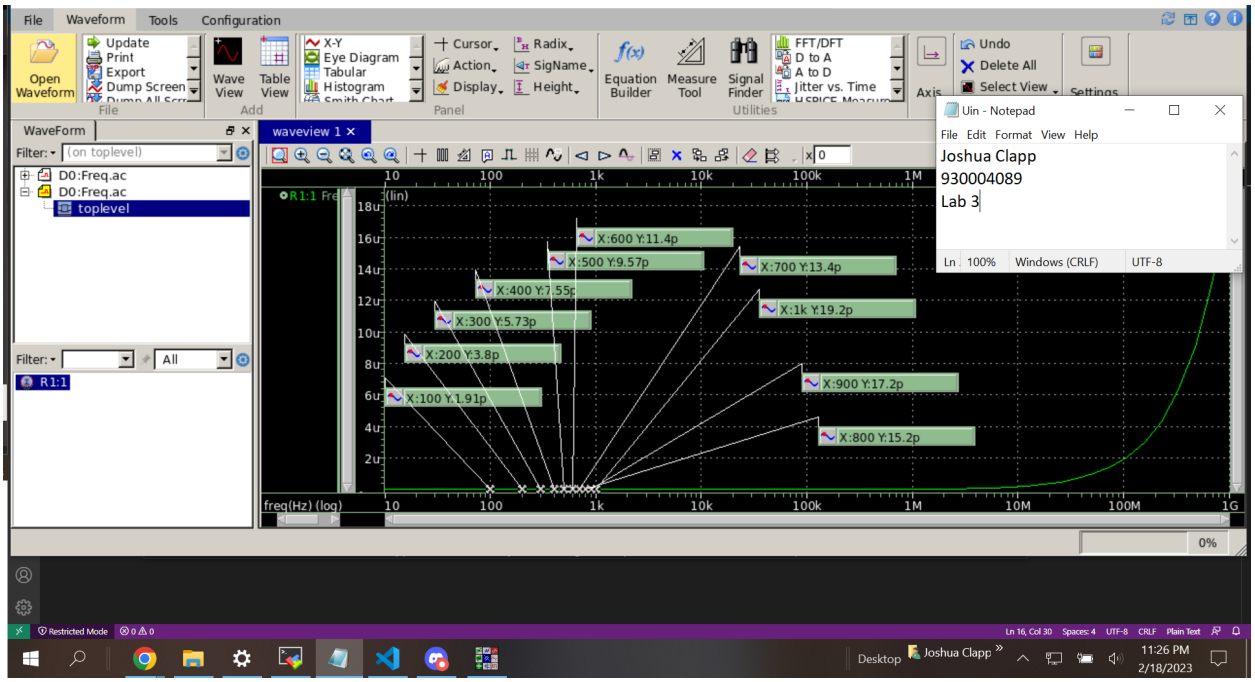
Simcap.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Nand Delay Waveform



Nand Ac



Nand				C= I / 2*pi*f	
C (fF)	**Delay R (ps)**	**Delay F (ps)**	**Error (%)**	**Y (uA)**	**X (MHz)**
1	-37.4	-54.4	31.25	1.91	100
2	-46.5	-63.1	26.30744849	3.8	200
5	-68.9	-83.9	17.8784267	5.73	300
10	-99.6	-111	10.27027027	7.55	400
15	-125	-135	7.407407407	9.57	500
20	-151	-160	5.625	11.4	600
25	-177	-184	3.804347826	13.4	700
30	-203	-209	2.870813397	15.2	800
40	-255	-259	1.544401544	17.2	900
50	-305	-310	1.612903226	19.2	1000
60	-357	-357	0	**Average**	**Average**
70	-410	-406	-0.9852216749	10.496	550
80	-460	-455	-1.098901099		
90	-510	-505	-0.9900990099	**Sink Cap**	
100	-562	-555	-1.261261261	**3.037x10^(-15)**	

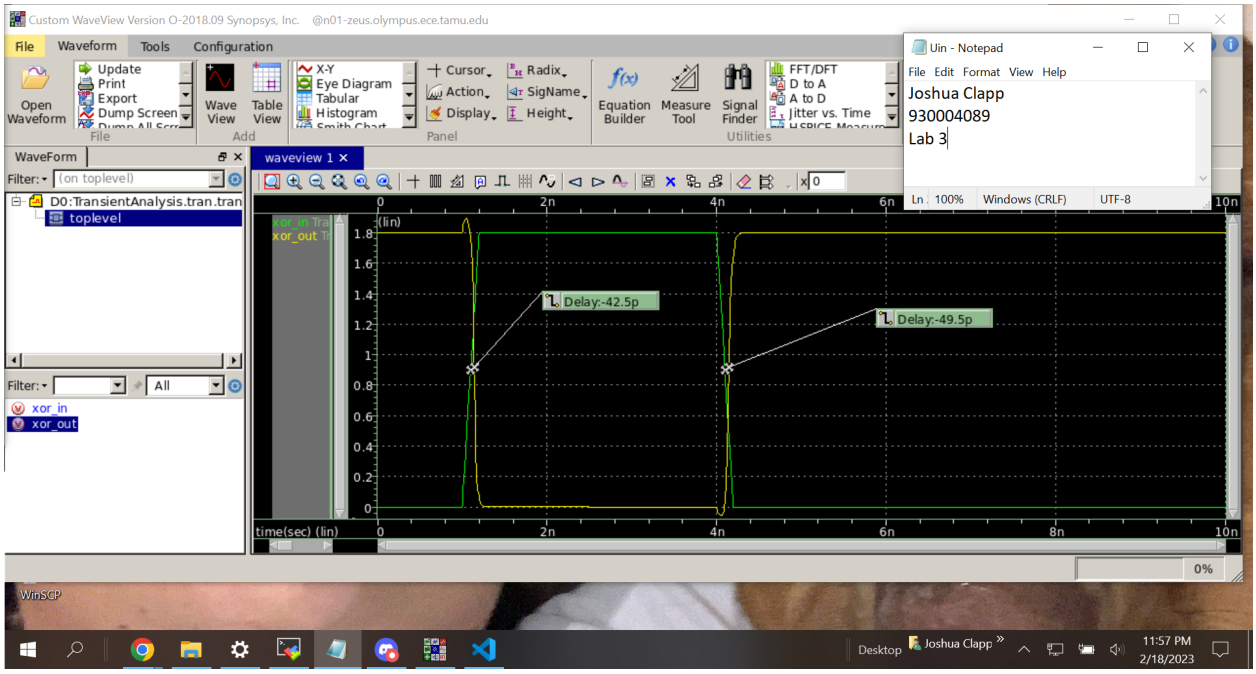
Nand_delay.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (nand_in 0) vsource dc=0 mag=1

R1 (nand_in nand_in1) resistor r=0

X1 (nand_in1 nand_out vdd gnd) nand wp=0.8u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

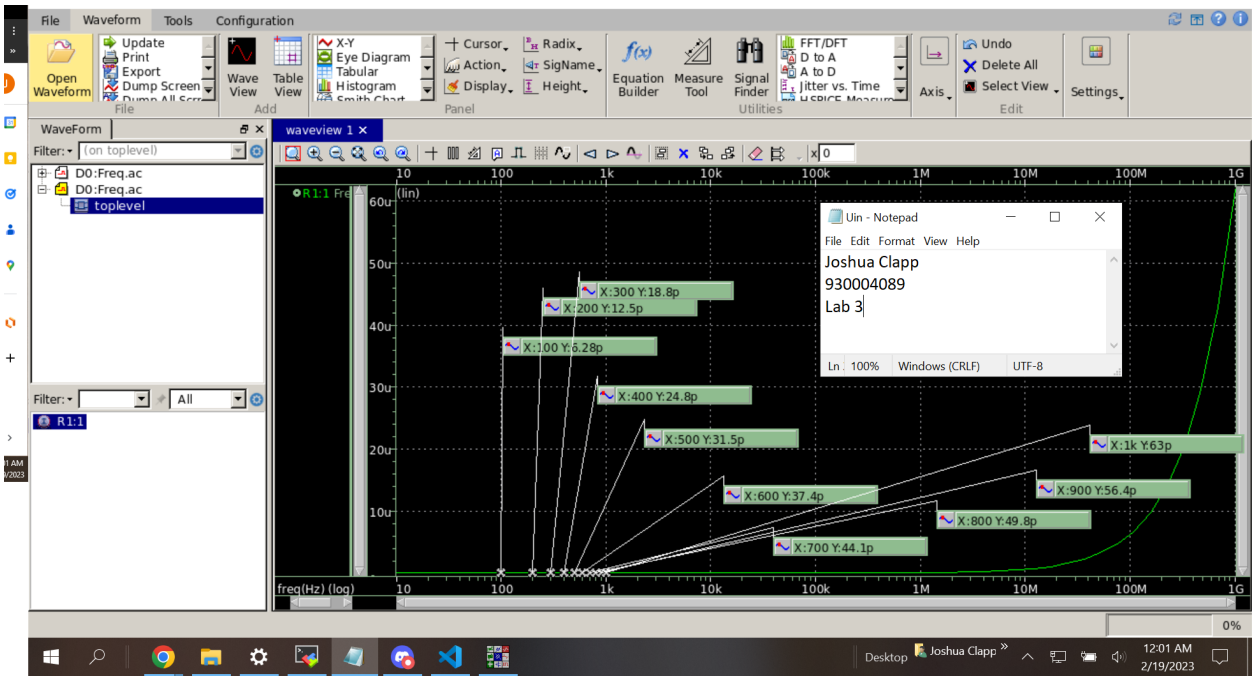
Simcap_nand

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (nand_in 0) vsource dc=0 mag=1

R1 (nand_in nand_in1) resistor r=0

X1 (nand_in1 nand_out vdd gnd) nand wp=0.8u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Xor waveform



Xor Ac



xor				C= I / 2*pi*f	
C (fF)	**Delay R (ps)**	**Delay F (ps)**	**Error (%)**	**Y (uA)**	**X (MHz)**
1	-42.5	-49.5	14.14141414	6.28	100
2	-49.1	-56	12.32142857	12.5	200
5	-67	-74.1	9.581646424	18.8	300
10	-94.8	-104	8.846153846	24.8	400
15	-121	-130	6.923076923	31.5	500
20	-147	-157	6.369426752	37.4	600
25	-174	-183	4.918032787	44.1	700
30	-200	-209	4.306220096	49.8	800
40	-252	-261	3.448275862	56.4	900
50	-304	-312	2.564102564	63	1000
60	-355	-364	2.472527473	**Average**	**Average**
70	-407	-418	2.631578947	34.458	550
80	-458	-469	2.345415778		
90	-510	-522	2.298850575	**Sink Cap**	
100	-562	-572	1.748251748	9.97x10^(-15)	

Xor_delay.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (xor_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

;X1 (IV_in IV_out vdd gnd) IV wp=0.6u lp=0.2u wn=0.3u ln=0.2u
X1 (xor_in xor_out vdd gnd) xor wp=1.5u lp=0.2u wn=0.4u ln=0.2u

;R1 (xor_out 1) resistor r=1
C1 (xor_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save xor_in xor_out
```

Xor_simcap.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (xor_in 0) vsource dc=0 mag=1

R1 (xor_in xor_in1) resistor r=0

X1 (xor_in1 xor_out vdd gnd) xor wp=1.5u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Cell18.spi

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
```

```
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV
subckt nand (input output VDD VSS)
      parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
      M1 output input VDD VDD tsmc18P w=wp l=lp
      M2 output VDD VDD VDD tsmc18P w=wp l=lp
      M3 output input C VSS tsmc18N w=wn l=ln
      M4 C VDD VSS VSS tsmc18N w=wn l=ln
ends nand
subckt xor (input output VDD VSS)
      parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
      M1 Aout input VDD VDD tsmc18P w=wp l=lp
      M2 Aout input VSS VSS tsmc18N w=wn l=ln
      M3 Bout VDD VDD VDD tsmc18P w=wp l=lp
      M4 Bout VDD VSS VSS tsmc18N w=wn l=ln
      M5 t1 VDD VDD VDD tsmc18P w=wp l=lp
      M6 output Aout t1 VDD tsmc18P w=wp l=lp
      M7 t2 Bout VDD VDD tsmc18P w=wp l=lp
      M8 output input t2 VDD tsmc18P w=wp l=lp
      M9 b1 Bout VSS VSS tsmc18N w=wn l=ln
      M10 output Aout b1 VSS tsmc18N w=wn l=ln
      M11 b2 VDD VSS VSS tsmc18N w=wn l=ln
      M12 output input b2 VSS tsmc18N w=wn l=ln
ends xor
```