Report Generated by Test Manager

Title: **Test**
Author: **Athira Varma J**
Date: **04-Feb-2019 13:26:45**

Test Environment

Platform: PCWIN64
MATLAB: (R2018b)

Summary

Name	Outcome	Duration (Seconds)
Results: 2019-Feb-03 15:48:42	30 ✓ 2 ✗	607
New Test Suite 1	30 ✓ 2 ✗	600
Init State	✓	17
FB_Select State	✓	20
Fetch State 1st Input and verify Addr output	✗	20
Fetch State 2nd Input	✓	19
Fetch State 3rd Input	✓	18
Execute State	✓	19
Write State 1st output	✓	19
Write State 2nd Output	✓	18
FB Done state	✓	17
Error in FB Select State	✓	18
Error in Fetch State	✓	17
Recoverable Error	✓	18
FB Select to FETCH State	✓	18
Non Recoverable Error	✗	17
Non Recoverable Error to INIT	✓	19
Error in Write State	✓	19
End of Sequence	✓	18
Task Done to INIT	✓	18
Error in LATCH_ADDR substate in Fetch State	✓	18
Error in MEM_WAIT substate in Fetch State	✓	19
Error in CTRL_HI SubState in Fetch State	✓	19

Error in CTRL_LO substate in Fetch State	✓	18
Error in INCREMENT_INST Substate in Fetch state	✓	18
Error in INST_WAIT Substate in Fetch state	✓	19
Error in CTRL_HI Substate in FB_EXECUTE state	✓	19
Error in CTRL_LO Substate in FB_EXECUTE state	✓	18
Error in LATCH_ADDR Substate in Write state	✓	18
Error in CTRL_HI Substate in Write state	✓	19
Error in CTRL_LO Substate in Write state	✓	21
Error in WRITE Substate in Write state	✓	23
Error in INCREMENT_INST Substate in Write state	✓	22
Error in INST_WAIT Substate in Write state	✓	20

Results: 2019-Feb-03 15:48:42

Result Type:	Result Set
Parent:	None
Start Time:	2019-Feb-03 15:48:42
End Time:	2019-Feb-03 15:58:49
Outcome:	Total: 32, Passed: 30, Failed: 2

Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Condition	MCDC	Execution
local_sequencer	Normal	61	99%	100%	NaN%	97%

Back to Report Summary

New Test Suite 1

Test Result Information

Result Type:	Test Suite Result
Parent:	Results: 2019-Feb-03 15:48:42
Start Time:	2019-Feb-03 15:48:49
End Time:	2019-Feb-03 15:58:49
Outcome:	Total: 32, Passed: 30, Failed: 2

Test Suite Information

Name: New Test Suite 1

Back to Report Summary

Init State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:48:49
End Time:	2019-Feb-03 15:49:06
Outcome:	Passed
Description:	

Verify that in Init state all the outputs task_done, inst_ptr, task_error, latch_addr, write, ctrl, abort and fb_select of local sequencer are reset to 0.
The instruction pointer should be reset to 0 to point to the first instruction.

Test Case Information

Name: Init State
Type: Baseline Test

Test Case Requirements

Description: INIT (local_sequencer_req#13)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	2946405130 1670660317 3481170102 1295358117
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:48:50
Simulation Stop Time:	2019-02-03 15:48:55
Platform:	PCWIN64

FB_Select State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:49:06
End Time:	2019-Feb-03 15:49:26
Outcome:	Passed
Description:	

Verify that with a trigger from global sequencer, the task execution is initiated.

Verify that the state transitions from INIT to FB_SELECT.
Verify that the function number register and start instruction pointer register are latched to the first instruction in the sequence

Verify that in the next cycle the instruction pointer increments..

Test Case Information

Name: FB_Select State
Type: Simulation Test

Test Case Requirements

Description: Transistions (local_sequencer_req#21)
Document: local_sequencer_req.slreqx
Description: FB_SELECT (local_sequencer_req#14)
Document: local_sequencer_req.slreqx
Description: Function Block Selection Service Provided (local_sequencer_req#33)
Document: local_sequencer_req.slreqx
Description: Trigger Service Received (local_sequencer_req#1)
Document: local_sequencer_req.slreqx
Description: Instruction Service Received (local_sequencer_req#2)
Document: local_sequencer_req.slreqx
Description: Function Number Register (local_sequencer_req#8)
Document: local_sequencer_req.slreqx
Description: Start Instruction Pointer Register (local_sequencer_req#9)
Document: local_sequencer_req.slreqx

Verify Result

Name
⊘ Test Assessment Block/Run:verify(task_done == 0)
⊘ Test Assessment Block/Run:verify(inst_ptr == 0)
⊘ Test Assessment Block/Run:verify(task_error == 0)
⊘ Test Assessment Block/Run:verify(latch_addr == 0)
⊘ Test Assessment Block/Run:verify(write == 0)
⊘ Test Assessment Block/Run:verify(ctrl == 0)
⊘ Test Assessment Block/Run:verify(abort == 0)
⊘ Test Assessment Block/Run:verify(fb_select == 0)
✓ Test Assessment Block/step2:verify(task_done == 0)
✓ Test Assessment Block/step2:verify(inst_ptr == 0)
✓ Test Assessment Block/step2:verify(task_error == 0)
✓ Test Assessment Block/step2:verify(latch_addr == 0)
✓ Test Assessment Block/step2:verify(write == 0)
✓ Test Assessment Block/step2:verify(ctrl == 0)
✓ Test Assessment Block/step2:verify(abort == 0)
✓ Test Assessment Block/step2:verify(fb_select == 42)
✓ Test Assessment Block/step3:verify(task_done == 0)
✓ Test Assessment Block/step3:verify(inst_ptr == 1)
✓ Test Assessment Block/step3:verify(task_error == 0)
✓ Test Assessment Block/step3:verify(latch_addr == 0)
✓ Test Assessment Block/step3:verify(write == 0)
✓ Test Assessment Block/step3:verify(ctrl == 0)
✓ Test Assessment Block/step3:verify(abort == 0)
✓ Test Assessment Block/step3:verify(fb_select == 42)
⊘ Test Assessment Block/step4:verify(task_done == 0)
⊘ Test Assessment Block/step4:verify(inst_ptr == 1)
⊘ Test Assessment Block/step4:verify(task_error == 0)
⊘ Test Assessment Block/step4:verify(latch_addr == 1)
⊘ Test Assessment Block/step4:verify(int32(addr) == 32)
⊘ Test Assessment Block/step4:verify(write == 0)
⊘ Test Assessment Block/step4:verify(ctrl == 0)
⊘ Test Assessment Block/step4:verify(abort == 0)
⊘ Test Assessment Block/step4:verify(fb_select == 42)
⊘ Test Assessment Block/step5:verify(task_done == 0)
⊘ Test Assessment Block/step5:verify(inst_ptr == 1)
⊘ Test Assessment Block/step5:verify(task_error == 0)
⊘ Test Assessment Block/step5:verify(latch_addr == 0)
⊘ Test Assessment Block/step5:verify(write == 0)
⊘ Test Assessment Block/step5:verify(ctrl == 0)
⊘ Test Assessment Block/step5:verify(abort == 0)
⊘ Test Assessment Block/step5:verify(fb_select == 42)
⊘ Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	2946405130 1670660317 3481170102 1295358117
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:49:10
Simulation Stop Time:	2019-02-03 15:49:14
Platform:	PCWIN64

Fetch State 1st Input and verify Addr output

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:49:26
End Time:	2019-Feb-03 15:49:46
Outcome:	Failed
Cause of Failure:	Failed criteria: Verification
Description:	

Verify that the state switches to Fetch automatically.
Verify that there is one cycle of wait state for data to be available to function blocks from task memories.

Verify that in the next cycle a ctrl pulse is sent to function blocks to begin execution.

Verify that after 2 cycles the instruction pointer is incremented.

Test Case Information

Name:	Fetch State 1st Input and verify Addr output
Type:	Baseline Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#22)
Document:	local_sequencer_req.slreqx
Description:	Conversion of Data Input (local_sequencer_req#34)
Document:	local_sequencer_req.slreqx
Description:	Current Address Register (local_sequencer_req#11)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	20
Checksum:	2270349598 670375184 1745057116 3272137456
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:49:30
Simulation Stop Time:	2019-02-03 15:49:35
Platform:	PCWIN64

Fetch State 2nd Input

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:49:46
End Time:	2019-Feb-03 15:50:05
Outcome:	Passed
Description:	

Verify that the state remains in Fetch if the super state (upper 4 bits of Code in status signal) has not changed but the code data bits 22 through 27 has been incremented once indicating a super state iteration.
Verify that the 2nd input fetch address in the instruction sequence is latched on to the addr output.

Verify that there is one cycle of wait state for data to be available to function blocks from task memories.

Verify that a ctrl pulse is sent to function blocks to begin execution.

Verify that the instruction pointer is incremented.

Test Case Information

Name:	Fetch State 2nd Input
Type:	Baseline Test

Test Case Requirements

Description:	FETCH (local_sequencer_req#15)
Document:	local_sequencer_req.slreqx
Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx
Description:	Task Memory Control Service Provided (local_sequencer_req#31)
Document:	local_sequencer_req.slreqx
Description:	Super State Iteration Detection (local_sequencer_req#4)
Document:	local_sequencer_req.slreqx
Description:	Function Block Status Service Received (local_sequencer_req#3)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	27
Checksum:	4144241666 3890879107 3895079110 4102482403
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:49:50
Simulation Stop Time:	2019-02-03 15:49:55
Platform:	PCWIN64

Fetch State 3rd Input

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:50:05
End Time:	2019-Feb-03 15:50:23
Outcome:	Passed
Description:	

Verify that the state remains in Fetch if the super state (upper 4 bits of Code in status signal) has not changed but the code data bits 22 through 27 has been incremented once indicating a super state iteration.
Verify that the 3rd input fetch address in the instruction sequence is latched on to the addr output.

Verify that there is one cycle of wait state for data to be available to function blocks from task memories.

Verify that a ctrl pulse is sent to function blocks to begin execution.

Verify that the instruction pointer is incremented.

Verify that the state stays in Fetch until the super state change from global sequencer is detected.

Test Case Information

Name: Fetch State 3rd Input
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#23)
Document: local_sequencer_req.slreqx
Description: Instruction Pointer Service Provided (local_sequencer_req#32)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	35
Checksum:	842347142 1364152625 118353973 750445995
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:50:08
Simulation Stop Time:	2019-02-03 15:50:14
Platform:	PCWIN64

Execute State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:50:23
End Time:	2019-Feb-03 15:50:42
Outcome:	Passed
Description:	

Verify that the state changes to Execute if the super state (upper 4 bits of Code in status signal) has changed indicating next state.

Verify that a ctrl pulse is sent to the function blocks for execution.

Test Case Information

Name: Execute State
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#23)
Document: local_sequencer_req.slreqx
Description: FB_EXECUTE (local_sequencer_req#16)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	40
Checksum:	2155861879 2434011949 3506385149 1882827719
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:50:27
Simulation Stop Time:	2019-02-03 15:50:32
Platform:	PCWIN64

Write State 1st output

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:50:42
End Time:	2019-Feb-03 15:51:01
Outcome:	Passed
Description:	

Verify that the state changes to Write if the super state (upper 4 bits of Code in status signal) has changed indicating next state.

Verify that the output address in the instruction sequence is latched on to the addr output.

Verify that a ctrl pulse is sent to function blocks to begin execution.

Verify that the write output is set high to allow the function block to write the result to the current address.

Verify that the instruction pointer is incremented after one cycle.

Test Case Information

Name: Write State 1st output
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#24)
Document: local_sequencer_req.slreqx
Description: Instruction Counter (local_sequencer_req#10)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	45
Checksum:	3900731963 119908724 348568191 1213259021
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:50:46
Simulation Stop Time:	2019-02-03 15:50:51
Platform:	PCWIN64

Write State 2nd Output

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:51:01
End Time:	2019-Feb-03 15:51:19
Outcome:	Passed
Description:	

Verify that the state remains in Write if the super state (upper 4 bits of Code in status signal) has not changed but the code data bits 22 through 27 has been incremented once indicating a super state iteration.
Verify that the 2nd output address in the instruction sequence is latched on to the addr output.

Verify that a ctrl pulse is sent to function blocks to begin execution.

Verify that the write output is set high to allow the function block to write the result to the current address.

Verify that the instruction pointer is incremented.

Test Case Information

Name: Write State 2nd Output
Type: Baseline Test

Test Case Requirements

Description: WRITE (local_sequencer_req#17)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	50
Checksum:	3997566239 2242021523 3449075664 2081074619
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:51:04
Simulation Stop Time:	2019-02-03 15:51:09
Platform:	PCWIN64

FB Done state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:51:19
End Time:	2019-Feb-03 15:51:36
Outcome:	Passed
Description:	

Verify that the state changes to FB_DONE if the super state (upper 4 bits of Code in status signal) has changed indicating next state.

Verify that a ctrl pulse is sent to function blocks to progress its state.

Verify that an Error while in FB_Done state does not cause it the local sequencer to move to the ERROR state.

Test Case Information

Name:	FB Done state
Type:	Baseline Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx
Description:	FB_DONE (local_sequencer_req#18)
Document:	local_sequencer_req.slreqx
Description:	Super State Change Detection (local_sequencer_req#5)
Document:	local_sequencer_req.slreqx
Description:	Function Block Status Service Received (local_sequencer_req#3)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	60
Checksum:	3957168329 1543921322 1911777152 1761218249
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:51:22
Simulation Stop Time:	2019-02-03 15:51:27
Platform:	PCWIN64

Error in FB Select State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:51:36
End Time:	2019-Feb-03 15:51:54
Outcome:	Passed
Description:	

Verify that the state changes to FB_SELECT if the super state (upper 4 bits of Code in status signal) has changed indicating next state.

Verify that the function number register and start instruction pointer register are latched to the 2nd function block instruction in the sequence.

Verify that the instruction pointer is incremented.

Verify that an Error while in FB_SELECT state does not cause it the local sequencer to move to the ERROR state.

Test Case Information

Name: Error in FB Select State
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#26)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	60
Checksum:	3957168329 1543921322 1911777152 1761218249
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:51:40
Simulation Stop Time:	2019-02-03 15:51:44
Platform:	PCWIN64

Error in Fetch State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:51:54
End Time:	2019-Feb-03 15:52:11
Outcome:	Passed
Description:	

Verify that the state switches to Fetch automatically.

Verify that the fetch address in the instruction sequence is latched on the addr output.

Verify that the state switches to ERROR if the Error signal in Status input is true.
Verify that a ctrl pulse is sent to function blocks.
Verify that abort and Task_Error output signals are set to false if the lower 22 bits of the Code in Status signal indicate a recoverable error.

Test Case Information

Name: Error in Fetch State
Type: Baseline Test

Test Case Requirements

Description: ERROR (local_sequencer_req#20)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	65
Checksum:	799440849 4060682207 132053812 1287153246
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:51:57
Simulation Stop Time:	2019-02-03 15:52:02
Platform:	PCWIN64

Recoverable Error

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:52:11
End Time:	2019-Feb-03 15:52:29
Outcome:	Passed
Description:	

If the lower 22 bits of the Code in Status signal indicate a recoverable error, verify that the state changes from ERROR to FB_SELECT.

With a recoverable error verify that the instruction pointer is loaded with the value stored in the start instruction pointer register.

Verify that the instruction pointer is incremented.

Test Case Information

Name:	Recoverable Error
Type:	Baseline Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#28)
Document:	local_sequencer_req.slreqx
Description:	Error Recovery Determination (local_sequencer_req#6)
Document:	local_sequencer_req.slreqx
Description:	Function Block Status Service Received (local_sequencer_req#3)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	70
Checksum:	2752943682 1142429451 1244692139 1047519825
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:52:15
Simulation Stop Time:	2019-02-03 15:52:20
Platform:	PCWIN64

FB Select to FETCH State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:52:29
End Time:	2019-Feb-03 15:52:47
Outcome:	Passed
Description:	

Verify that the state switches to Fetch automatically.

Verify that the fetch address in the instruction sequence is latched on the addr output.
Verify that there is one cycle of wait state for data to be available to function blocks from task memories.
Verify that in the next cycle a ctrl pulse is sent to function blocks to begin execution.
Verify that after 2 cycles the instruction pointer is incremented.

Test Case Information

Name: FB Select to FETCH State
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#22)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	70
Checksum:	2752943682 1142429451 1244692139 1047519825
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:52:33
Simulation Stop Time:	2019-02-03 15:52:37
Platform:	PCWIN64

Non Recoverable Error

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:52:47
End Time:	2019-Feb-03 15:53:04
Outcome:	Failed
Cause of Failure:	Failed criteria: Verification
Description:	

Verify that the state changes to Execute if the super state (upper 4 bits of Error Code in status signal) has changed indicating next state.
Verify that a ctrl pulse is sent to the function blocks for execution.

Verify that the state switches to ERROR if the Error signal in Status input is true.
If the lower 22 bits of the Code in Status signal indicate a non recoverable error, verify that a ctrl and abort signals are pulsed for one cycle.
Verify that the Task_Error output is set to true until the Trigger goes low.

Test Case Information

Name:	Non Recoverable Error
Type:	Baseline Test

Test Case Requirements

Description:	ERROR (local_sequencer_req#20)
Document:	local_sequencer_req.slreqx
Description:	Error Signal Service Provided (local_sequencer_req#29)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	70
Checksum:	2752943682 1142429451 1244692139 1047519825
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:52:50
Simulation Stop Time:	2019-02-03 15:52:55
Platform:	PCWIN64

Non Recoverable Error to INIT

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:53:04
End Time:	2019-Feb-03 15:53:23
Outcome:	Passed
Description:	

Verify that the state transitions from ERROR state to INIT if the error is not recoverable and the trigger from the global sequencer is low.

Verify if in Init state all the outputs are reset to 0.
The instruction pointer should be reset to 0 to point to the first instruction in the sequence

Test Case Information

Name: Non Recoverable Error to INIT
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#28)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	70
Checksum:	2752943682 1142429451 1244692139 1047519825
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:53:08
Simulation Stop Time:	2019-02-03 15:53:13
Platform:	PCWIN64

Error in Write State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:53:23
End Time:	2019-Feb-03 15:53:42
Outcome:	Passed
Description:	

Verify that with a trigger from global sequencer, the task execution is initiated. The state transitions from INIT to FB_SELECT.

Verify that the function number register and start instruction pointer register are latched to the first instruction in the sequence.

Verify that the instruction pointer increments.

Verify that the write state is entered.

Verify that Error state is entered from write state if error is detected.

Test Case Information

Name:	Error in Write State
Type:	Baseline Test

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	100
Checksum:	2093908169 3179825545 579071532 4249762891
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:53:27
Simulation Stop Time:	2019-02-03 15:53:32
Platform:	PCWIN64

End of Sequence

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:53:42
End Time:	2019-Feb-03 15:54:00
Outcome:	Passed
Description:	

Verify that state moves to Task_Done from FB_Done state once function block signals a new state and EOF flag is the current instruction.

Verify that Task_Done output is set to TRUE while in the Task_Done state.

Test Case Information

Name: End of Sequence
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#26)
Document: local_sequencer_req.slreqx
Description: TASK_DONE (local_sequencer_req#19)
Document: local_sequencer_req.slreqx
Description: Task Done Service Provided (local_sequencer_req#30)
Document: local_sequencer_req.slreqx
Description: End of File Determination (local_sequencer_req#7)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:53:45
Simulation Stop Time:	2019-02-03 15:53:50
Platform:	PCWIN64

Task Done to INIT

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:54:00
End Time:	2019-Feb-03 15:54:18
Outcome:	Passed
Description:	

Verify that the state moves from Task_Done to INIT state once Trigger goes low.

Test Case Information

Name: Task Done to INIT
Type: Baseline Test

Test Case Requirements

Description: Transitions (local_sequencer_req#27)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	130
Checksum:	3561885442 3679184002 1957729918 2315183824
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:54:03
Simulation Stop Time:	2019-02-03 15:54:08
Platform:	PCWIN64

Error in LATCH_ADDR substate in Fetch State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:54:18
End Time:	2019-Feb-03 15:54:36
Outcome:	Passed
Description:	

Verify that Error state is entered from the LATCH_ADDR substate of Fetch state if Error is detected.

Test Case Information

Name:	Error in LATCH_ADDR substate in Fetch State
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	130
Checksum:	3561885442 3679184002 1957729918 2315183824
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:54:22
Simulation Stop Time:	2019-02-03 15:54:27
Platform:	PCWIN64

Error in MEM_WAIT substate in Fetch State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:54:36
End Time:	2019-Feb-03 15:54:55
Outcome:	Passed
Description:	

Verify that Error state is entered from the MEM_WAIT substate of Fetch state if Error is detected.

Test Case Information

Name:	Error in MEM_WAIT substate in Fetch State
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	150
Checksum:	1012164172 3728227656 1028335012 1189976733
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:54:40
Simulation Stop Time:	2019-02-03 15:54:45
Platform:	PCWIN64

Error in CTRL_HI SubState in Fetch State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:54:55
End Time:	2019-Feb-03 15:55:14
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_HI substate of Fetch state if Error is detected.

Test Case Information

Name: Error in CTRL_HI SubState in Fetch State
Type: Simulation Test

Test Case Requirements

Description: Transitions (local_sequencer_req#23)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:54:58
Simulation Stop Time:	2019-02-03 15:55:04
Platform:	PCWIN64

Error in CTRL_LO substate in Fetch State

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:55:14
End Time:	2019-Feb-03 15:55:32
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_LO substate of Fetch state if Error is detected.

Test Case Information

Name:	Error in CTRL_LO substate in Fetch State
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:55:17
Simulation Stop Time:	2019-02-03 15:55:22
Platform:	PCWIN64

Error in INCREMENT_INST Substate in Fetch state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:55:32
End Time:	2019-Feb-03 15:55:50
Outcome:	Passed
Description:	

Verify that Error state is entered from the INCREMENT_INST subtate of Fetch state if Error is detected.

Test Case Information

Name:	Error in INCREMENT_INST Substate in Fetch sta te
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:55:36
Simulation Stop Time:	2019-02-03 15:55:41
Platform:	PCWIN64

Error in INST_WAIT Substate in Fetch state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:55:50
End Time:	2019-Feb-03 15:56:09
Outcome:	Passed
Description:	

Verify that Error state is entered from the INST_WAIT substate of Fetch state if Error is detected.

Test Case Information

Name:	Error in INST_WAIT Substate in Fetch state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#23)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:55:54
Simulation Stop Time:	2019-02-03 15:55:59
Platform:	PCWIN64

Error in CTRL_HI Substate in FB_EXEC UTE state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:56:09
End Time:	2019-Feb-03 15:56:28
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_HI substate of FB_EXECUTE state if Error is detected.

Test Case Information

Name:	Error in CTRL_HI Substate in FB_EXECUTE state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#24)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:56:13
Simulation Stop Time:	2019-02-03 15:56:18
Platform:	PCWIN64

Error in CTRL_LO Substate in FB_EXEC UTE state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:56:28
End Time:	2019-Feb-03 15:56:46
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_LO substate of FB_EXECUTE state if Error is detected.

Test Case Information

Name:	Error in CTRL_LO Substate in FB_EXECUTE state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#24)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:56:31
Simulation Stop Time:	2019-02-03 15:56:36
Platform:	PCWIN64

Error in LATCH_ADDR Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:56:46
End Time:	2019-Feb-03 15:57:04
Outcome:	Passed
Description:	

Verify that Error state is entered from the LATCH_ADDR substate of Write state if Error is detected.

Test Case Information

Name:	Error in LATCH_ADDR Substate in Write state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:56:50
Simulation Stop Time:	2019-02-03 15:56:55
Platform:	PCWIN64

Error in CTRL_HI Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:57:04
End Time:	2019-Feb-03 15:57:23
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_HI substate of Write state if Error is detected.

Test Case Information

Name:	Error in CTRL_HI Substate in Write state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:57:08
Simulation Stop Time:	2019-02-03 15:57:13
Platform:	PCWIN64

Error in CTRL_LO Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:57:23
End Time:	2019-Feb-03 15:57:44
Outcome:	Passed
Description:	

Verify that Error state is entered from the CTRL_LO substate of Write state if Error is detected.

Test Case Information

Name:	Error in CTRL_LO Substate in Write state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:57:26
Simulation Stop Time:	2019-02-03 15:57:31
Platform:	PCWIN64

Error in WRITE Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:57:44
End Time:	2019-Feb-03 15:58:07
Outcome:	Passed
Description:	

Verify that Error state is entered from the WRITE substate of Write state if Error is detected.

Test Case Information

Name: Error in WRITE Substate in Write state
Type: Simulation Test

Test Case Requirements

Description: Transitions (local_sequencer_req#25)
Document: local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:57:48
Simulation Stop Time:	2019-02-03 15:57:53
Platform:	PCWIN64

Error in INCREMENT_INST Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:58:07
End Time:	2019-Feb-03 15:58:29
Outcome:	Passed
Description:	

Verify that Error state is entered from the INCREMENT_INST substate of Write state if Error is detected.

Test Case Information

Name:	Error in INCREMENT_INST Substate in Write state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:58:13
Simulation Stop Time:	2019-02-03 15:58:19
Platform:	PCWIN64

Error in INST_WAIT Substate in Write state

Test Result Information

Result Type:	Test Case Result
Parent:	New Test Suite 1
Start Time:	2019-Feb-03 15:58:29
End Time:	2019-Feb-03 15:58:49
Outcome:	Passed
Description:	

Verify that Error state is entered from the INST_WAIT substate of Write state if Error is detected.

Test Case Information

Name:	Error in INST_WAIT Substate in Write state
Type:	Simulation Test

Test Case Requirements

Description:	Transitions (local_sequencer_req#25)
Document:	local_sequencer_req.slreqx

Verify Result

Name
Test Assessment Block/Run:verify(task_done == 0)
Test Assessment Block/Run:verify(inst_ptr == 0)
Test Assessment Block/Run:verify(task_error == 0)
Test Assessment Block/Run:verify(latch_addr == 0)
Test Assessment Block/Run:verify(write == 0)
Test Assessment Block/Run:verify(ctrl == 0)
Test Assessment Block/Run:verify(abort == 0)
Test Assessment Block/Run:verify(fb_select == 0)
Test Assessment Block/step2:verify(task_done == 0)
Test Assessment Block/step2:verify(inst_ptr == 0)
Test Assessment Block/step2:verify(task_error == 0)
Test Assessment Block/step2:verify(latch_addr == 0)
Test Assessment Block/step2:verify(write == 0)
Test Assessment Block/step2:verify(ctrl == 0)
Test Assessment Block/step2:verify(abort == 0)
Test Assessment Block/step2:verify(fb_select == 42)
Test Assessment Block/step3:verify(task_done == 0)
Test Assessment Block/step3:verify(inst_ptr == 1)
Test Assessment Block/step3:verify(task_error == 0)
Test Assessment Block/step3:verify(latch_addr == 0)
Test Assessment Block/step3:verify(write == 0)
Test Assessment Block/step3:verify(ctrl == 0)
Test Assessment Block/step3:verify(abort == 0)
Test Assessment Block/step3:verify(fb_select == 42)
Test Assessment Block/step4:verify(task_done == 0)
Test Assessment Block/step4:verify(inst_ptr == 1)
Test Assessment Block/step4:verify(task_error == 0)
Test Assessment Block/step4:verify(latch_addr == 1)
Test Assessment Block/step4:verify(int32(addr) == 32)
Test Assessment Block/step4:verify(write == 0)
Test Assessment Block/step4:verify(ctrl == 0)
Test Assessment Block/step4:verify(abort == 0)
Test Assessment Block/step4:verify(fb_select == 42)
Test Assessment Block/step5:verify(task_done == 0)
Test Assessment Block/step5:verify(inst_ptr == 1)
Test Assessment Block/step5:verify(task_error == 0)
Test Assessment Block/step5:verify(latch_addr == 0)
Test Assessment Block/step5:verify(write == 0)
Test Assessment Block/step5:verify(ctrl == 0)
Test Assessment Block/step5:verify(abort == 0)
Test Assessment Block/step5:verify(fb_select == 42)
Test Assessment Block/step6:verify(task_done == 0)

Simulation

System Under Test Information

Model:	local_sequencer
Harness:	local_sequencer_Harness3
Harness Owner:	local_sequencer
Simulation Mode:	normal
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	140
Checksum:	1246428927 1032405156 113024743 3801906147
Simulink Version:	9.2
Model Version:	1.189
Model Author:	jayakumarav
Date:	Sun Feb 03 00:17:14 2019
User ID:	jayakumarav
Model Path:	C:\Users\jayakumarav\Documents\GitHub\SympleVerification\Local_Sequencer\local_sequencer.slx
Machine Name:	EGR-ELKS-05
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	1
Simulation Start Time:	2019-02-03 15:58:33
Simulation Stop Time:	2019-02-03 15:58:38
Platform:	PCWIN64