Coverage Report for FB_Controller

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Analysis Information

Model Information

Model version	1.49
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Harness information

Harness model(s)	FB_Controller_Harness_FbController
Harness model owner	FB_Controller

Simulation Optimization Options

Default parameter behavior	tunable
Block reduction	forced off
Conditional branch optimization	on

Coverage Options

Analyzed model	FB_Controller
Logic block short circuiting	off
MCDC mode	masking

Tests

Test#	Started execution	Ended execution

Test 1 08-Feb-2019 01:09:47 08-Feb-2019 01:12:33

Summary

Model Hierarchy/Complexity	Test 1							
		Decision		Condition		MCDC		Execution	
1. FB_Controller	40	60%		78%		40%		84%	
2. . . . counterSelector	2	100%		100%		NA		100%	
3. . . . edge_counter_input	9	50%		75%		50%		81%	
4. . . . . Triggered Subsystem	9	50%		60%		0%		79%	
5. . . . . HDL Counter	8	50%		33%		0%		78%	
6. . . . . Add_wrap	1	50%		NA		NA		75%	
7. . . . . Dir_logic		NA		50%		0%		100%	
8. . . . . Max_value		NA		0%		NA		0%	
9. . . . . Sub_wrap	1	0%		NA		NA		25%	
10. . . . edge_counter_output	9	50%		75%		50%		81%	
11. . . . . Triggered Subsystem	9	50%		60%		0%		79%	
12. . . . . HDL Counter	8	50%		33%		0%		78%	
13. . . . . Add_wrap	1	50%		NA		NA		75%	
14. . . . . Dir_logic		NA		50%		0%		100%	
15. . . . . Max_value		NA		0%		NA		0%	
16. . . . . Sub_wrap	1	0%		NA		NA		25%	
17. . . . errorCodeGeneratorFunction	3	100%		NA		NA		NA	
18. . . . . errorCodeGenerator	3	100%		NA		NA		NA	
19. . . . timeOutCounter	15	63%		79%		0%		87%	
20. . . . . HDL Counter	8	56%		50%		0%		85%	
21. . . . . Add_wrap	1	50%		NA		NA		75%	
22. . . . . Dir_logic		NA		50%		0%		100%	
23. . . . . Max_value		NA		50%		NA		100%	
24. . . . . Sub_wrap	1	0%		NA		NA		25%	
25. . . . . S-R Flip-Flop	7	75%		100%		NA		100%	

Details

1. Model "FB_Controller"

Child Systems: counterSelector, edge_counter_input, edge_counter_output, errorCodeGeneratorFunction, timeOutCounter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	40
Condition	NA	78% (39/50) condition outcomes
Decision	NA	60% (38/63) decision outcomes
MCDC	NA	40% (4/10) conditions reversed the outcome
Execution	NA	84% (85/101) objective outcomes

Full Coverage

Model Object	Metric
ModelReference block "Model"	Execution

2. SubSystem block "counterSelector"

Justify or Exclude

Parent: /FB_Controller

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	2
Condition	NA	100% (4/4) condition outcomes
Decision	NA	100% (4/4) decision outcomes
Execution	NA	100% (7/7) objective outcomes

Full Coverage

Model Object	Metric
Switch block "Switch"	Decision, Execution
Switch block "Switch1"	Decision, Execution
RelationalOperator block "Relational Operator"	Condition, Execution
RelationalOperator block "Relational Operator1"	Condition, Execution
Constant block "Constant3"	Execution
Constant block "inputCode"	Execution
Constant block "outputCode"	Execution

3. SubSystem block "edge_counter_input"

Justify or Exclude

Parent: /FB_Controller
Child Systems: Triggered Subsystem

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	9
Condition	NA	75% (12/16) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	50% (2/4) conditions reversed the outcome
Execution	NA	81% (25/31) objective outcomes

Full Coverage

Model Object	Metric
Logic block "Logical Operator"	Condition, Execution
Logic block "Logical Operator1"	Condition, MCDC, Execution

4. SubSystem block "Triggered Subsystem"

Justify or Exclude

Parent: FB_Controller/edge_counter_input
Child Systems: HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	9
Condition	NA	60% (6/10) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	79% (23/29) objective outcomes

Full Coverage

Model Object	Metric
RelationalOperator block "Relational Operator"	Condition, Execution
RelationalOperator block "Relational Operator1"	Condition, Execution

5. SubSystem block "HDL Counter"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem
Child Systems: Add_wrap, Dir_logic, Max_value, Sub_wrap

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	8
Condition	NA	33% (2/6) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	78% (21/27) objective outcomes

Switch block "Switch_dir"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter
Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Switch block "Switch_load"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1346/1346
true (output is from 1st input port)	0/1346

Switch block "Switch_max"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	0% (0/2) decision outcomes
Execution	0% (0/1) objective outcomes

Decisions analyzed

logical trigger input	0%
false (output is from 3rd input port)	--
true (output is from 1st input port)	--

Switch block "Switch_type"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1

Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	0/36
true (output is from 1st input port)	36/36

Full Coverage

Model Object	Metric
Switch block "Switch_enb"	Decision, Execution
Switch block "Switch_reset"	Decision, Execution
DataTypeConversion block "DT_convert"	Execution
DataTypeConversion block "DT_convert1"	Execution
UnitDelay block "Count_reg"	Execution
Constant block "Free_running"	Execution
Constant block "From_value"	Execution
Constant block "Init_value"	Execution
Constant block "Step_value"	Execution
Constant block "const_dir"	Execution
Constant block "const_load"	Execution
Constant block "const_load_val"	Execution

6. SubSystem block "Add_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision	NA	50% (1/2) decision outcomes
Execution	NA	75% (3/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Add_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

trigger > threshold	50%
false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Add_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Sum block "Add"	Execution
Constant block "Mod_value"	Execution

7. SubSystem block "Dir_logic"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	50% (2/4) condition outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	100% (2/2) objective outcomes

Logic block "Logical Operator"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Dir_logic

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	50% (2/4) condition outcomes
MCDC	0% (0/2) conditions reversed the outcome
Execution	100% (1/1) objective outcomes

Conditions analyzed

Description	True	False
input port 1	13	0
input port 2	13	0

MC/DC analysis (combinations in parentheses did not occur)

Decision/Condition	True Out	False Out
expression for output		
input port 1	NA	NA
input port 2	NA	NA

Full Coverage

Model Object	Metric
Constant block "Pos_step"	Execution

8. SubSystem block "Max_value"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	0% (0/2) condition outcomes
Execution	NA	0% (0/1) objective outcomes

RelationalOperator block "Compare"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Max_value

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	0% (0/2) condition outcomes
Execution	0% (0/1) objective outcomes

Conditions analyzed

Description	True	False
input1 == input2	0	0

9. SubSystem block "Sub_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1

Decision	NA	0% (0/2) decision outcomes
Execution	NA	25% (1/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	0% (0/2) decision outcomes
Execution	0% (0/1) objective outcomes

Decisions analyzed

trigger >= threshold	0%
false (output is from 3rd input port)	--
true (output is from 1st input port)	--

Sum block "Add"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_input/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Constant block "Mod_value"	Execution

10. SubSystem block "edge_counter_output"

Justify or Exclude

Parent: /FB_Controller
Child Systems: Triggered Subsystem

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	9
Condition	NA	75% (12/16) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	50% (2/4) conditions reversed the outcome
Execution	NA	81% (25/31) objective outcomes

Full Coverage

Model Object	Metric
Logic block "Logical Operator"	Condition, Execution
Logic block "Logical Operator1"	Condition, MCDC, Execution

11. SubSystem block "Triggered Subsystem"

Justify or Exclude

Parent: FB_Controller/edge_counter_output
Child Systems: HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	9
Condition	NA	60% (6/10) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	79% (23/29) objective outcomes

Full Coverage

Model Object	Metric
RelationalOperator block "Relational Operator"	Condition, Execution
RelationalOperator block "Relational Operator1"	Condition, Execution

12. SubSystem block "HDL Counter"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem
Child Systems: Add_wrap, Dir_logic, Max_value, Sub_wrap

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	8
Condition	NA	33% (2/6) condition outcomes
Decision	NA	50% (8/16) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	78% (21/27) objective outcomes

Switch block "Switch_dir"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Switch block "Switch_load"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1346/1346
true (output is from 1st input port)	0/1346

Switch block "Switch_max"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	0% (0/2) decision outcomes
Execution	0% (0/1) objective outcomes

Decisions analyzed

logical trigger input	0%
false (output is from 3rd input port)	--

true (output is from 1st input port)	--

Switch block "Switch_type"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	0/9
true (output is from 1st input port)	9/9

Full Coverage

Model Object	Metric
Switch block "Switch_enb"	Decision, Execution
Switch block "Switch_reset"	Decision, Execution
DataTypeConversion block "DT_convert"	Execution
DataTypeConversion block "DT_convert1"	Execution
UnitDelay block "Count_reg"	Execution
Constant block "Free_running"	Execution
Constant block "From_value"	Execution
Constant block "Init_value"	Execution
Constant block "Step_value"	Execution
Constant block "const_dir"	Execution
Constant block "const_load"	Execution
Constant block "const_load_val"	Execution

13. SubSystem block "Add_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision	NA	50% (1/2) decision outcomes
Execution	NA	75% (3/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Add_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

trigger > threshold	50%
false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Add_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Sum block "Add"	Execution
Constant block "Mod_value"	Execution

14. SubSystem block "Dir_logic"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	50% (2/4) condition outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	100% (2/2) objective outcomes

Logic block "Logical Operator"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Dir_logic

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	50% (2/4) condition outcomes
MCDC	0% (0/2) conditions reversed the outcome
Execution	100% (1/1) objective outcomes

Conditions analyzed

Description	True	False
input port 1	13	0
input port 2	13	0

MC/DC analysis (combinations in parentheses did not occur)

Decision/Condition	True Out	False Out
expression for output		
input port 1	NA	NA
input port 2	NA	NA

Full Coverage

Model Object	Metric
Constant block "Pos_step"	Execution

15. SubSystem block "Max_value"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	0% (0/2) condition outcomes
Execution	NA	0% (0/1) objective outcomes

RelationalOperator block "Compare"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Max_value

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	0% (0/2) condition outcomes
Execution	0% (0/1) objective outcomes

Conditions analyzed

Description	True	False

input1 == input2	0	0

16. SubSystem block "Sub_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision	NA	0% (0/2) decision outcomes
Execution	NA	25% (1/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	0% (0/2) decision outcomes
Execution	0% (0/1) objective outcomes

Decisions analyzed

trigger >= threshold	0%
false (output is from 3rd input port)	--
true (output is from 1st input port)	--

Sum block "Add"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/edge_counter_output/Triggered Subsystem/HDL Counter/Sub_wrap

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Constant block "Mod_value"	Execution

17. SubSystem block "errorCodeGeneratorFunction"

Justify or Exclude

Parent: /FB_Controller

Child Systems: errorCodeGenerator

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	3
Decision	NA	100% (3/3) decision outcomes

18. MATLAB Function "errorCodeGenerator"

Justify or Exclude

Parent: FB_Controller/errorCodeGeneratorFunction

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	3

Decision	NA	100% (3/3) decision outcomes

Full Coverage

Model Object	Metric
MATLAB Function "fcn"	Decision

19. SubSystem block "timeOutCounter"

Justify or Exclude

Parent: /FB_Controller
Child Systems: HDL Counter, S-R Flip-Flop

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	15
Condition	NA	79% (11/14) condition outcomes
Decision	NA	63% (15/24) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	87% (27/31) objective outcomes

Full Coverage

Model Object	Metric
RelationalOperator block "Relational Operator"	Condition, Execution
Constant block "Constant3"	Execution

20. SubSystem block "HDL Counter"

Justify or Exclude

Parent: FB_Controller/timeOutCounter
Child Systems: Add_wrap, Dir_logic, Max_value, Sub_wrap

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	8
Condition	NA	50% (3/6) condition outcomes

Decision	NA	56% (9/16) decision outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	85% (23/27) objective outcomes

Switch block "Switch_dir"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Switch block "Switch_load"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1666/1666
true (output is from 1st input port)	0/1666

Switch block "Switch_max"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1125/1125
true (output is from 1st input port)	0/1125

Switch block "Switch_type"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	1125/1125
true (output is from 1st input port)	0/1125

Full Coverage

Model Object	Metric

Switch block "Switch_enb"	Decision, Execution
Switch block "Switch_reset"	Decision, Execution
DataTypeConversion block "DT_convert"	Execution
DataTypeConversion block "DT_convert1"	Execution
UnitDelay block "Count_reg"	Execution
Constant block "Free_running"	Execution
Constant block "From_value"	Execution
Constant block "Init_value"	Execution
Constant block "Step_value"	Execution
Constant block "const_dir"	Execution
Constant block "const_load"	Execution
Constant block "const_load_val"	Execution

21. SubSystem block "Add_wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision	NA	50% (1/2) decision outcomes
Execution	NA	75% (3/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Add_wrap

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

trigger > threshold	50%

false (output is from 3rd input port)	1683/1683
true (output is from 1st input port)	0/1683

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Add_wrap

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Sum block "Add"	Execution
Constant block "Mod_value"	Execution

22. SubSystem block "Dir_logic"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	50% (2/4) condition outcomes
MCDC	NA	0% (0/2) conditions reversed the outcome
Execution	NA	100% (2/2) objective outcomes

Logic block "Logical Operator"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Dir_logic

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	50% (2/4) condition outcomes
MCDC	0% (0/2) conditions reversed the outcome
Execution	100% (1/1) objective outcomes

Conditions analyzed

Description	True	False
input port 1	13	0
input port 2	13	0

MC/DC analysis (combinations in parentheses did not occur)

Decision/Condition	True Out	False Out
expression for output		
input port 1	NA	NA
input port 2	NA	NA

Full Coverage

Model Object	Metric
Constant block "Pos_step"	Execution

23. SubSystem block "Max_value"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	50% (1/2) condition outcomes
Execution	NA	100% (1/1) objective outcomes

RelationalOperator block "Compare"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Max_value

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	0
Condition	50% (1/2) condition outcomes
Execution	100% (1/1) objective outcomes

Conditions analyzed

Description	True	False
input1 == input2	0	1125

24. SubSystem block "Sub_wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision	NA	0% (0/2) decision outcomes
Execution	NA	25% (1/4) objective outcomes

Switch block "Switch_wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Sub_wrap

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	1
Decision	0% (0/2) decision outcomes
Execution	0% (0/1) objective outcomes

Decisions analyzed

trigger >= threshold	0%

false (output is from 3rd input port)	-- 
true (output is from 1st input port)	-- 

Sum block "Add"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Sub_wrap

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Sum block "Wrap"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/HDL Counter/Sub_wrap

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric
Constant block "Mod_value"	Execution

25. SubSystem block "S-R Flip-Flop"

Justify or Exclude

Parent: FB_Controller/timeOutCounter

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	7

Condition	NA	100% (6/6) condition outcomes
Decision	NA	75% (6/8) decision outcomes
Execution	NA	100% (2/2) objective outcomes

CombinatorialLogic block "Logic"

Justify or Exclude

Parent: FB_Controller/timeOutCounter/S-R Flip-Flop

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	7
Condition	100% (6/6) condition outcomes
Decision	75% (6/8) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

integer index value	75%
calculated to 0 based on inputs FFF (output row 1)	541/1683
calculated to 1 based on inputs FFT (output row 2)	960/1683
calculated to 2 based on inputs FTF (output row 3)	13/1683
calculated to 3 based on inputs FTT (output row 4)	4/1683
calculated to 4 based on inputs TFF (output row 5)	12/1683
calculated to 5 based on inputs TFT (output row 6)	153/1683
calculated to 6 based on inputs TTF (output row 7)	0/1683
calculated to 7 based on inputs TTT (output row 8)	0/1683

Full Coverage

Model Object	Metric
Memory block "Memory"	Execution