Report Generated by Test Manager

Title: Test

Author: Athira Varma J

Date: 07-Jan-2019 15:00:31

Test Environment

Platform: PCWIN64 MATLAB: (R2018b)

Summary

Name	Outcome	Duration (Seconds)
New Test Suite 1	5 🗷 1😵	91
New Test Case 1	Ø	25
New Test Case 2	Ø	15
New Test Case 3	•	12
New Test Case 4	8	14
New Test Case 5	•	13
New Test Case 6	•	12

New Test Suite 1

Test Result Information

Result Type: Test Suite Result

Parent: None

Start Time: 2019-Jan-07 14:54:11 End Time: 2019-Jan-07 14:55:42

Outcome: Total: 6, Passed: 5, Failed: 1

Test Suite Information

Name: New Test Suite 1

Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Condition	MCDC	Execution
FBFunctions/BSL_DUPLEX	Normal	28	71%	96%	88%	98%

Back to Report Summary

New Test Case 1

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:54:11
End Time: 2019-Jan-07 14:54:36

Outcome: Passed

Test Case Information

Name: New Test Case 1
Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
Test Sequence2/step_1:verify(state_error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
Test Sequence2/step_42:verify(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
✓ Test Sequence2/step_3:verify(dataOut == 0) — = — = — = — — — — — — — — — — — — — —
✓ Test Sequence2/step_3:verify(state_error == 0) ————————————————————————————————————
✓ Test Sequence2/step_3:verify(executed == 1) — — — — — — — — — — — — — — — — — — —
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
Test Sequence2/step_4:verify(executed == 1)
Test Sequence2/step_5:verify(numInputs == 2)
Test Sequence2/step_5:verify(numOutputs == 2)
Test Sequence2/step_5:verify(fb_error_code == 0)
Test Sequence2/step_5:verify(dataOut == 0)
Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
Test Sequence2/step_6:verify(numInputs == 2)
Test Sequence2/step_6:verify(numOutputs == 2)
Test Sequence2/step_6:verify(fb_error_code == 0)
Test Sequence2/step_6:verify(dataOut == 67108864)
Test Sequence2/step_6:verify(state_error == 0)
Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

New Test Case 2

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:54:36
End Time: 2019-Jan-07 14:54:51

Outcome: Passed

Test Case Information

Name: New Test Case 2 Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
✓ Test Seguence2/sten 1:verify(state error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
✓ Test Seguence2/sten 42:verifv(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
Test Sequence2/step_3:verify(dataOut == 0)
Test Sequence2/step_3:verify(state_error == 0)
Test Sequence2/step_3:verify(executed == 1)
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
O Test Sequence2/step_4:verify(executed == 1)
O Test Sequence2/step_5:verify(numInputs == 2)
O Test Sequence2/step_5:verify(numOutputs == 2)
Test Sequence2/step_5:verify(fb_error_code == 0)
O Test Sequence2/step_5:verify(dataOut == 0)
Oracle Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
O Test Sequence2/step_6:verify(numInputs == 2)
O Test Sequence2/step_6:verify(numOutputs == 2)
O Test Sequence2/step_6:verify(fb_error_code == 0)
O Test Sequence2/step_6:verify(dataOut == 67108864)
O Test Sequence2/step_6:verify(state_error == 0)
✓ Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

New Test Case 3

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:54:51
End Time: 2019-Jan-07 14:55:03

Outcome: Passed

Test Case Information

Name: New Test Case 3
Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
✓ Test Seguence2/sten 1:verify(state error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
✓ Test Seguence2/sten 42:verifv(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
Test Sequence2/step_3:verify(dataOut == 0)
Test Sequence2/step_3:verify(state_error == 0)
Test Sequence2/step_3:verify(executed == 1)
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
O Test Sequence2/step_4:verify(executed == 1)
O Test Sequence2/step_5:verify(numInputs == 2)
O Test Sequence2/step_5:verify(numOutputs == 2)
Test Sequence2/step_5:verify(fb_error_code == 0)
O Test Sequence2/step_5:verify(dataOut == 0)
Oracle Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
O Test Sequence2/step_6:verify(numInputs == 2)
O Test Sequence2/step_6:verify(numOutputs == 2)
Test Sequence2/step_6:verify(fb_error_code == 0)
O Test Sequence2/step_6:verify(dataOut == 67108864)
O Test Sequence2/step_6:verify(state_error == 0)
✓ Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration 1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

New Test Case 4

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:55:03
End Time: 2019-Jan-07 14:55:17

Outcome: Failed

Cause of Failure: Failed criteria: Verification

Test Case Information

Name: New Test Case 4

Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
✓ Test Seguence2/sten 1:verify(state error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
✓ Test Seguence2/sten 42:verifv(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
Test Sequence2/step_3:verify(dataOut == 0)
Test Sequence2/step_3:verify(state_error == 0)
Test Sequence2/step_3:verify(executed == 1)
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
✓ Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
O Test Sequence2/step_4:verify(executed == 1)
O Test Sequence2/step_5:verify(numInputs == 2)
O Test Sequence2/step_5:verify(numOutputs == 2)
Oracle Test Sequence2/step_5:verify(fb_error_code == 0)
O Test Sequence2/step_5:verify(dataOut == 0)
Oracle Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
O Test Sequence2/step_6:verify(numInputs == 2)
O Test Sequence2/step_6:verify(numOutputs == 2)
Test Sequence2/step_6:verify(fb_error_code == 0)
O Test Sequence2/step_6:verify(dataOut == 67108864)
O Test Sequence2/step_6:verify(state_error == 0)
✓ Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

New Test Case 5

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:55:17
End Time: 2019-Jan-07 14:55:30

Outcome: Passed

Test Case Information

Name: New Test Case 5 Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
✓ Test Seguence2/sten 1:verify(state error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
✓ Test Seguence2/sten 42:verifv(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
Test Sequence2/step_3:verify(dataOut == 0)
Test Sequence2/step_3:verify(state_error == 0)
Test Sequence2/step_3:verify(executed == 1)
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
O Test Sequence2/step_4:verify(executed == 1)
O Test Sequence2/step_5:verify(numInputs == 2)
O Test Sequence2/step_5:verify(numOutputs == 2)
Oracle Test Sequence2/step_5:verify(fb_error_code == 0)
O Test Sequence2/step_5:verify(dataOut == 0)
Oracle Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
O Test Sequence2/step_6:verify(numInputs == 2)
O Test Sequence2/step_6:verify(numOutputs == 2)
Test Sequence2/step_6:verify(fb_error_code == 0)
O Test Sequence2/step_6:verify(dataOut == 67108864)
O Test Sequence2/step_6:verify(state_error == 0)
✓ Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

New Test Case 6

Test Result Information

Result Type: Test Case Result
Parent: New Test Suite 1
Start Time: 2019-Jan-07 14:55:30
End Time: 2019-Jan-07 14:55:42

Outcome: Passed

Test Case Information

Name: New Test Case 6 Type: Baseline Test

Name
Test Sequence2/step_1:verify(numInputs == 2)
Test Sequence2/step_1:verify(numOutputs == 2)
Test Sequence2/step_1:verify(fb_error_code == 256)
Test Sequence2/step_1:verify(dataOut == 0)
✓ Test Seguence2/sten 1:verify(state error == 0)
Test Sequence2/step_1:verify(executed == 1)
Test Sequence2/step_42:verify(numInputs == 2)
✓ Test Seguence2/sten 42:verifv(numOutputs == 2)
Test Sequence2/step_42:verify(fb_error_code == 256)
Test Sequence2/step_42:verify(dataOut == 0)
Test Sequence2/step_42:verify(state_error == 0)
Test Sequence2/step_42:verify(executed == 1)
Test Sequence2/step_2:verify(numInputs == 2)
Test Sequence2/step_2:verify(numOutputs == 2)
Test Sequence2/step_2:verify(fb_error_code == 256)
Test Sequence2/step_2:verify(dataOut == 0)
Test Sequence2/step_2:verify(state_error == 0)
Test Sequence2/step_2:verify(executed == 1)
Test Sequence2/step_3:verify(numInputs == 2)
Test Sequence2/step_3:verify(numOutputs == 2)
Test Sequence2/step_3:verify(fb_error_code == 256)
Test Sequence2/step_3:verify(dataOut == 0)
Test Sequence2/step_3:verify(state_error == 0)
Test Sequence2/step_3:verify(executed == 1)
Test Sequence2/step_4:verify(numInputs == 2)
Test Sequence2/step_4:verify(numOutputs == 2)
Test Sequence2/step_4:verify(fb_error_code == 0)
Test Sequence2/step_4:verify(dataOut == 0)
Test Sequence2/step_4:verify(state_error == 0)
O Test Sequence2/step_4:verify(executed == 1)
O Test Sequence2/step_5:verify(numInputs == 2)
O Test Sequence2/step_5:verify(numOutputs == 2)
Oracle Test Sequence2/step_5:verify(fb_error_code == 0)
O Test Sequence2/step_5:verify(dataOut == 0)
Oracle Test Sequence2/step_5:verify(state_error == 0)
Test Sequence2/step_5:verify(executed == 1)
O Test Sequence2/step_6:verify(numInputs == 2)
O Test Sequence2/step_6:verify(numOutputs == 2)
Test Sequence2/step_6:verify(fb_error_code == 0)
O Test Sequence2/step_6:verify(dataOut == 67108864)
O Test Sequence2/step_6:verify(state_error == 0)
✓ Test Sequence2/step_6:verify(executed == 1)

System Under Test Information

Model: FBFunctions

Harness: FBFunctions_Harness_BSL Harness Owner: FBFunctions/BSL_DUPLEX

Simulation Mode: normal

Configuration Set: Configuration 1

Start Time: 0 Stop Time: 10

Checksum: 1460360143 3497721408 2131485215 3158160438

Simulink Version: 9.2 Model Version: 1.18

Model Author: jayakumarav

Date: Mon Jan 07 14:53:59 2019

User ID: jayakumarav

Model Path: C:\Users\jayakumarav\Documents\GitHub\Sympl

eVerification\FBFunctions\FBFunctions.slx

Machine Name: EGR-ELKS-05

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64