Coverage Report for FBFunctions

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Analysis Information

Model Information

Model version	1.68
Author	hiterd
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Harness information

Harness model(s)	FBFunctions_Harness_XOR
Harness model owner	FBFunctions

Simulation Optimization Options

Default parameter behavior	tunable
Block reduction	forced off
Conditional branch optimization	on

Coverage Options

Analyzed model	FBFunctions_Harness_XOR/XOR_DUPLEX
Logic block short circuiting	off
MCDC mode	masking

Tests

Test#	Started execution	Ended execution

Test 1 03-Feb-2019 22:18:39 03-Feb-2019 22:20:12

Summary

Model Hierarchy/Complexity		Test 1			
		Decision	Condition	MCDC	Execution
1. XOR_DUPLEX	24	95%	97%	71%	99%
2. . . . State Comparator	1	50%	100%	NA	80%
3. . . . . Compare To Zero		NA	100%	NA	100%
4. . . . XOR	11	100%	98%	75%	100%
5. . . . . 2_val_shift_register	4	NA	NA	NA	100%
6. . . . . Data 1	1	NA	NA	NA	100%
7. . . . . Unit Delay Enabled Resettable	1	NA	NA	NA	100%
8. . . . . Data 2	1	NA	NA	NA	100%
9. . . . . Unit Delay Enabled Resettable	1	NA	NA	NA	100%
10. . . . . Type 1	1	NA	NA	NA	100%
11. . . . . Unit Delay Enabled Resettable	1	NA	NA	NA	100%
12. . . . . Type 2	1	NA	NA	NA	100%
13. . . . . Unit Delay Enabled Resettable	1	NA	NA	NA	100%
14. . . . . TypeCheck2T2D	1	100%	100%	20%	100%
15. . . . . code_type_bit		NA	NA	NA	100%
16. . . . . cond_generate_error_code	1	100%	NA	NA	100%
17. . . . . code_no_error		NA	NA	NA	100%
18. . . . . isType1		NA	100%	NA	100%
19. . . . . isType		NA	100%	NA	100%
20. . . . . typeMask		NA	NA	NA	100%
21. . . . . isType1		NA	100%	NA	100%
22. . . . . typeMask		NA	NA	NA	100%
23. . . . . isType2		NA	100%	NA	100%
24. . . . . isType		NA	100%	NA	100%
25. . . . . typeMask		NA	NA	NA	100%
26. . . . . isType1		NA	100%	NA	100%
27. . . . . typeMask		NA	NA	NA	100%
28. . . . . isTypeMatch2		NA	100%	NA	100%
29. . . . . typeMask		NA	NA	NA	100%
30. . . . . typeMask1		NA	NA	NA	100%
31. . . . . Unit Delay Enabled Resettable Synchronous8	1	NA	NA	NA	100%
32. . . . . Unit Delay Enabled Resettable	1	NA	NA	NA	100%

33.	Unit Delay Enabled Resettable Synchronous9	1	NA		NA		NA		100%	
34.	Unit Delay Enabled Resettable	1	NA		NA		NA		100%	
35.	bool type		NA		NA		NA		100%	
36.	boolToSafebool	1	100%		NA		NA		100%	
37.	safebool false		NA		NA		NA		100%	
38.	safebool true		NA		NA		NA		100%	
39.	isType		NA		100%		NA		100%	
40.	typeMask		NA		NA		NA		100%	
41.	safebool type		NA		NA		NA		100%	
42.	safebool type1		NA		NA		NA		100%	
43.	safeboolToBool1		NA		100%		NA		100%	
44.	safebool true		NA		NA		NA		100%	
45.	safeboolToBool2		NA		50%		NA		100%	
46.	safebool true		NA		NA		NA		100%	
47.	safeboolToBool3		NA		100%		NA		100%	
48.	safebool true		NA		NA		NA		100%	
49. . . .	XOR1	11	100%		98%		75%		100%	
50.	2_val_shift_register	4	NA		NA		NA		100%	
51.	Data 1	1	NA		NA		NA		100%	
52.	Unit Delay Enabled Resettable	1	NA		NA		NA		100%	
53.	Data 2	1	NA		NA		NA		100%	
54.	Unit Delay Enabled Resettable	1	NA		NA		NA		100%	
55.	Type 1	1	NA		NA		NA		100%	
56.	Unit Delay Enabled Resettable	1	NA		NA		NA		100%	
57.	Type 2	1	NA		NA		NA		100%	
58.	Unit Delay Enabled Resettable	1	NA		NA		NA		100%	
59.	TypeCheck2T2D	1	100%		100%		20%		100%	
60.	code_type_bit		NA		NA		NA		100%	
61.	cond_generate_error_code	1	100%		NA		NA		100%	
62.	code_no_error		NA		NA		NA		100%	
63.	isType1		NA		100%		NA		100%	
64.	isType		NA		100%		NA		100%	
65.	typeMask		NA		NA		NA		100%	
66.	isType1		NA		100%		NA		100%	
67.	typeMask		NA		NA		NA		100%	
68.	isType2		NA		100%		NA		100%	
69.	isType		NA		100%		NA		100%	
70.	typeMask		NA		NA		NA		100%	

71. . . . . isType1		NA	100%		NA	100%
72. . . . . typeMask		NA	NA		NA	100%
73. . . . . isTypeMatch2		NA	100%		NA	100%
74. . . . . typeMask		NA	NA		NA	100%
75. . . . . typeMask1		NA	NA		NA	100%
76. . . . . Unit Delay Enabled Resettable Synchronous8	1	NA	NA		NA	100%
77. . . . . Unit Delay Enabled Resettable	1	NA	NA		NA	100%
78. . . . . Unit Delay Enabled Resettable Synchronous9	1	NA	NA		NA	100%
79. . . . . Unit Delay Enabled Resettable	1	NA	NA		NA	100%
80. . . . . bool type		NA	NA		NA	100%
81. . . . . boolToSafebool	1	100%	NA		NA	100%
82. . . . . safebool false		NA	NA		NA	100%
83. . . . . safebool true		NA	NA		NA	100%
84. . . . . isType		NA	100%		NA	100%
85. . . . . typeMask		NA	NA		NA	100%
86. . . . . safebool type		NA	NA		NA	100%
87. . . . . safebool type1		NA	NA		NA	100%
88. . . . . safeboolToBool1		NA	100%		NA	100%
89. . . . . safebool true		NA	NA		NA	100%
90. . . . . safeboolToBool2		NA	50%		NA	100%
91. . . . . safebool true		NA	NA		NA	100%
92. . . . . safeboolToBool3		NA	100%		NA	100%
93. . . . . safebool true		NA	NA		NA	100%
94. . . . combine_error_codes		NA	NA		NA	100%

Details

1. SubSystem block "XOR_DUPLEX"

Child Systems: State Comparator, XOR, XOR1, combine_error_codes

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	24
Condition	NA	97% (144/148) condition outcomes
Decision	NA	95% (21/22) decision outcomes
MCDC	NA	71% (24/34) conditions reversed the outcome
Execution	NA	99% (114/115) objective outcomes

Logic block "Logical Operator"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX

Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Condition	50% (2/4) condition outcomes
MCDC	0% (0/2) conditions reversed the outcome
Execution	100% (1/1) objective outcomes

Conditions analyzed

Description	True	False
input port 1	187	0
input port 2	187	0

MC/DC analysis (combinations in parentheses did not occur)

Decision/Condition	True Out	False Out
expression for output		
input port 1	**T**T	(**F**T)
input port 2	T**T**	(T**F**)

Full Coverage

Model Object	Metric
RelationalOperator block "Relational Operator"	Condition, Execution
Constant block "Num Ins"	Execution
Constant block "Num Outs"	Execution
Constant block "fb_num_constant"	Execution

2. SubSystem block "State Comparator"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX
Child Systems: Compare To Zero

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Condition	NA	100% (14/14) condition outcomes
Decision	NA	50% (1/2) decision outcomes
Execution	NA	80% (4/5) objective outcomes

Switch block "Switch1"

Justify or Exclude
Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/State Comparator
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	1
Decision	50% (1/2) decision outcomes
Execution	100% (1/1) objective outcomes

Decisions analyzed

logical trigger input	50%
false (output is from 3rd input port)	0/187
true (output is from 1st input port)	187/187

Constant block "Constant1"

Justify or Exclude
Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/State Comparator
Uncovered Links:

Metric	Coverage
Cyclomatic Complexity	0
Execution	0% (0/1) objective outcomes

Full Coverage

Model Object	Metric

Sum block "Sum of Elements"	Execution
RelationalOperator block "Relational Operator"	Condition, Execution

3. SubSystem block "Compare To Zero"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/State Comparator

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	0
Condition	NA	100% (2/2) condition outcomes
Execution	NA	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
RelationalOperator block "Compare"	Condition, Execution

4. SubSystem block "XOR"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX

Child Systems: 2_val_shift_register, TypeCheck2T2D, Unit Delay Enabled Resettable Synchronous8, Unit Delay Enabled Resettable Synchronous9, bool type, boolToSafebool, isType, safebool type, safebool type1, safeboolToBool1, safeboolToBool2, safeboolToBool3

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	11
Condition	NA	98% (63/64) condition outcomes
Decision	NA	100% (10/10) decision outcomes
MCDC	NA	75% (12/16) conditions reversed the outcome
Execution	NA	100% (52/52) objective outcomes

Logic block "Logical Operator3"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR

Metric	Coverage
Cyclomatic Complexity	0
Condition	100% (4/4) condition outcomes
MCDC	see Logical Operator
Execution	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
Logic block "Logical Operator"	Condition, MCDC, Execution
Logic block "Logical Operator1"	Condition, MCDC, Execution
Logic block "Logical Operator2"	Condition, MCDC, Execution
Logic block "Logical Operator4"	Condition, MCDC, Execution
Logic block "Logical Operator5"	Condition, MCDC, Execution
Logic block "Logical Operator6"	Condition, Execution
Switch block "Switch"	Decision, Execution
Switch block "Switch1"	Decision, Execution
Switch block "Switch2"	Decision, Execution
Constant block "Constant"	Execution
Constant block "Constant1"	Execution

5. SubSystem block "2_val_shift_register"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR
Child Systems: Type 1, Type 2, Data 1, Data 2

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	4
Execution	NA	100% (4/4) objective outcomes

6. SubSystem block "Data 1"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register
Child Systems: Unit Delay Enabled Resettable

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Execution	NA	100% (1/1) objective outcomes

7. SubSystem block "Unit Delay Enabled Resettable"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register/Data 1

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	1
Execution	NA	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
Delay block "Enabled Resettable Delay"	Execution

8. SubSystem block "Data 2"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register
Child Systems: Unit Delay Enabled Resettable

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Execution	NA	100% (1/1) objective outcomes

9. SubSystem block "Unit Delay Enabled Resettable"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register/Data 2

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	1
Execution	NA	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
Delay block "Enabled Resettable Delay"	Execution

10. SubSystem block "Type 1"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register
Child Systems: Unit Delay Enabled Resettable

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Execution	NA	100% (1/1) objective outcomes

11. SubSystem block "Unit Delay Enabled Resettable"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register/Type 1

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	1
Execution	NA	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
Delay block "Enabled Resettable Delay"	Execution

12. SubSystem block "Type 2"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register
Child Systems: Unit Delay Enabled Resettable

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Execution	NA	100% (1/1) objective outcomes

13. SubSystem block "Unit Delay Enabled Resettable"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/2_val_shift_register/Type 2

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	1	1
Execution	NA	100% (1/1) objective outcomes

Full Coverage

Model Object	Metric
Delay block "Enabled Resettable Delay"	Execution

14. SubSystem block "TypeCheck2T2D"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR
Child Systems: code_type_bit, cond_generate_error_code, isType1, isType2, isTypeMatch2

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Condition	NA	100% (30/30) condition outcomes
Decision	NA	100% (2/2) decision outcomes
MCDC	NA	20% (1/5) conditions reversed the outcome
Execution	NA	100% (20/20) objective outcomes

Logic block "Logical Operator"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/TypeCheck2T2D

Metric	Coverage
Cyclomatic Complexity	0
Condition	100% (2/2) condition outcomes
MCDC	see Logical Operator1
Execution	100% (1/1) objective outcomes

Logic block "Logical Operator1"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/TypeCheck2T2D

Uncovered Links: 

Metric	Coverage
Cyclomatic Complexity	0
Condition	100% (6/6) condition outcomes
MCDC	20% (1/5) conditions reversed the outcome
Execution	100% (1/1) objective outcomes

MC/DC analysis (combinations in parentheses did not occur)

Includes 6 blocks

Decision/Condition	True Out	False Out
(~C1 || ~(C2 || C3)) || ~(C4 || C5)		
C1 (Logical Operator In1)	**F**TFFT	**T**TFTF
C2 (Logical Operator In1)	(T**F**FTF)	T**T**FTF
C3 (Logical Operator In2)	(TF**F**TT)	TF**T**FT
C4 (Logical Operator In1)	(TTF**F**F)	TTF**T**F
C5 (Logical Operator In2)	(TTTF**F**)	TFTF**T**

Logic block "Logical Operator2"

Justify or Exclude

Parent: FBFunctions_Harness_XOR/XOR_DUPLEX/XOR/TypeCheck2T2D

Metric	Coverage
Cyclomatic Complexity	0

Condition	100% (2/2) condition outcomes
MCDC	see Logical Operator1
Execution	100% (1/1) objective outcomes

Logic block "Logical Operator3"

Justify or E