SMART CAR PARKING SYSTEM

ADVANCED EMBEDDED SYSTEM

GROUP 8 - SPRINT 1

Team Members:

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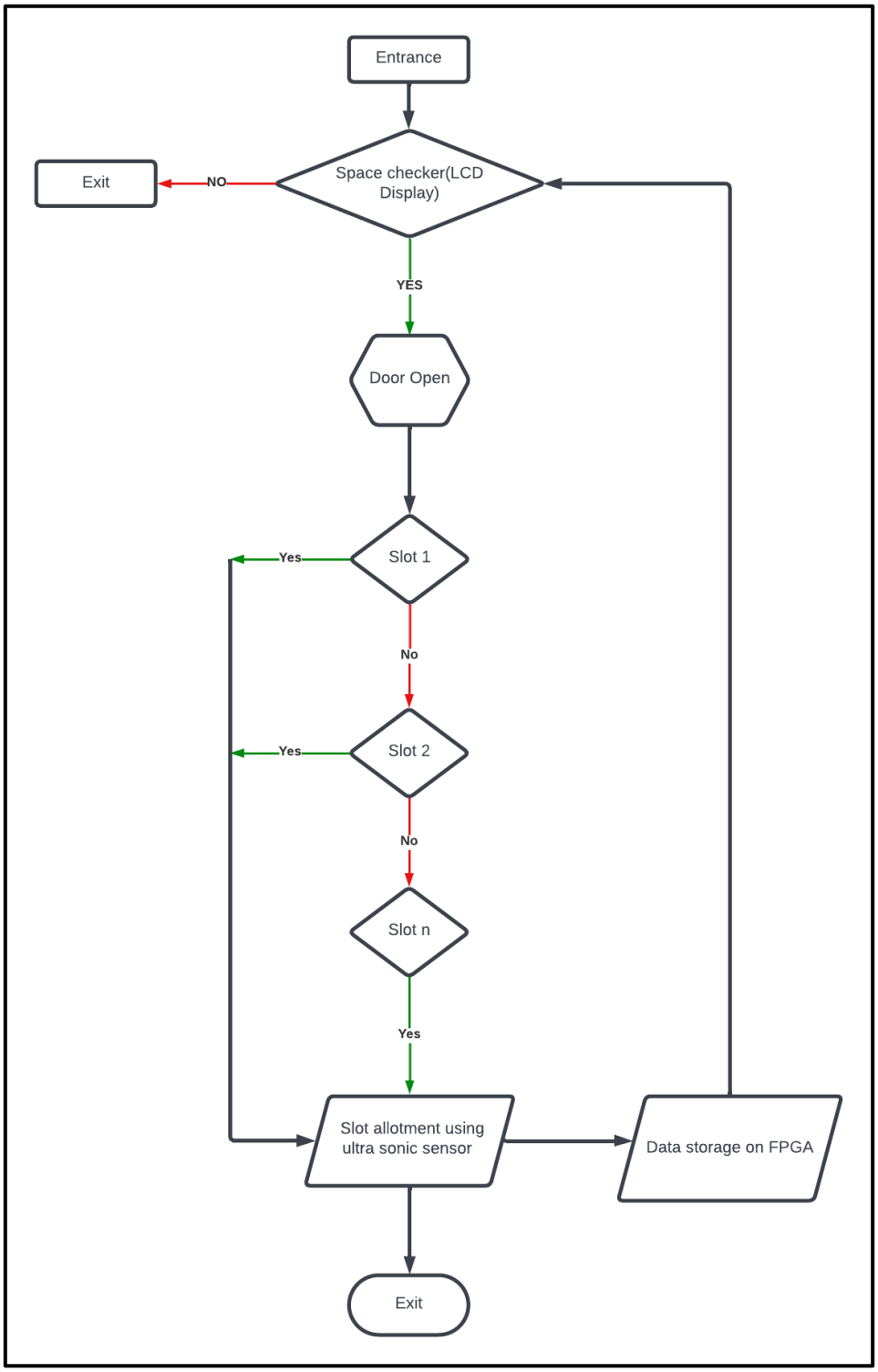
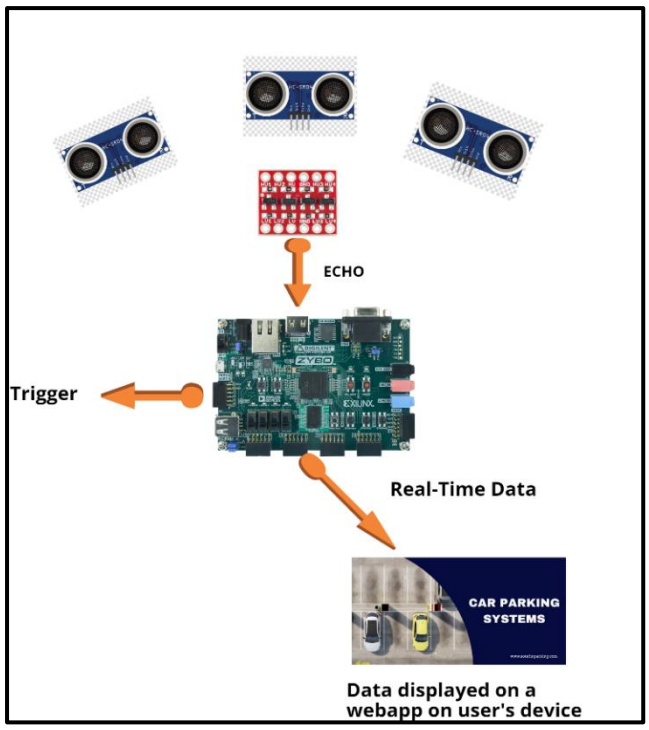
Hardware Required:

1. Ultrasonic sensors
2. Logic Level Convertor
3. FPGA

Work-flow diagram:

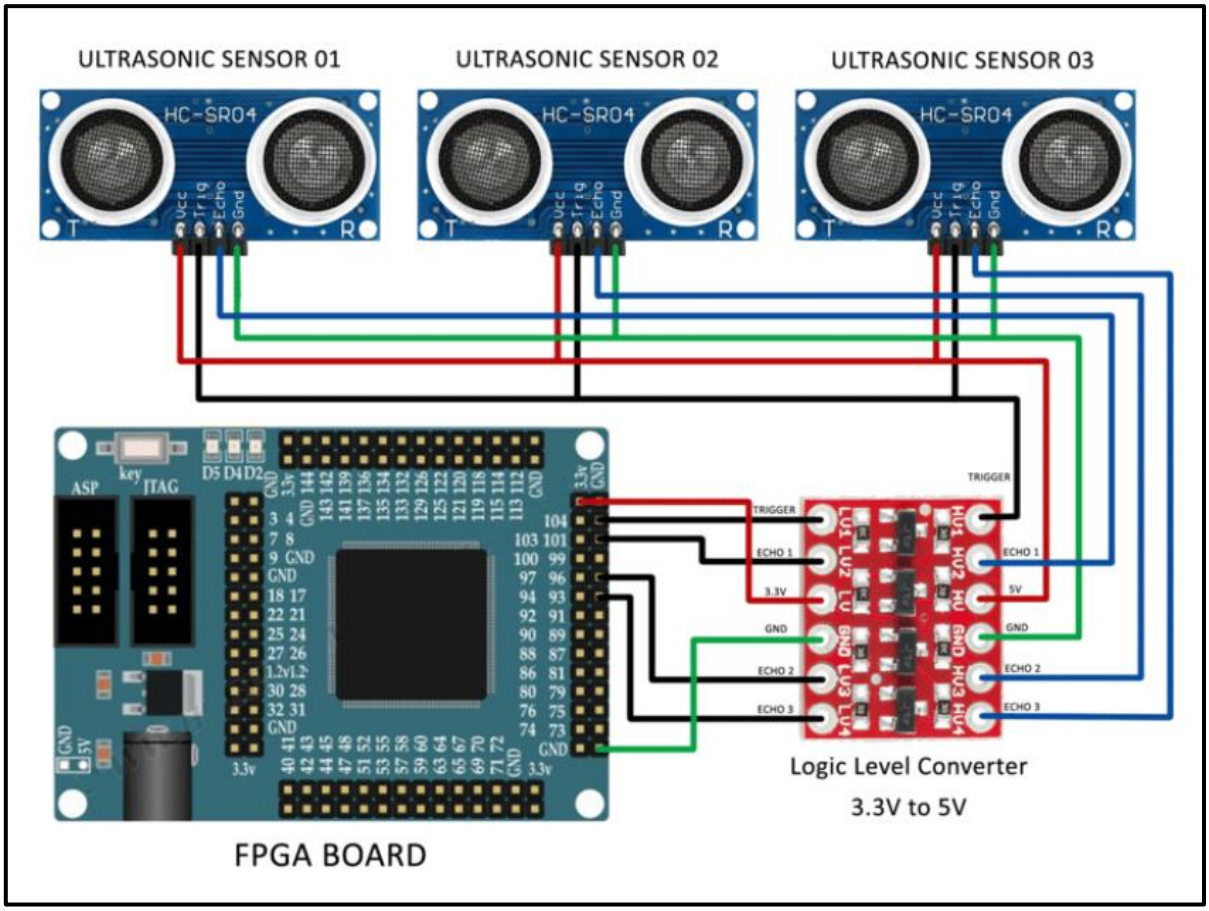


Assembly of the parts:



The input to the system is an array of three low-cost HC-SR04 ultrasonic sensors. Each sensor has 4 pins, namely VCC, Trigger, Echo and Ground. When a trigger signal of 10uS is sent to the ultrasonic sensor the sensor itself produces a set of eight burst signals through the transmitter. The receiver receives the reflected back signal and output a pulse proportional to the distance measured. A detailed image is shown here. The ultrasonic range sensors have a detection range of 4m with an accuracy of 3mm. The best of the ultrasonic range sensors could be gained through a FPGA chip. A large amount of sensor readings is gained concurrently without any delay with use of an FPGA

Connections:



- **Sensor**
  HC-SR04 Ultrasonic Distance Sensor The HC-SR04 required 5V to operate properly and its detection range is 2cm – 400cm. Here is the basic principle of how the sensor works: The trigger is HIGH for at least 10us 2. The module automatically sends eight 40kHz pulses and detects the pulse echo, if it exists 3. Time of high output I/O duration is the time from sending the ultrasonic pulse to receiving the ultrasonic pulse

- **FPGA:**
  FPGA, over the equivalent discrete circuit or an Application Specific IC (ASIC) is the ability to easily change its functionality after a product has been designed. In addition, FPGA require a smaller board space and can be more energy efficient than the equivalent discrete circuit.

- **Logic Level Converter:**
  A logic level converter or logic level shifter is a necessary circuit while interfacing devices with different voltage requirements. Logic level converter steps up or steps down the voltage as per the requirement of a device.

Connections Steps:

1. **Ultrasonic Sensors:**

   - Each ultrasonic sensor typically has a "Trigger" pin and an "Echo" pin.

   - Connect the "Trigger" pin of each sensor to separate GPIO pins on your FPGA board. These pins will be used to send the trigger signal.

   - Connect the "Echo" pin of each sensor to separate GPIO pins on the FPGA. These pins will be used to receive the echo signal.

2. **Logic Level Converter:**

   - Logic level converters are used to translate voltage levels from one voltage domain to another.

   - Connect the "LV" side of the logic level converter to the FPGA GPIO pins. Make sure to connect each converted pin to the corresponding ultrasonic sensor's "Trigger" and "Echo" pins.

   - Connect the "HV" side of the logic level converter to the ultrasonic sensors' "Trigger" and "Echo" pins.

3. **FPGA Board:**

    - Consult your FPGA board's documentation to determine the voltage levels it operates with (usually 3.3V or 2.5V).

    - Connect the "LV" side of the logic level converter to appropriate GPIO pins on the FPGA board.

    - Ensure you configure the FPGA GPIO pins as outputs for sending trigger signals and as inputs for receiving echo signals.

Backup Plan:

RF Module: In this module IR trans-receiver pair is used to detect vehicle presence. IR sensors transmit slot's status to HT12E encoder. Encoder consists of 18 pin configurations. Parallel data convert into serial by encoder. Data is collected at data out pin of encoder. From data out pin data serially transmit towards RF transmitter. Data serially received at RF receiver. HT12 D decoder receiver's data from RF receiver, then converter back serial to parallel form. HT12D decoder's data pins are interfaced with Virtex 5 C I/O port signal pins.