

• FSM (in Our Project)

a) Initialisation :- 'State - Idle'

b) State - Idle :- FSM waits for the 'start_measurement'

c) Trigger STATE :- * After signal measurement

* Activates 'sensor trigger' output signal - initializes the ultrasonic sensor

* Counts the clock cycles until the trigger pulse duration is reached. (COUNT_TRIGGER_PULSE)

d) STATE - WAIT - FOR - ECHO :-

After sending Trigger pulse

↳ Waits for the (SENSOR_ECHO) signal. (Return of ultrasonic signal)

↳ When sensor-echo is detected measurement state.

e) MEASUREMENT State :- 'State - Measurement'

* FSM measure the time taken for the ultra-sonic signal to travel (from target & back)

* Increments Counter on each clock cycle.

* When 'Count - Timeout' occurs / 'sensor-echo' goes down

f) Measurement Complete state :-

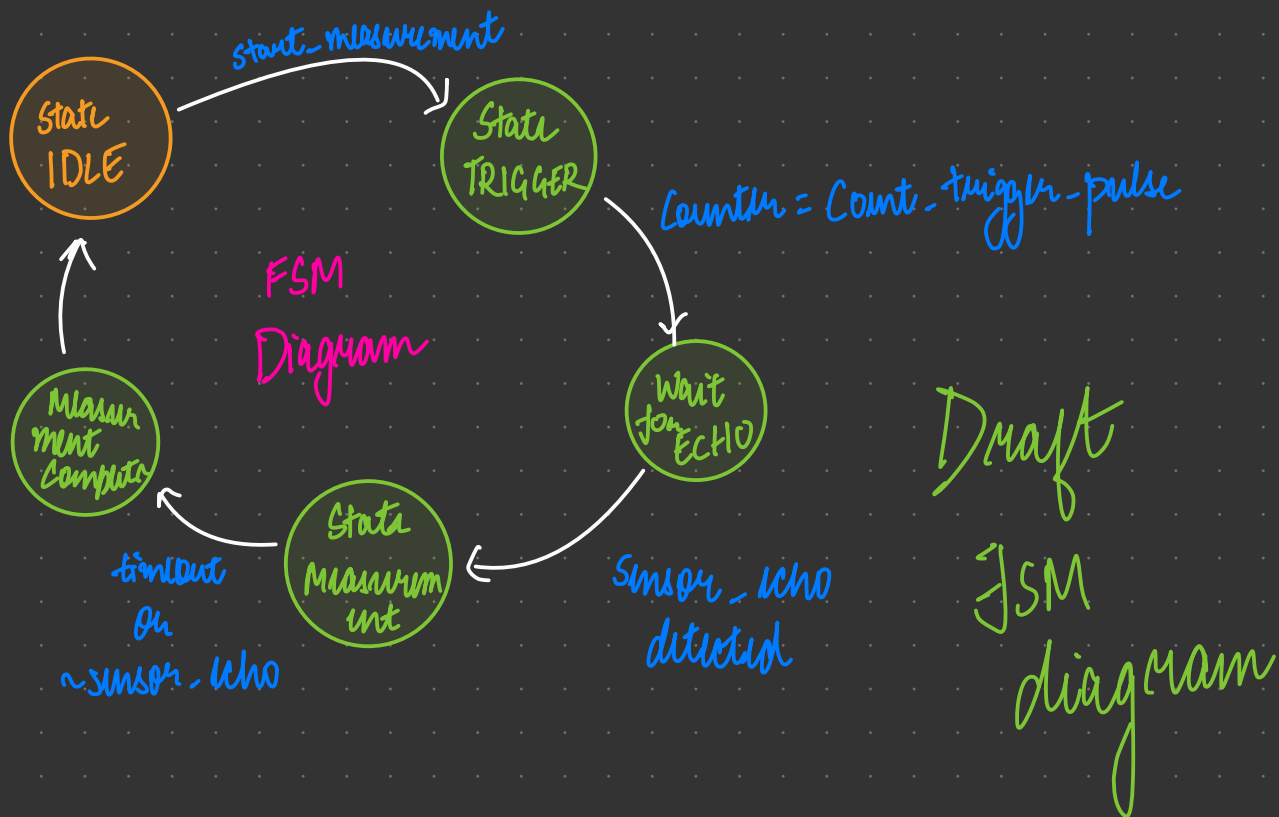
* Completes the measurement

* Counter value is captured as 'counter capture' ↑ time taken.

* Resets the counter & returns to idle state.

• FSM TABLE:-

Current State	Input/Condition	Next State	Output Actions
STATE_IDLE	start_measurement asserted	STATE_TRIGGER	Activate sensor_trigger to initiate measurement.
STATE_TRIGGER	Counter reaches COUNT_TRIGGER_PULSE	STATE_WAIT_FOR_ECHO	Continue waiting for sensor_echo.
STATE_WAIT_FOR_ECHO	sensor_echo detected	STATE_MEASUREMENT	Begin distance measurement.
STATE_MEASUREMENT	Timeout or (~sensor_echo)	STATE_MEASUREMENT_COMPLETE	Measurement complete; capture measurement.
STATE_MEASUREMENT_COMPLETE	N/A	STATE_IDLE	Reset for the next measurement cycle.



Clock

Data Input of Counter

Main logic
L (user man)

LEDD

2

LED1

2

3

4

5

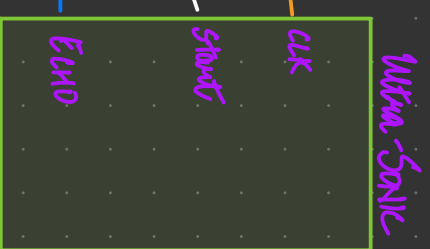
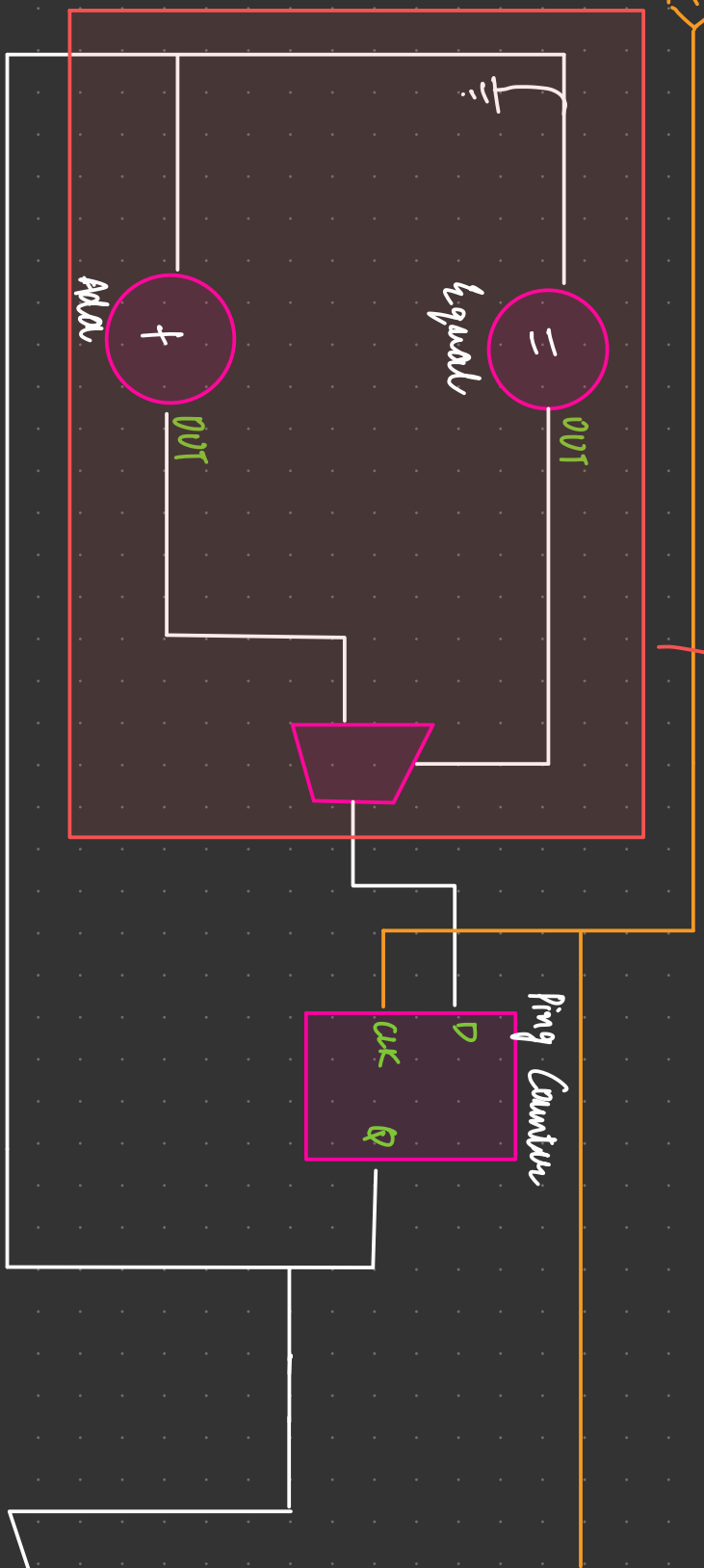
6

timeOut

timeOut



LEDs



ECHO

SCHEMATIC DIAGRAM

