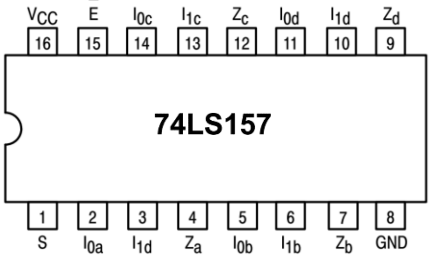
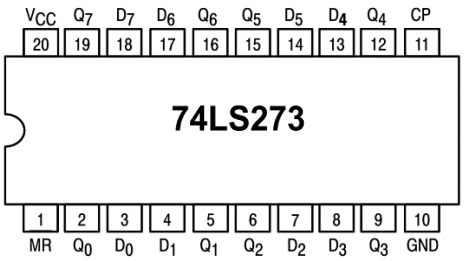


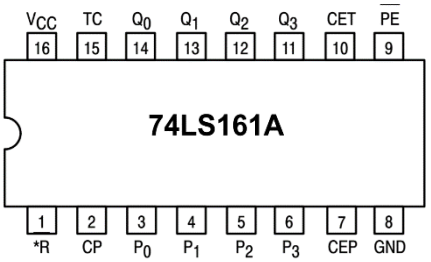
PIN NAMES

$\overline{S}$	Common Select Input
E	Enable (Active LOW) Input
$I_{0a}-I_{0d}$	Data Inputs from Source 0
$I_{1a}-I_{1d}$	Data Inputs from Source 1
Z_a-Z_d	Multiplexer Outputs (Note b)



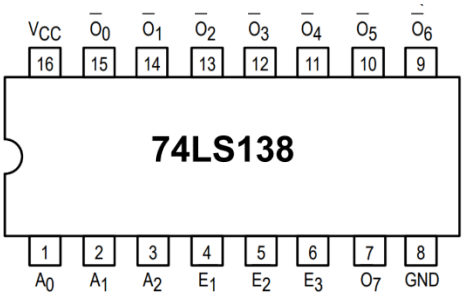
PIN NAMES

CP	Clock (Active HIGH Going Edge) Input
$\overline{D_0}-D_7$	Data Inputs
MR	Master Reset (Active LOW) Input
Q_0-Q_7	Register Outputs (Note b)



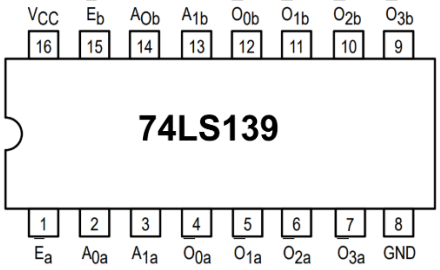
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0-P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
$\overline{CP}$	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
SR	Synchronous Reset (Active LOW) Input
Q_0-Q_3	Parallel Outputs (Note b)
TC	Terminal Count Output (Note b)



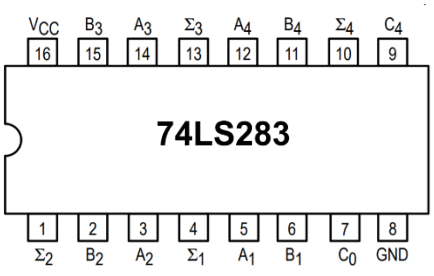
PIN NAMES

$\overline{A_0}-\overline{A_2}$	Address Inputs
E_1, E_2	Enable (Active LOW) Inputs
$\overline{E_3}$	Enable (Active HIGH) Input
$\overline{O_0}-\overline{O_7}$	Active LOW Outputs (Note b)



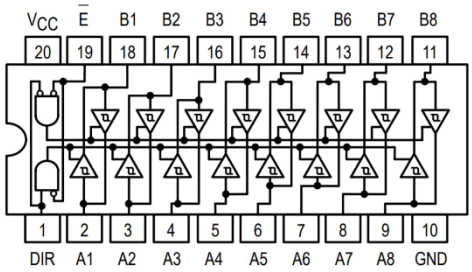
PIN NAMES

A_0, A_1	Address Inputs
$\overline{E}$	Enable (Active LOW) Input
$\overline{O_0}-\overline{O_3}$	Active LOW Outputs (Note b)



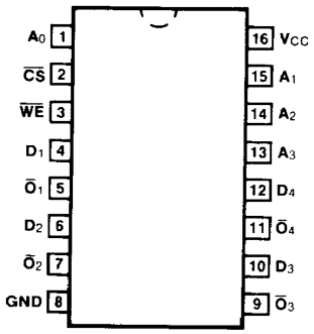
PIN NAMES

A_1-A_4	Operand A Inputs
B_1-B_4	Operand B Inputs
C_0	Carry Input
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)
C_4	Carry Output (Note b)



74LS245

INPUTS		OUTPUT
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation



74LS189

PIN NAMES	DESCRIPTION
A_0-A_3	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
D_1-D_4	Data Inputs
$\overline{O_1}-\overline{O_4}$	Inverted Data Outputs

74138 3 to 8 decoder

74139 Dual 2-line to 4-line decoder

74157 Quad 2-line to 1-line multiplexer

74161 4-bit synchronous binary counter

74189 64-bit RAM

74245 Octal bus transceiver

74273 Octal D flip-flop

74283 4-bit binary full adder

7400 NAND

7402 NOR

7404 NOT

7408 AND

7432 OR

7476 JK

7486 XOR