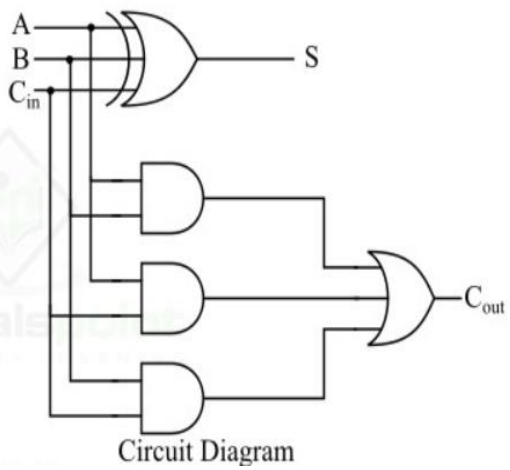
Marwadi University	**Marwadi University** **Faculty of engineering and technology** **Department of Information and Communication Technology**	
Subject: VLSI Design	**AIM: Design and Implementation of Digital Circuits in Microwind**	
LONG HOUR DESIGN	**Date: 13/09/2025**	**Enrollment No:92410133045**

1. 4-Bit Full Adder

A 4-bit Full Adder is designed to generate a 4-bit Sum and is designed by combining four 2-bit Full Adders and the Four bits output along with the Carry Bit.

Circuit Diagrams: -



Circuit Diagram

Truth Tables: -

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Equations: -

The sum (S) of the full-adder is the XOR of A, B, and Cin. Therefore,

$$\text{Sum, } S = A \oplus B \oplus C_{in} = A'B'C_{in} + A'BC'_{in} + AB'C'_{in} + ABC_{in}$$

The carry (C) of the half-adder is the AND of A and B. Therefore,

$$\text{Carry, } C = AB + AC_{in} + BC_{in}$$

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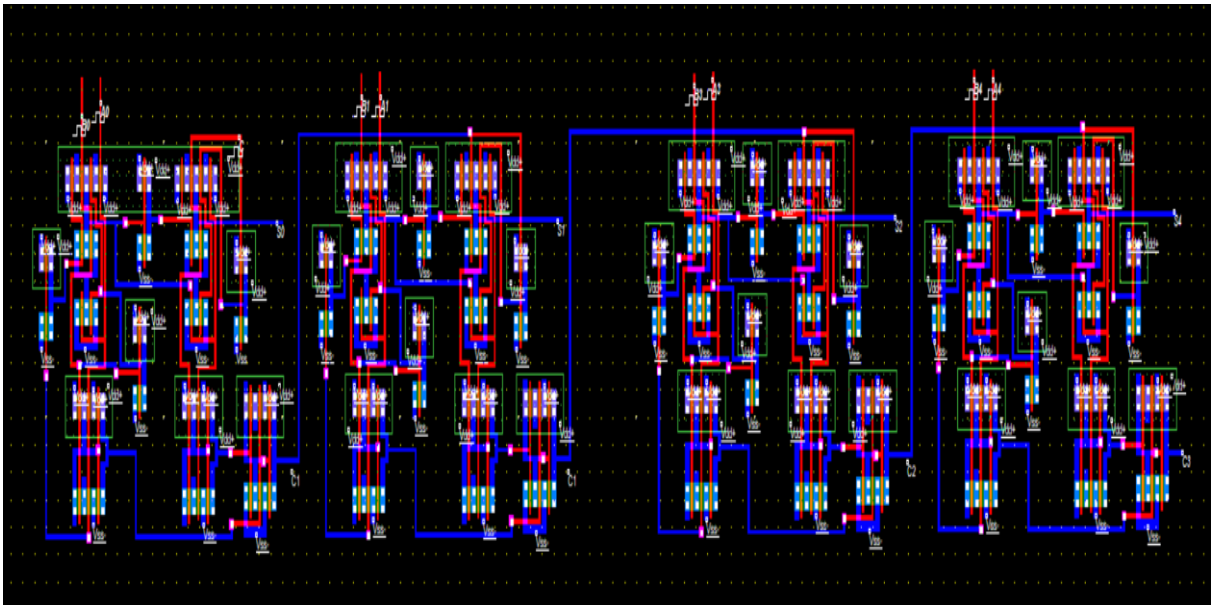
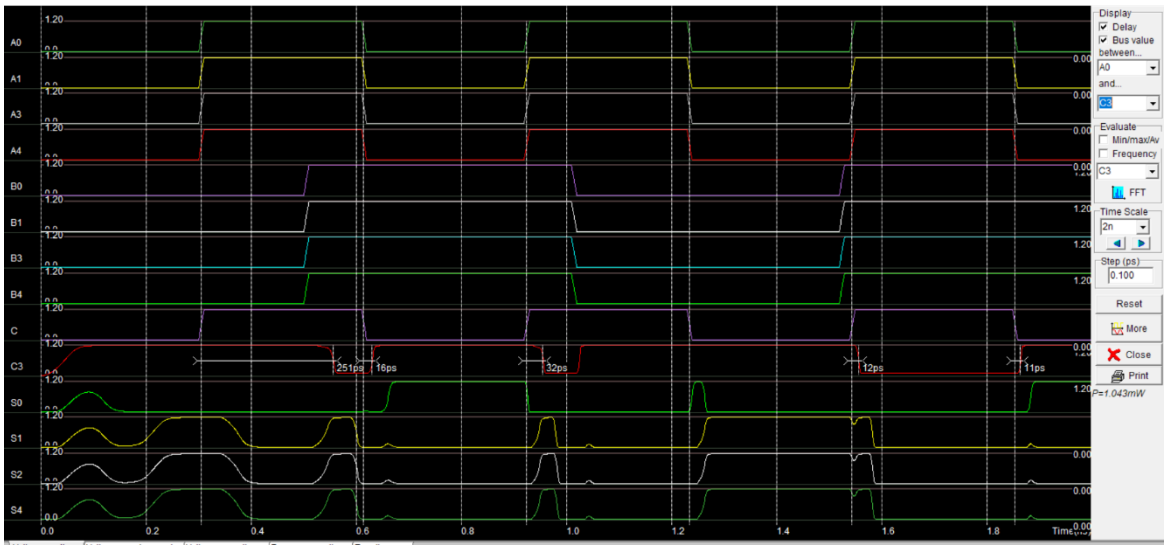
Screenshots Of Layouts: -





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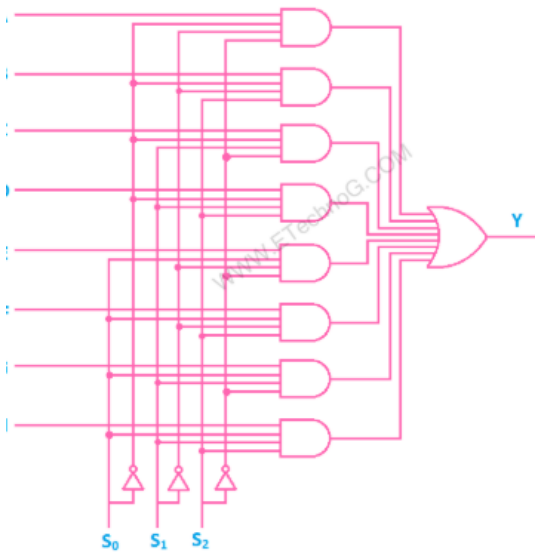
2. 8×1 Multiplexer

The 8×1 Multiplexer is made using 4×1 Multiplexers and 2×1 Multiplexer. We know that 4×1 Multiplexer has 4 data inputs, 2 selection lines and one output. Whereas, 8×1 Multiplexer has 8 data inputs, 3 selection lines and one output.

Circuit Diagrams: -



Block Diagram: -

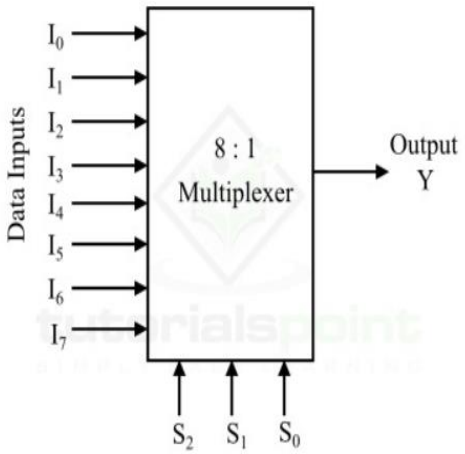


Figure 4 - 8:1 Multiplexer

Truth Tables: -

Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

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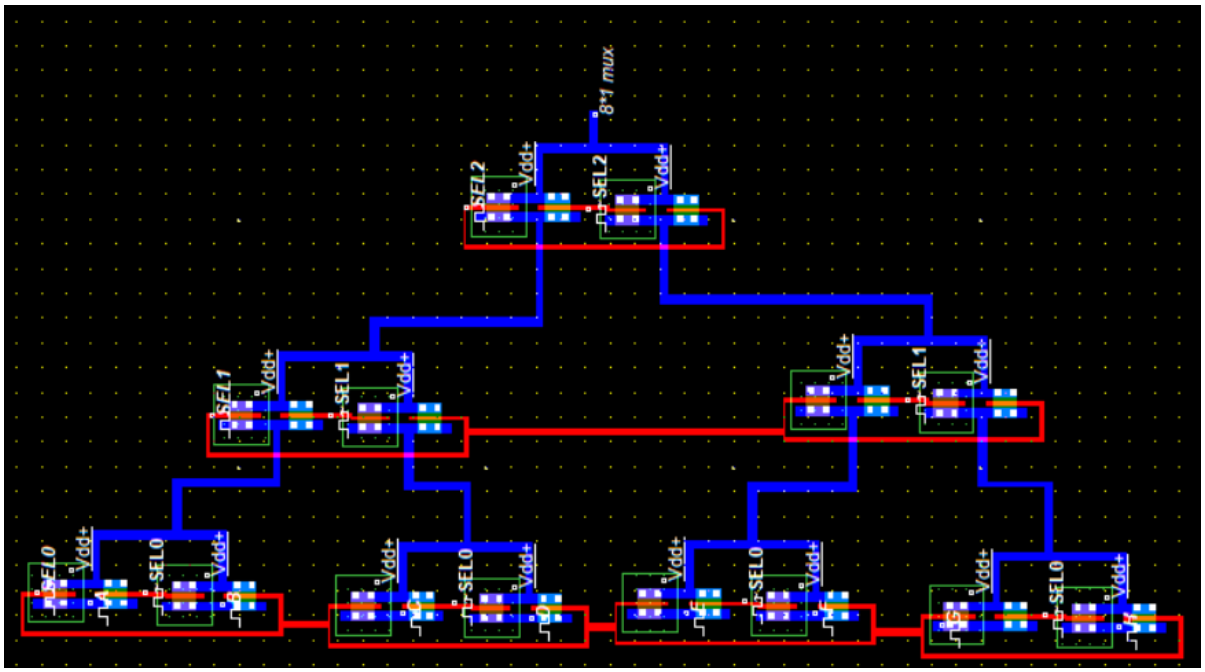
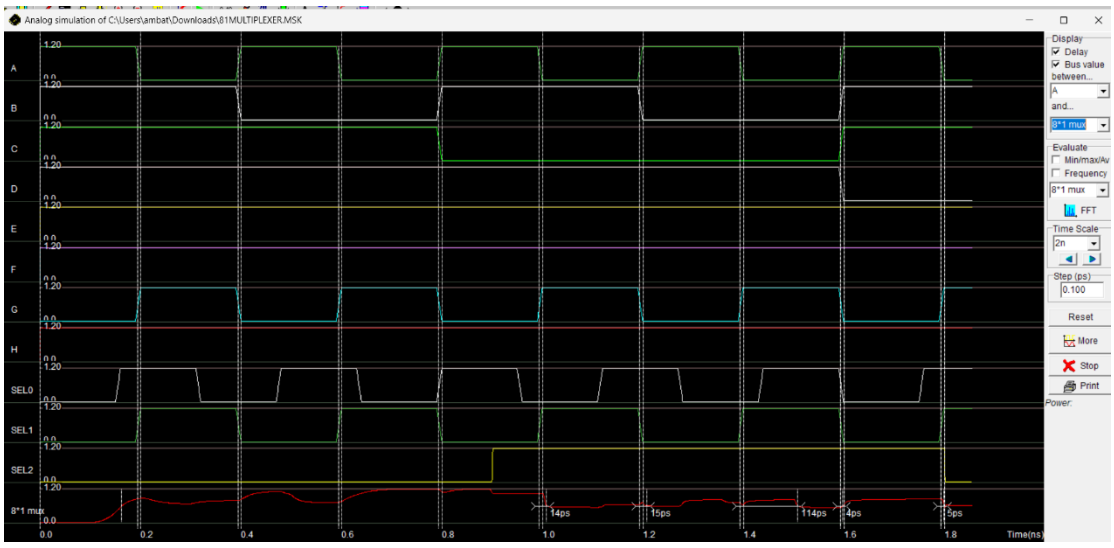
Logic Equations: -

$Y = S2S1S0I0+S2S1S0I1+S2S1S0I2+S2S1S0I3+S2S1S0I4+S2S1S0I5+S2S1S0I6+S2S1S0I7$

Screenshots Of Layouts: -





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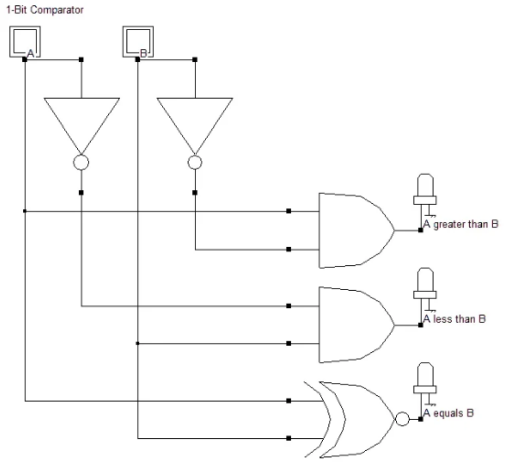
3. 1-bit Magnitude Comparator

A 1-bit magnitude comparator circuit diagram compares two 1-bit binary inputs (A and B) and produces outputs indicating whether A is greater than, equal to, or less than B. The circuit typically uses logic gates like XOR, AND, and NOT gates to implement these comparisons. The output signals would represent the comparison outcomes: A > B, A = B, or A < B.

Circuit Diagrams: -



The logic circuit of a 1-bit comparator

Truth Tables: -

Inputs		Outputs		
B	A	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Logic Equations: -

$$Z = A'B' + AB$$

This is similar to the equation of an EXNOR gate. Hence,

$$Z = A \oplus B$$

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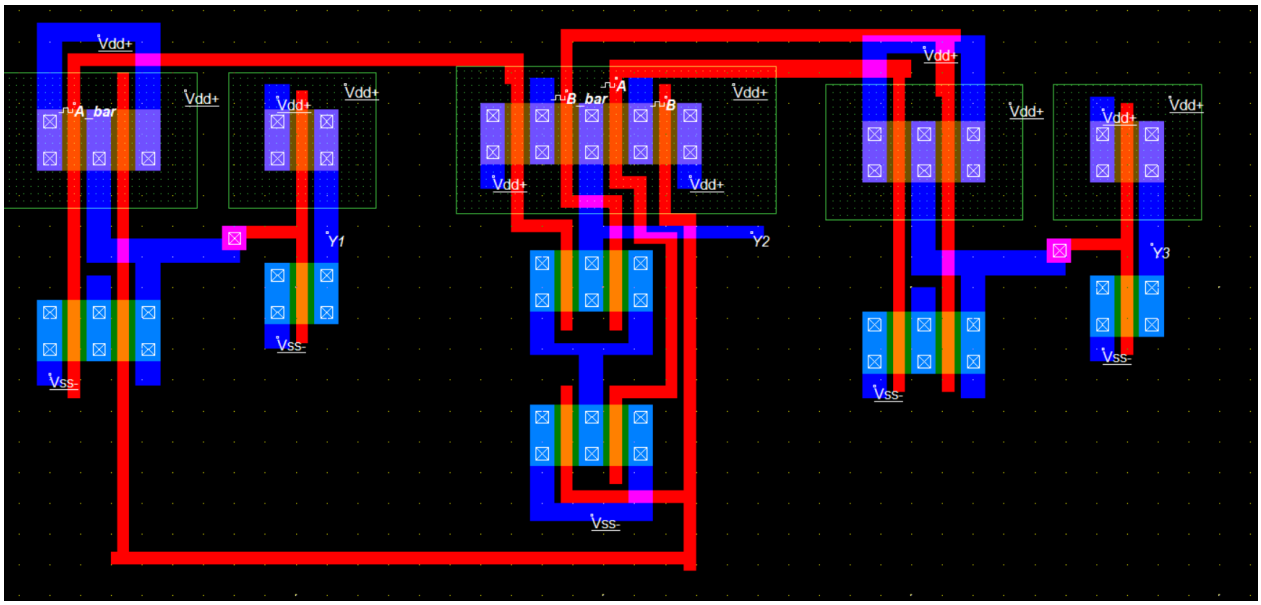

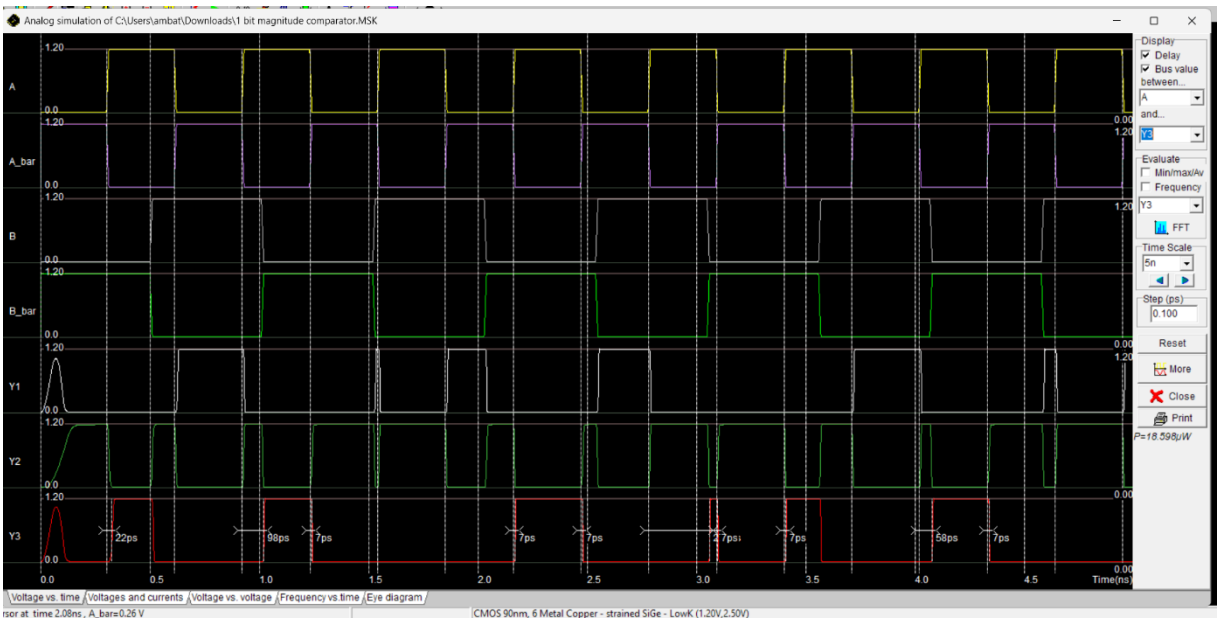

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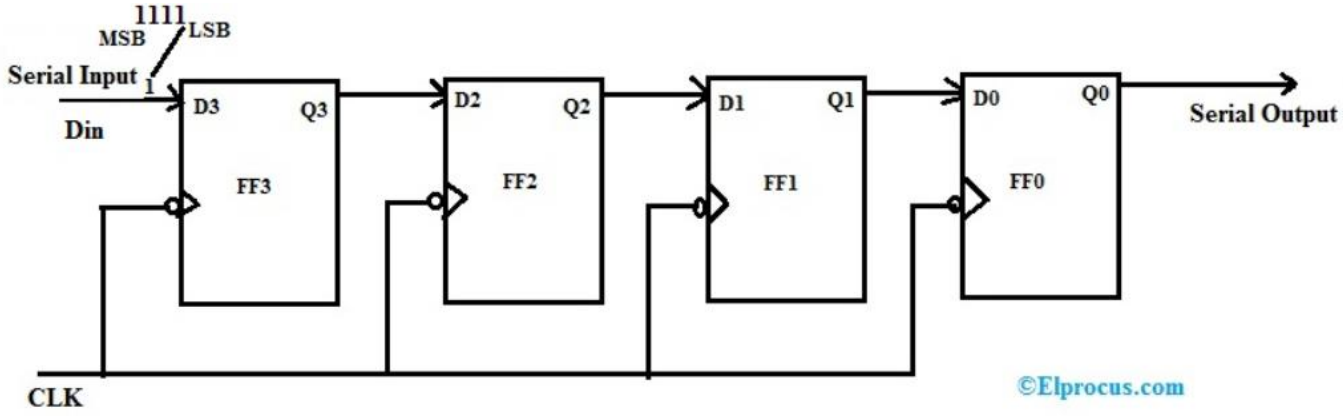
4. 4-bit Serial-In Serial-Out (SISO) Register

The term "SISO" stands for "Serial-In Serial-Out". The SISO shift register circuit accepts serial data on its input pin and shifts it out serially on its output pin. The number of bits that can be shifted out before the next bit arrives depends on the speed of the clock signal that controls the operation of the shift register. This type of shift register can be used as a buffer between two asynchronous devices that communicate with each other using signals with different frequencies or phases.

Circuit Diagrams: -



Truth Table:

Operation of the Shift-right Register

Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	1	1	0	0	0
After 3rd clock pulse	0	1	1	0	0
After 4th clock pulse	1	0	1	1	1

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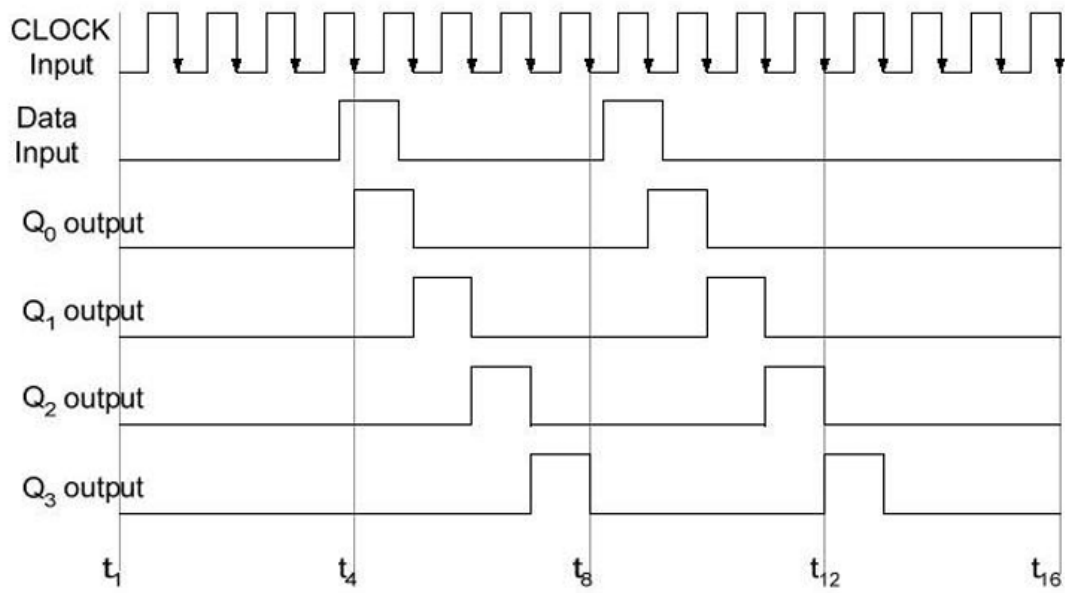
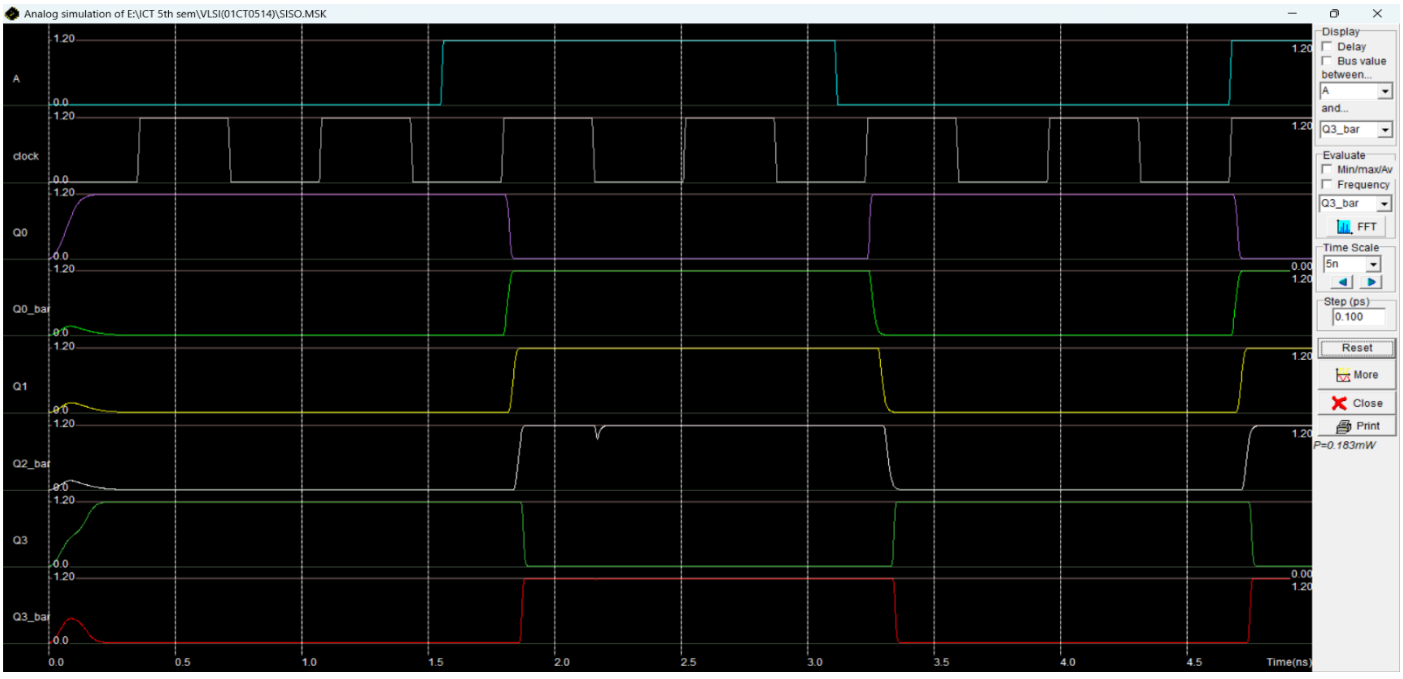
Timing Diagram:



Screenshots Of Layouts: -



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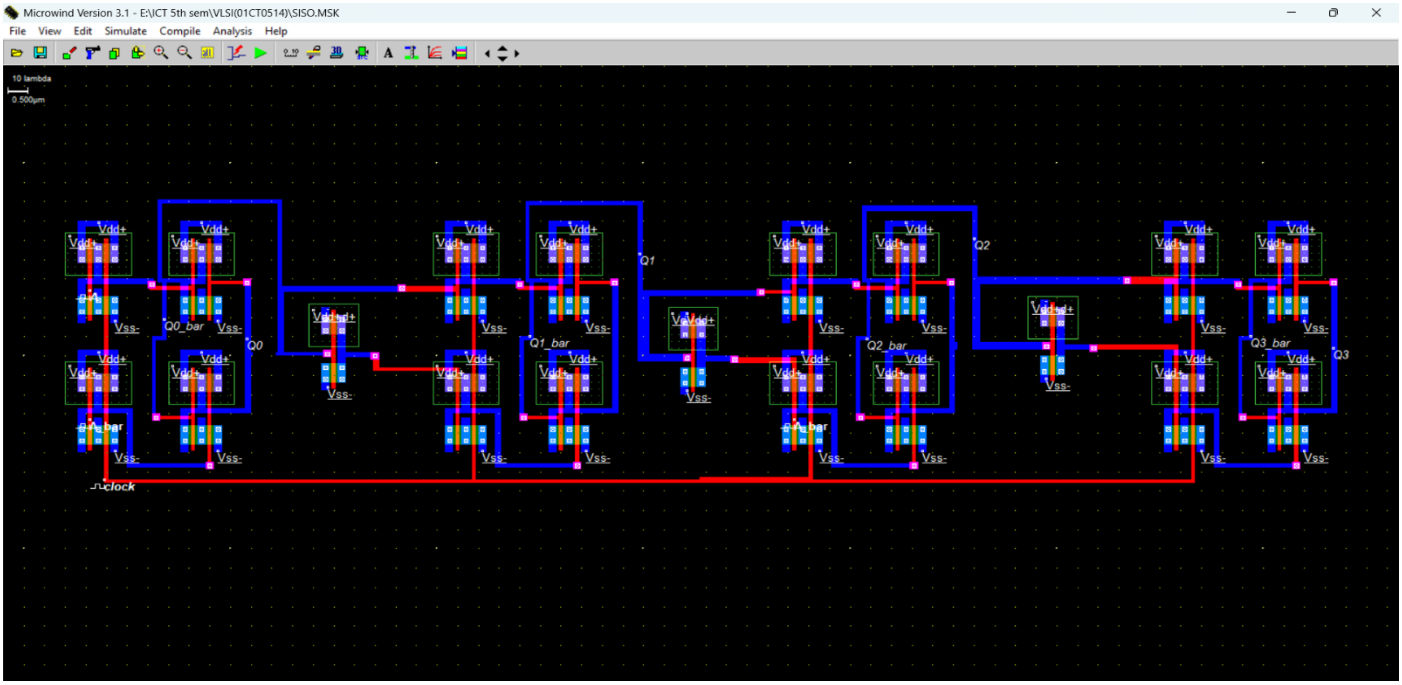

Conclusion

- Successfully designed and simulated four circuits in Microwind
- Learned transistor-level layout design and timing verification
- Future work: extend to larger adders, PIPO registers, multipliers