ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB MANUAL

ECL331

BY

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DEPARTMENT OF ECE

SREE BUDDHA COLLEGE OF ENGINEERING

PATTOOR

Department of Electronics and Communication Engineering

Sree Buddha College of Engineering, Pattoor

Vision

To nurture professionally competent and socially responsible Electronics and Communication Engineers

Mission

- Provide knowledge, facilities and value-based education for developing competent Engineers
- Promote industry-institute interaction, lifelong learning and research
- Inculcate ethical and interpersonal skills to address the societal needs

Program Educational Objectives (PEOs)

The graduates will:

- Acquire capability to analyze, formulate and solve problems in Electronics and Communication Engineering
- Develop a quest for lifelong learning, research and entrepreneurship for professional development
- Be motivated to address societal needs through sustainable and ethical practices

GENERAL RULES FOR PERSONAL SAFETY

1. Always wear tight shirt/lab coat, pants and shoes inside the lab.
2. REMOVE ALL METAL JEWELLERY since rings, wrist watches or bands, necklaces, etc. make excellent electrodes in the event of accidental contact with electric power sources.
3. DO NOT MAKE CIRCUIT CHANGES without turning off the power.
4. Make sure that equipment working on electrical power are grounded properly.
5. Avoid standing on metal surfaces or wet concrete. Keep your shoes dry.
6. Never handle electrical equipment with wet skin.
7. Hot soldering irons should be rested in its holder. Never leave a hot iron unattended.
8. Avoid use of loose clothing and hair near machines and avoid running around inside lab.

ECL331	ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble: This course aims to (i) familiarize students with the Analog Integrated Circuits and Design and implementation of application circuits using basic Analog Integrated Circuits (ii) familiarize students with simulation of basic Analog Integrated Circuits.

Prerequisite: ECL202 Analog Circuits and Simulation Lab

Course Outcomes: After the completion of the course the student will be able to

CO 1	Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs.
CO 2	Design and simulate the application circuits with Analog Integrated Circuits using simulation tools.
CO 3	Function effectively as an individual and in a team to accomplish the given task.

Mapping of course outcomes with program outcomes

	PO1	PO 2	PO3	PO 4	PO5	PO 6	PO7	PO8	PO9	PO 10	PO 11	PO 12
CO1	3	3	3						2			2
CO2	3	3	3	2	3				2			2
CO3	2	2	2		2				3	2		3

Assessment

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	3 hours

Continuous Evaluation Pattern

Attendance : 15 marks

Continuous Assessment : 30 marks

Internal Test (Immediately before the second series test) : 30 marks

End Semester Examination Pattern: The following guidelines should be followed regardingaward of marks

(a) Preliminary work : 15 Marks

(b) Implementing the work/Conducting the experiment : 10 Marks

(c) Performance, result and inference (usage of equipment and troubleshooting): 25 Marks

(d) Viva voce : 20 marks

(e) Record : 5 Marks

General instructions: End-semester practical examination is to be conducted immediatelyafter the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

LIST OF EXPERIMENTS

I. Fundamentals of operational amplifiers and basic circuits [Minimum seven experiments are to be done]

1. Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, frequency response, Adder, Integrator, Comparators.
2. Measurement of Op-Amp parameters.
3. Difference Amplifier and Instrumentation amplifier.
4. Schmitt trigger circuit using Op–Amps.
5. Astable and Monostable multivibrator using Op-Amps.
6. Wien bridge oscillator using Op-Amp - without & with amplitude stabilization.
7. RC Phase shift Oscillator.
8. Active second order filters using Op-Amp (LPF, HPF, BPF and BSF).
9. Precision rectifiers using Op-Amp.

II. Application circuits of 555 Timer/565 PLL/ Regulator (IC 723) ICs [Minimum three experiments are to be done]

1. Astable and Monostable multivibrator using Timer IC NE555
2. DC power supply using IC 723: Low voltage and high voltage configurations, Short circuit and Fold-back protection.
3. D/A Converters - R-2R ladder circuit.

III. Simulation experiments [The experiments shall be conducted using SPICE]

1. Simulation of any three circuits from Experiments 3, 5, 7, 8, 9and 11 of section I
2. Simulation of Experiments 3 from section II

I. Fundamentals of operational amplifiers and basic circuits

EXPERIMENTS-I-1

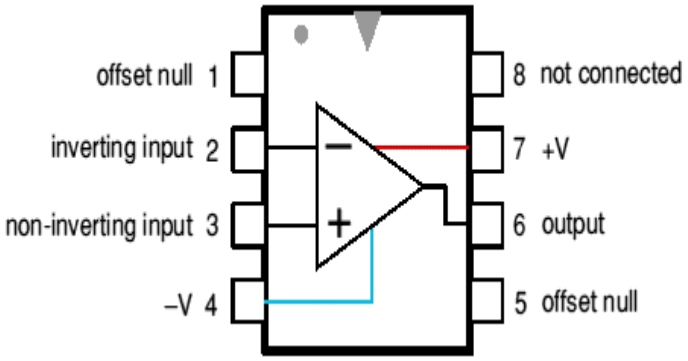
Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, frequency response, Adder, Integrator, Comparators.

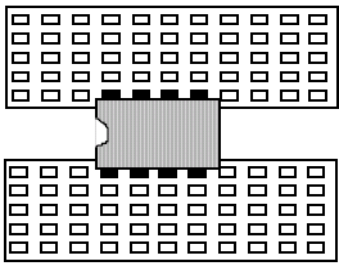
AIM: To familiarize with µC741C operational amplifier IC and its electrical characteristics.

1) FAMILIARIZATION OF OPERATIONAL AMPLIFIERS

AIM: To familiarize with µC741C operational amplifier IC and its electrical characteristics.

741 op amp IC





Insert the ICs (carefully to avoid bending their leads) into the wider strips, as shown above: Plug an op-amp into the breadboard so that it straddles the gap between the top and bottom sections of the socket strip.

If you have wired the power buses as suggested above, Pin 1 should be to the left.

Warning:

Do not try to unplug the op-amp with your thumb and forefinger. Use the IC puller or tip of a pen for unplugging.

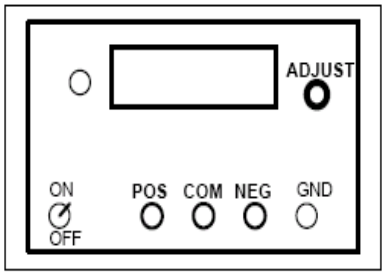
PARAMETER	IDEAL	GENERAL PURPOSE 741 OPAMP
Voltage Gain, A	∝	1×10^5
Output Impedance, Ro	0	75Ω
Input Resistance, R_{in}	∝	2MΩ
Offset Current, I_{io}	0	20nA
Offset Voltage, V_{io}	0	2mV
Bandwidth, BW	∝	1MHz
Slew rate, SR	∝	0.5 V/µs

Throughout this experiment use the external dual DC Power Supply Unit shown in figure below.

Use the dual trace oscilloscope to observe the shape and to measure the amplitude of the input and output waveforms.

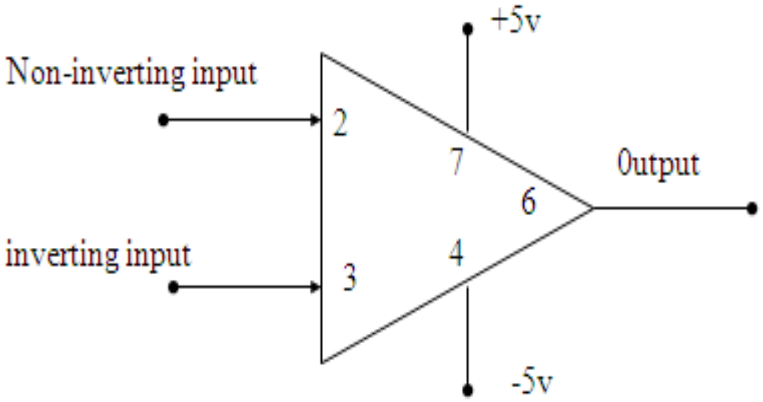
Connecting an Op-Amp to Power Supply Unit:

- Turn the Power Supply ON. Adjust the voltage of the Power Supply to 15V. This will set both positive and negative power sources respectively to +15V and –15V.
- Turn the Power Supply OFF before connecting to the circuits.
- Connect the **POS** terminal of the Power Supply to the **Vcc+** of your circuit. Connect the **NEG** terminal of the Power Supply to the **Vcc-** of your circuit. Connect the **COM** terminal of the Power Supply to the ground of your circuit.

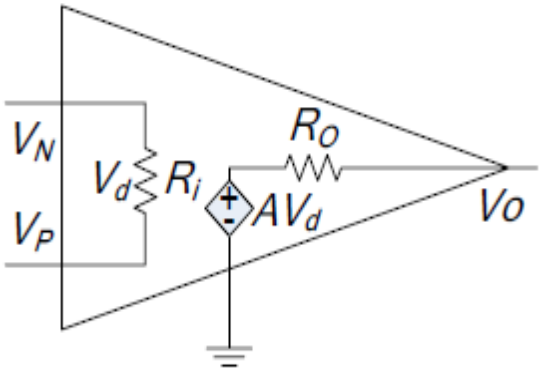


Front panel of power supply unit

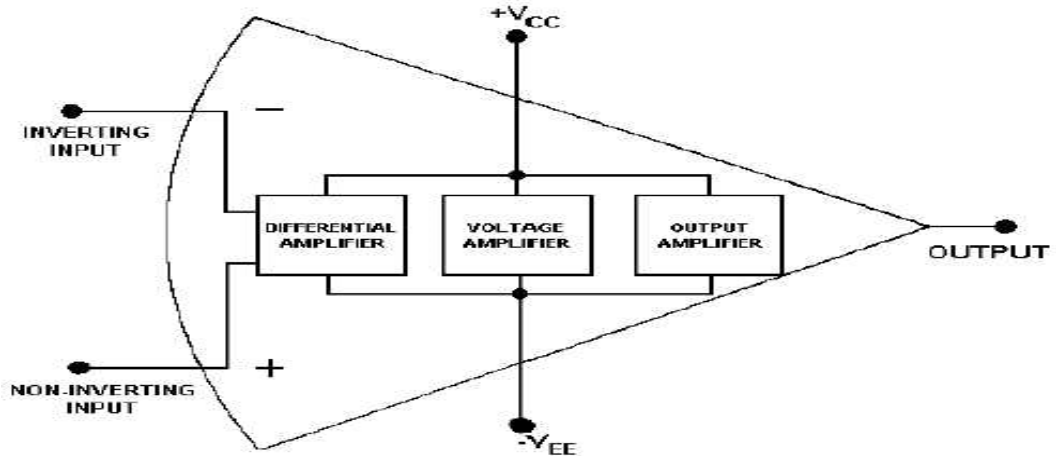
Symbol Of Op-Amp



A Equivalent Circuit Of An Op-Amp



A Internal block diagram of Op-Amp:

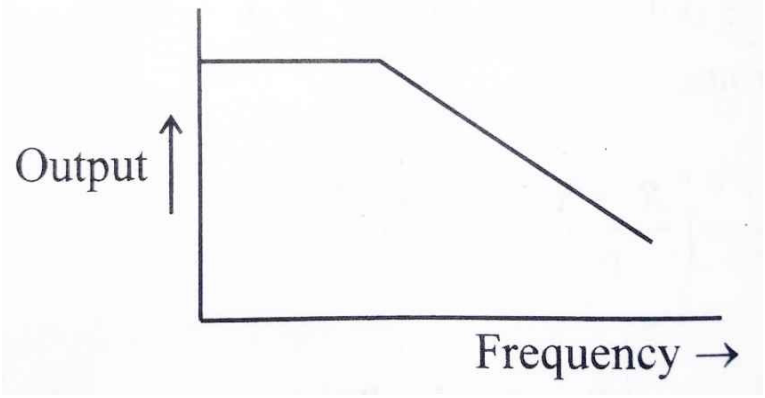


2) FREQUENCY RESPONSE OF AN OP-AMP

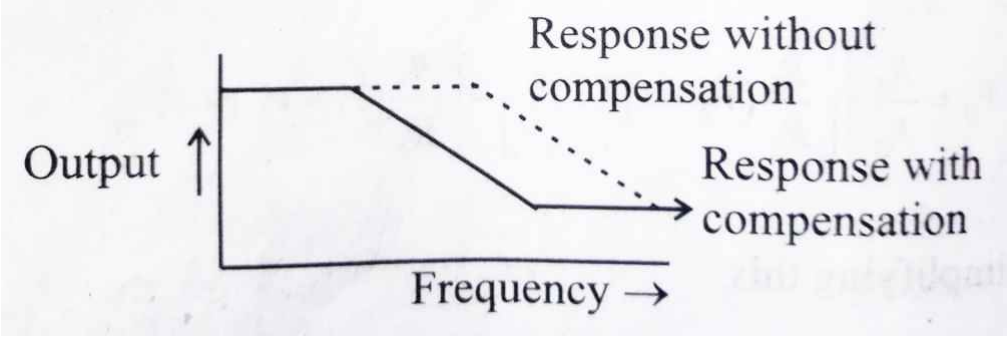
In an Op-Amp Bandwidth, frequency response & gain bandwidth product are key parameters for any circuit. Typically, Op-Amps are used for comparatively low frequency circuit but with the performance of these chips is improving all the time, much higher bandwidth Op-Amps are available.

The frequency response of a typical Op-Amp chip will often start to fall at a very low frequency when operated in its open loop mode. The point at which the frequency starts to roll off is known as break point.

Frequency compensation added in most of OP-AMP chips. It is introduced to ensure that they remain stable& do not produce unwanted high frequency spurious oscillations.



The frequency response of open loop OP-AMP is shown above



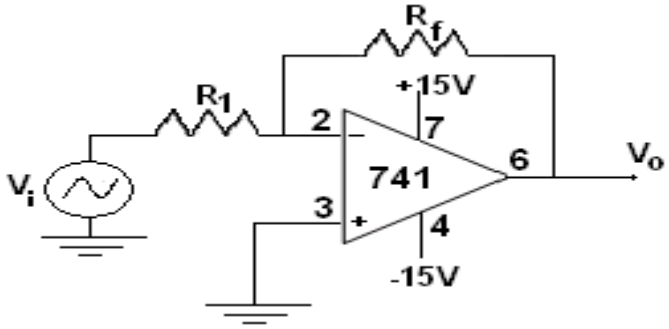
(Op-Amp frequency Response With & Without Frequency Compensation)

3) INVERTING, NON-INVERTING AMPLIFIER AND VOLTAGE FOLLOWER

Inverting Operational Amplifier

In the inverting operational amplifier circuit, the signal is applied at the inverting input and the non-inverting input is connected to the ground. In this type of amplifier, the output is 180º out of phase to the input, i.e., when positive signal is applied to circuit, the output of the circuit will be negative.

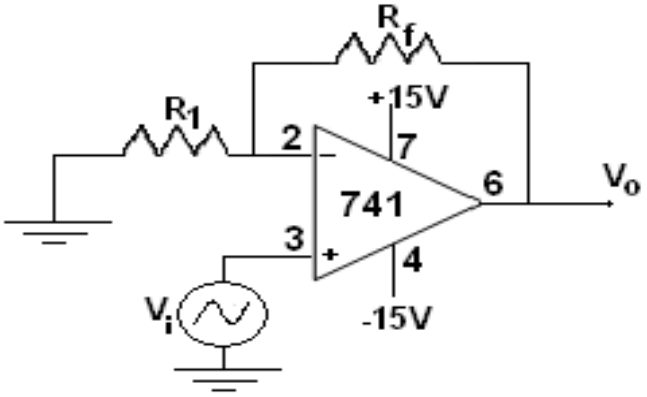
Circuit Diagram



Non-Inverting Operational Amplifier

When the signal is applied at the non-inverting input, the resulting circuit is known as Non-Inverting Op-Amp. In this amplifier the output is exactly in phase with the input i.e., when a positive voltage is applied to the circuit, the output will also be positive.

Circuit Diagram

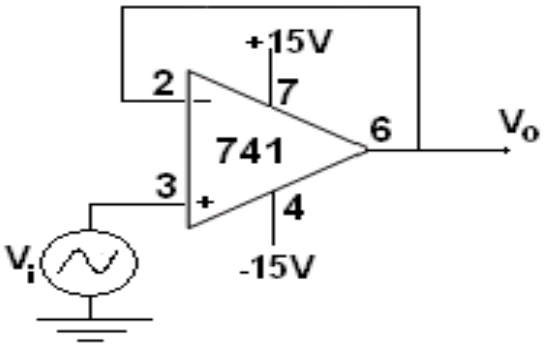


Voltage Follower

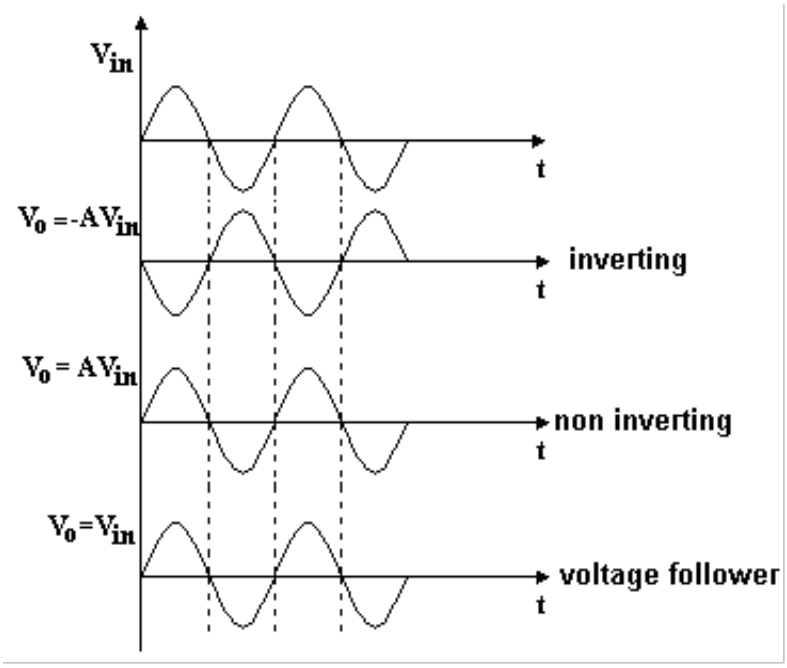
A voltage follower (also known as a buffer amplifier, unity-gain amplifier, or isolation amplifier) is an op-amp circuit whose output voltage is equal to the input voltage (it "follows" the input voltage). Hence a voltage follower op-amp does not amplify the input signal and has a voltage gain of 1.

The voltage follower provides no attenuation or amplification—only buffering.

Circuit Diagram



Model graph:



DESIGN:

I Inverting Amplifier

A = -Rf/R1 (Voltage gain)

Take A =5

Rf = 5R1

Choose Rf = 10kΩ, R1=2kΩ

II Non-Inverting Amplifier

$A = 1 + Rf/R1$

Take $A = 2$

$Rf = R1$

Choose $Rf = 10k\Omega$, $R1 = 10k\Omega$

PROCEDURE:

I Inverting Amplifier

1. Construct the inverting amplifier circuit shown in figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply 1V amplitude, 1 kHz sinusoidal input signal to the amplifier.
5. Observe the input and output waveforms simultaneously on CRO.
6. Compare the phase of input and output signals.
7. Record the output waveform amplitude.
8. Increase the amplitude of the input until distortion occurs at the output.
9. Record the corresponding output amplitudes and plot a graph of the output amplitude vs the input amplitude.

II Non-Inverting Amplifier

1. Construct the non-inverting amplifier as shown in the figure.
2. Apply 1V amplitude, 1 kHz sinusoidal input signal to the amplifier.
3. Observe V_{in} and V_o at the same time on the CRO.
4. Verify whether the output is in phase with the input.
5. Note down the output voltage by varying the frequency of the input signal.
6. Draw its frequency response characteristics.

III Voltage Follower

1. Wire up the voltage follower circuit.
2. Apply a sine wave of frequency 10 KHz, with amplitude of approximately 1.0 V to the circuit.
3. Observe V_{in} and V_o at the same time on the CRO.
4. Confirm that input and output amplitudes are equal.

OBSERVATION:

1) Inverting Amplifier

$V_i = 1V$

f (Hz)	Vo(V)	Av(dB)

2) Non inverting Amplifier

$V_i = 1V$

f (Hz)	Vo(V)	Av(dB)

3) Voltage follower

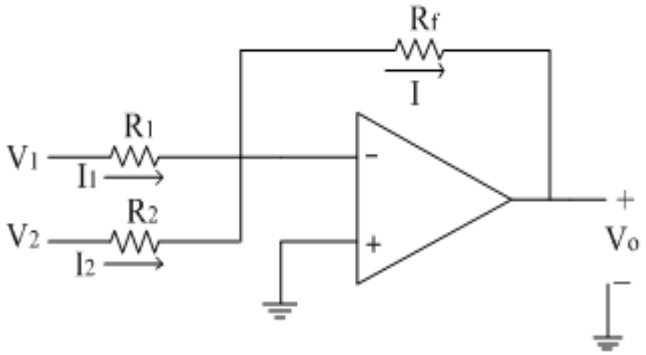
f (Hz)	Vin(V)	Vo(V)

4) ADDER, INTEGRATOR, COMPARATORS.

a) Adder: Adders are of two types Inverting and Non-Inverting type.

i)Inverting adder:

The input signals to be added are applied to the inverting input terminal of op-amp. The following figure shows the inverting adder using op-amp with two inputs V1 and V2.

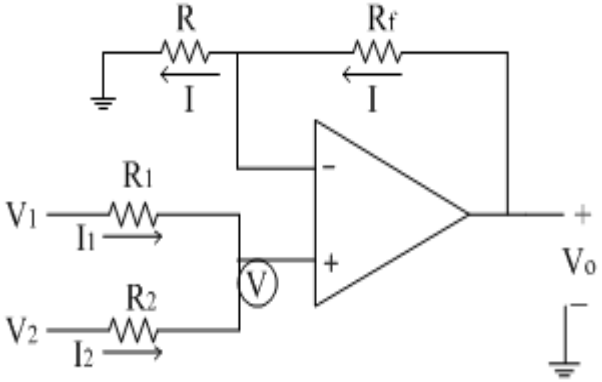


Here Vo is output and is defined by the formula

$$\boldsymbol{V_o = -\frac{R_f\,(V_1 + V_2)}{R_1}}$$

ii) Non-inverting adder:

The input signals to be added are applied to the non-inverting input terminal of op-amp. The following figure shows the non- inverting adder using op-amp with two inputs V1 and V2.



Here Vo is output and is defined by the formula

$$\boldsymbol{V_o = \left(1 + \frac{R_f}{R}\right)(V_1 + V_2)}$$

Here $\boldsymbol{R_1 = R_2 = R}$

OBSERVATION:

1)Inverting Adder

V1(V)	V2(V)	Vo(V)

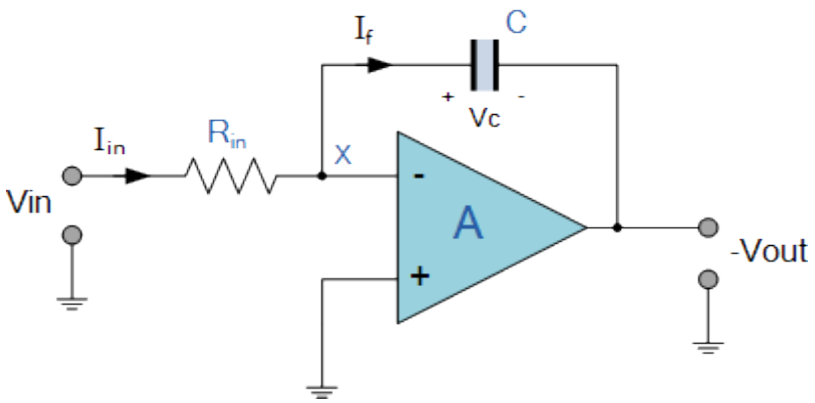
2) Non inverting Adder

V1(V)	V2(V)	Vo(V)

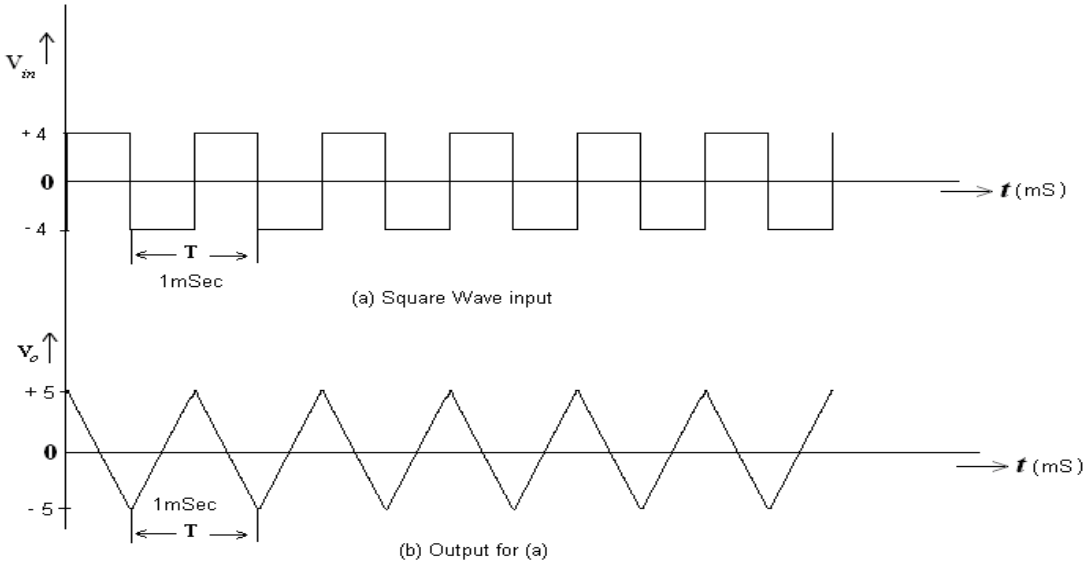
b) Integrator:

The Op-amp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration, that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

CIRCUIT DIAGRAM:



Model graph:



Design:

Given f =1 KHz

So, T = 1/f = 1ms

Design equation is T = 2πRinC

Let C = 0.01μF

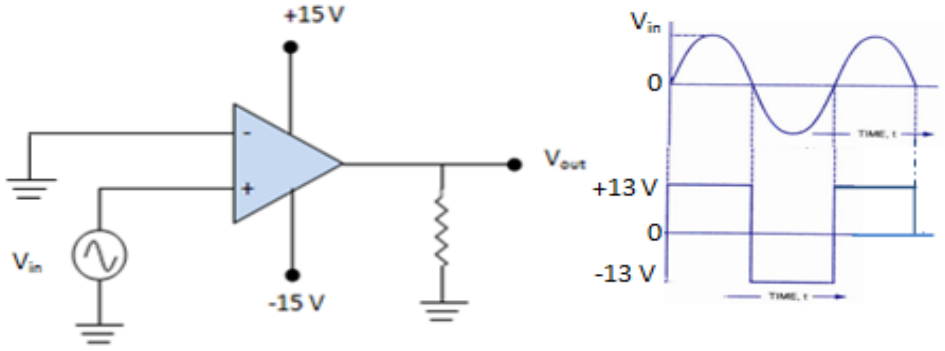
Then Rin = 15KΩ

c) Comparators:

The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two. There are three major types of comparators which will be discussed.

i) Zero crossing Detector:

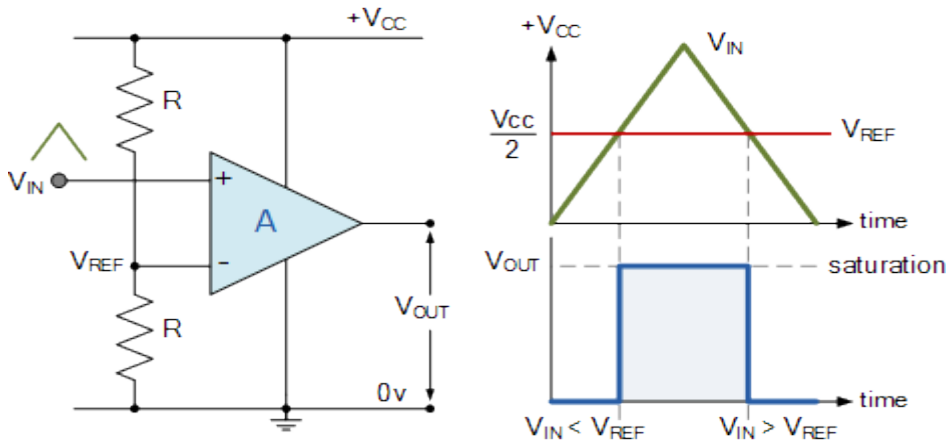
When one input of a comparator is connected to ground, it is known as zero crossing detector because the output changes when the input crosses 0 V. The zero-crossing circuit is shown in figure below with its input and output wave forms.



ii) Positive Voltage Comparator:

The basic configuration for the positive voltage comparator, also known as a non-inverting comparator circuit detects when the input signal, VIN is ABOVE or more positive than the reference voltage, VREF producing an output at VOUT which is HIGH as shown.

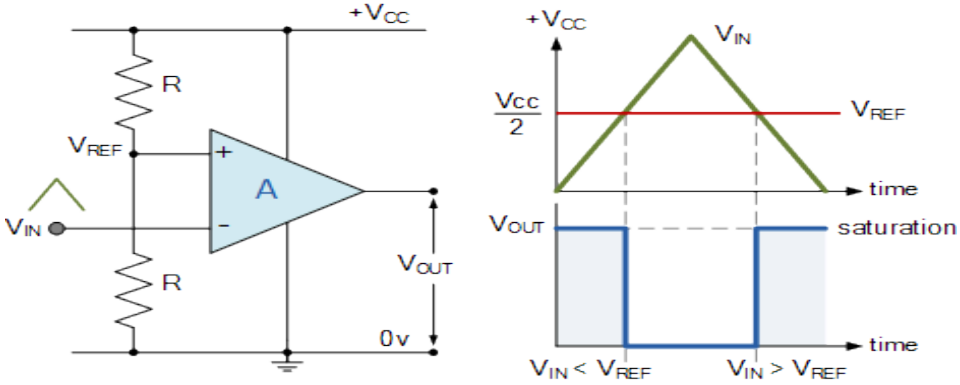
Non-inverting Comparator Circuit



iii) Negative Voltage Comparator

The basic configuration for the negative voltage comparator, also known as an inverting comparator circuit detects when the input signal, V_{IN} is BELOW or more negative than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

Inverting Comparator Circuit



RESULT:

EXPERIMENT-I-2

Measurement of Op-Amp parameters.

AIM: To measure the following parameters of an Op-amp

1. Input offset voltage
2. Input bias current
3. Input offset current
4. CMRR
5. Slew rate

The characteristics of an ideal op-amp are as follows:

(i) Infinite input resistance, Ri =∞
(ii) Zero output resistance, Ro = 0
(iii) Infinite voltage gain, Av =∞
(iv) Infinite bandwidth, BW = ∞
(v) Infinite common-mode rejection ratio, CMRR = ∞z
(vi) Infinite slew rate, SR = ∞
(vii) Zero offset, i.e., when V1 = V2, Vo = 0
(viii) Characteristics do not drift with temperature

1) Input offset voltage: Input offset voltage is the differential input voltage that exists between the inverting and non-inverting input terminals of an op-amp. In other words, this can be defined as the voltage that is to be applied between the two input terminals for making the output voltage zero.

2) Input bias current: The input bias current is the average of the currents that flow into the inverting and non-inverting input terminals of an op-amp.

3) Input offset current: The input transistors of an Op-Amp cannot be made identical, and there always exists a small difference between the bias currents IB1 and IB2. The difference in magnitude between IB1 and IB2 is called input offset current.

4) CMRR: It is is the ratio of the common-mode gain to differential-mode gain or in other words the ability of an Op-Amp to reject common mode signals.

PROCEDURE:

1) Input Offset Voltage

1. Connect the circuit as shown in figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Measure the output voltage and record the result in the table given.
5. Calculate the input offset voltage using the expression $V_{io} = \frac{V_o R_f}{(R_f + R_i)}$ where V_o= output voltage and V_{io}=input offset voltage.
6. Compare this value with the theoretical value.

2) Input Bias Current

1. Set up the circuit as shown.
2. Measure the output voltage and record it in the table given.
3. Calculate I_{B1} and I_{B2} using the expressions Vo = I_{B1}R. and Vo = I_{B2}R.
4. The input bias current can be calculated as I = (I_{B1}+I_{B2})/2.
5. Compare this value with the theoretical value.

3) Input Offset Current

1. Reconnect the circuit as shown.
2. Follow the above steps 2 and 3.
3. The input offset current can be calculated as I = I_{B1}-I_{B2}.
4. Compare this value with the theoretical value.

4) CMRR

1. Set up the circuit for finding CMRR.
2. Apply an ac signal of 0.5V as input and measure Vo.
3. Calculate the common mode gain, A_c=V_o/V_i and differential mode gain, A_d=R_f/R_1.
4. Then find CMRR as CMRR=A_d/A_c.
5. Express CMRR in dB using the expression 20 log (CMRR).
6. Choose Rf, Rcom =100KΩ and R1, R2=100Ω

5) Slew Rate

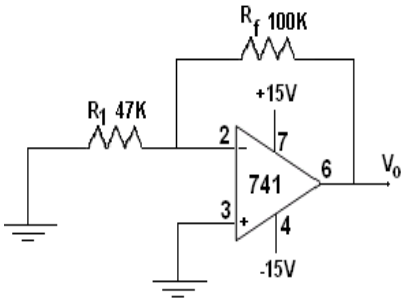
1. Connect the circuit as illustrated in figure.
2. Apply a 1 KHz, 1 Vp-p sinusoidal signal as input.
3. Vary the input frequency and observe the output voltage.
4. Note down the frequency at which the output gets disturbed.
5. Record the values in the table.
6. Measure the slew rate using the expression, SR=$\frac{2\pi f V_m}{10^{-6}}$ V/ μs.

Slew rate can also be measured using a zero-crossing detector. For that

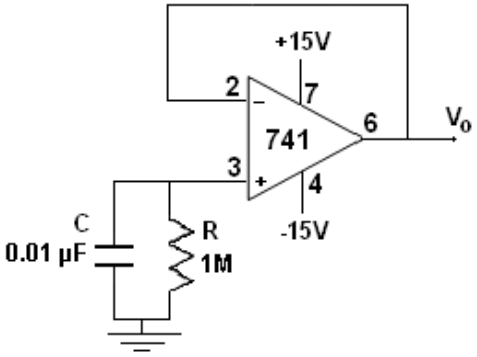
1. Feed a square wave as input.
2. Increase the frequency until rising and trailing edges of the output square wave becomes slanting or
   the output voltage from the square wave looks like a triangular wave.
3. Slew rate can be obtained from the slope of trailing or leading edge as SR=$\frac{\Delta V_o}{\Delta t}$.

CIRCUIT DIAGRAM

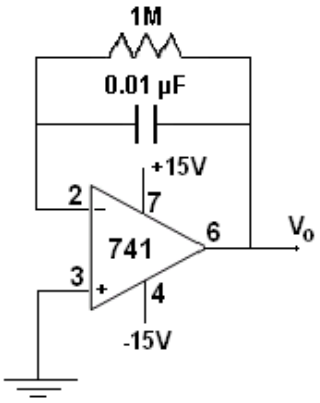
Input Offset Voltage



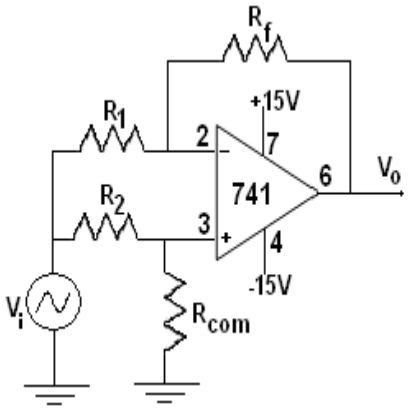
Bias current Ib1



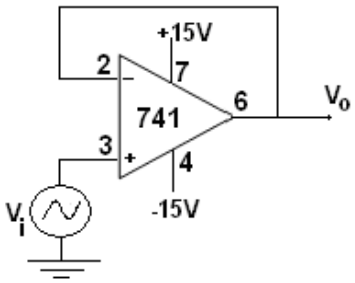
Bias current Ib2



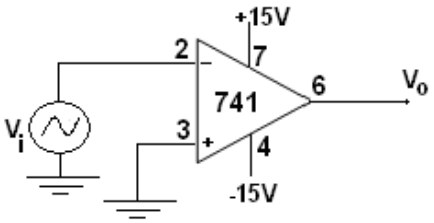
CMRR



Slew Rate



Slew Rate



OBSERVATION:

1. Input Offset Voltage

	V_o(mV)	V_{io}(mV)
Theoretical Value		
Actual Value		

2. Input bias current

	Vo(V)	I_{B1}(nA)	I_{B2}(nA)	I(nA)
Theoretical Value				
Actual Value				

3. Input offset current

	Vo(V)	I_{B1}(nA)	I_{B2}(nA)	I(nA)
Theoretical Value				
Actual Value				

4. CMRR

	A_c	A_d	CMRR	CMRR (dB)
Theoretical Value				
Actual Value				

5. Slew Rate

	V_m(V)	ΔVo(V)	Δt(μs)	SR(V/μs)
Theoretical Value				
Actual Value				

CALCULATIONS:

RESULT:

EXPERIMENT-I-3

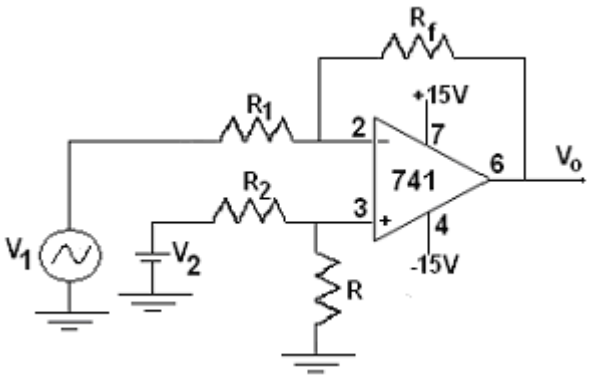
Difference Amplifier and Instrumentation amplifier

AIM 1: To design and set up the Difference Amplifier circuits

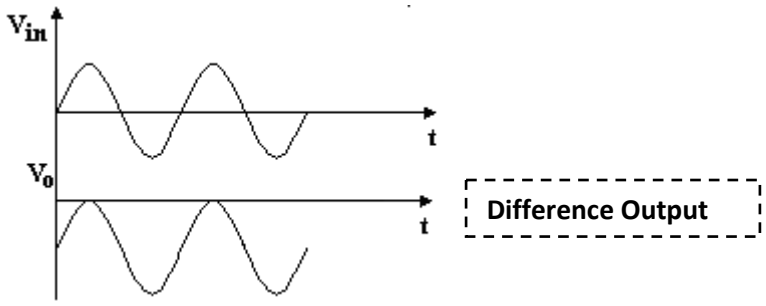
DIFFERENCE AMPLIFIERS:

A difference amplifier is a special purpose amplifier designed to measure differential signals, otherwise known as a subtractor. A key feature of a difference amplifier is its ability to remove unwanted common mode signals, known as common mode rejection (CMR). Unlike most types of amplifiers, difference amplifiers are typically able to measure voltages beyond the supply rails, and are used in applications where large dc or ac common-mode voltages are present. They are ideal for current and voltage monitoring.

Circuit Diagram:



Model Graph:



DESIGN:

Assume $R_1 = R_2$ and $R_f = R$

$$Vo = \frac{R_f}{R_1}(V_2 - V_1)$$

PROCEDURE:

1. Set up a difference amplifier circuit as shown in figure.
2. With V_i adjusted to produce a 1 V peak sine wave at 1 kHz, observe the output voltage V_O (and V_i to note the phase relationship) on an oscilloscope.
3. Sketch the output voltage waveform. Be sure to note the dc level in the output.
4. Interchange the 5 V dc power supply and the 1 V peak signal generator. Repeat procedure step 3.
5. Measure Vout for three or four different values of V1 and V2, and verify that $V_o = (V_1 - V_2)$

CALCULATIONS:

OBSERVATION:

V1(V)	V2(V)	Vo(V)

RESULT:

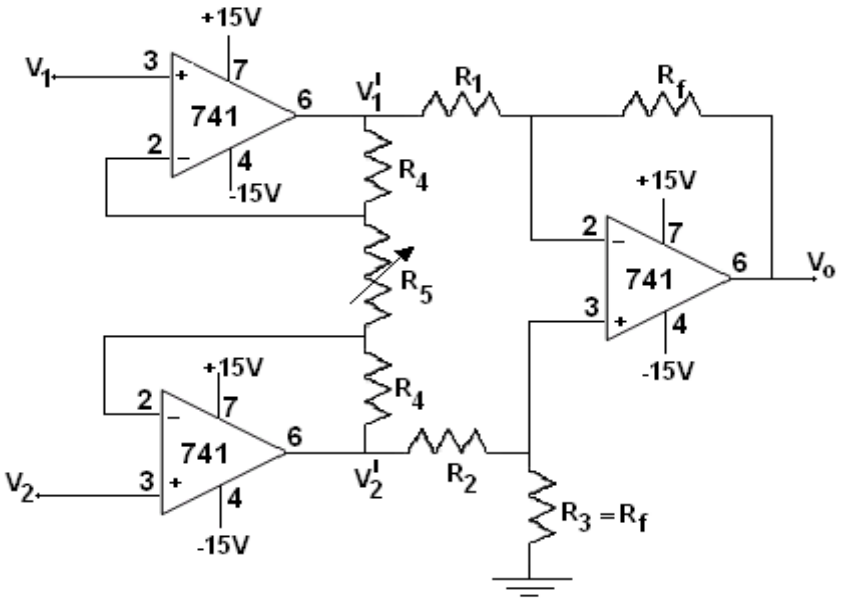
AIM 2: To design and set up an instrumentation amplifier using three op-amps to obtain an overall gain of 900 given input signal amplitude is 15mV and to measure the CMRR.

INSTRUMENTATION AMPLIFIERS:

Instrumentation Amplifiers are basically used to amplify small differential signals. Instrumentation Amplifier provides the most important function of Common-Mode Rejection (CMR). It cancels out any signals that have the same potential on both the inputs. The signals that have a potential difference between the inputs get amplified.

An Instrumentation Amplifier (In-Amp) is used for low-frequency signals (≪1 MHz) to provide a large amount of Gain. It amplifies the input signal rejecting Common-Mode Noise that is present in the input signal.

Circuit Diagram:



DESIGN:

Let Av1= Av2= 3

Here Av1= $A_{Vdiff} = \dfrac{2R4 + R5}{R5}$

$R4 = 1k\Omega$

$R5 = 1k\Omega pot$

Choose

$Av2 = 3$ And $Rf = 3k\Omega$

R1=R2=1kΩ

Rf=R3=3KΩ

$$R1 = \frac{Rf}{Av2} = 1\text{k}\Omega$$

PROCEDURE:

1) Verify whether the op-amps are in good condition.
2) Manually trace the circuit to check the correctness of physical connection.
3) Calibrate the CRO.
4) Set up V_1=0.5V dc and V_2=0.4V dc and measure output voltage on CRO keeping R_5 in maximum position
5) Repeat the step 4 by keeping R_5 in minimum position. Note down the increase in gain. This is the difference mode gain, A_d.

$$A_d = \frac{V_{od}}{V_{id}}$$

6) Feed V_1=V_2=0.5V and observe the gain keeping R_5 in minimum position. This is the common mode gain A_c.

$$A_c = \frac{V_{oc}}{V_{ic}}$$

7) Calculate CMRR from the relation CMRR=20 log (A_d/A_c).

OBSERVATION:

Common Mode Gain

V_i(V)	V_o(V)	A_c

Differential Mode Gain

V_i(V)	V_o(V)	A_d

CALCULATION:

CMRR =

RESULT:

EXPERIMENT-I-4

Schmitt Trigger circuit using Op–Amps

AIM: To design and set up an inverting Schmitt Trigger using op-amp for an LTP = 2V and a UTP = 3V.

SCHMITT TRIGGER:

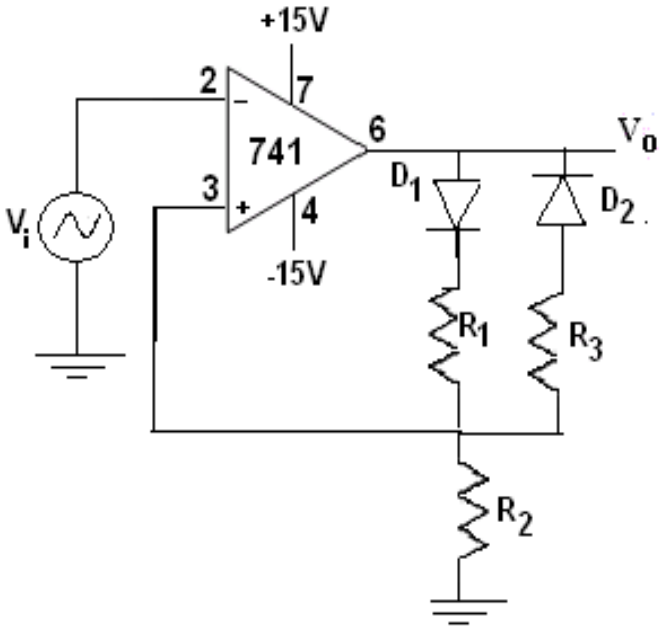
Schmitt Trigger was invented by Otto Schmitt in early 1930's. It is an electronic circuit that adds hysteresis to the input-output transition threshold with the help of positive feedback. Hysteresis here means it provides two different threshold voltage levels for rising and falling edge.

Essentially, a Schmitt Trigger is a Bi-stable Multivibrator and its output remains in either of the stable states indefinitely. For the output to change from one stable state to other, the input signal must change (or trigger) appropriately.

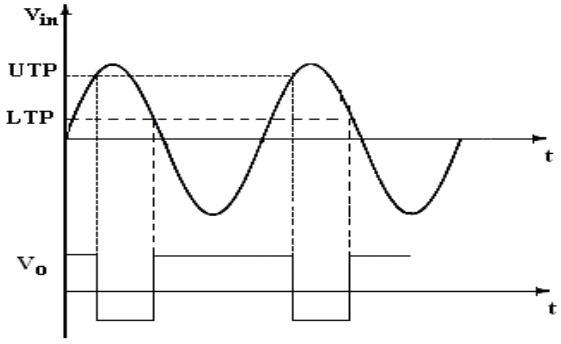
This Bistable operation of the Schmitt Trigger requires an amplifier with positive feedback (or regenerative feedback) with a loop gain greater than one. Hence, Schmitt Trigger is also known as Regenerative Comparator.

Note: A square wave generator.

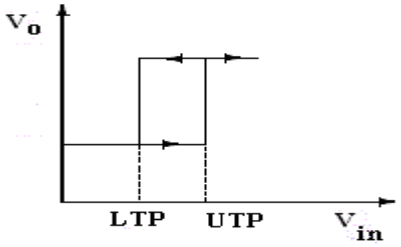
CIRCUIT DIAGRAM



MODEL GRAPH



Hysteresis curve



DESIGN:

Assume $|V_o|$ = Vcc-1V = ± 14v

$$\text{UTP} = \frac{(|V_o| - V_F) \times R2}{R1 + R2}$$

$$\text{LTP} = \frac{(|V_o| - V_F) \times R2}{R3 + R2}$$

Here $R2 = \frac{V_{R2}}{I_2}$

Where V_{R2} is either UTP or LTP

I_2 is assumed as 50μ

PROCEDURE:

1. Make connections according to the circuit diagram.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Adjust the signal generator to produce a 5Vp-p, 1 KHz sine wave as the input.
5. Verify the input and output simultaneously on CRO.
6. Measure and record the output amplitude and frequency.
7. Observe the hysteresis curve on CRO by keeping the time/div knob of CRO in x-y mode and feed V_{in} to the x-channel and V_o to the y-channel.

CALCULATIONS:

RESULT:

EXPERIMENT-I-5

Astable and Monostable multivibrator using Op-Amps

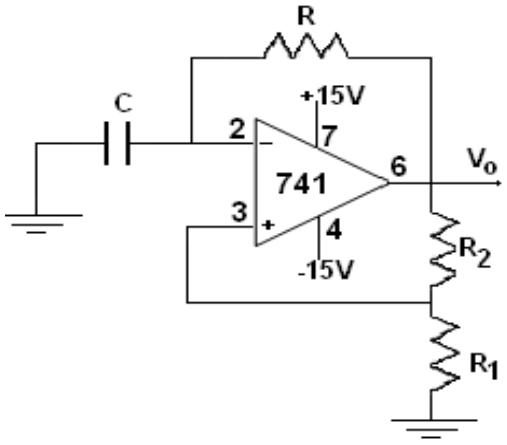
AIM 1: To design and set up an astable multivibrator circuit using op amp whose frequency of operation = 1 KHz.

ASTABLE MULTIVIBRATOR:

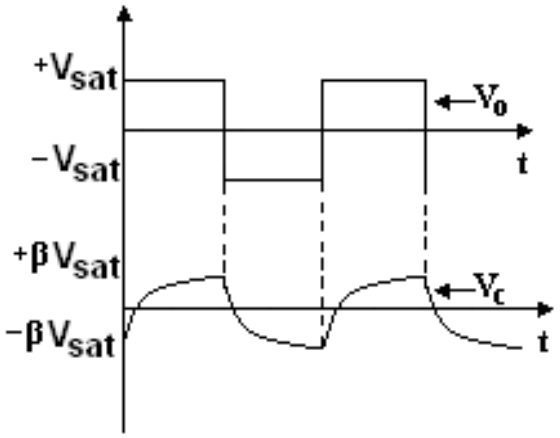
An astable multivibrator is a type of multivibrator that does not require a triggering pulse thus, sometimes known as a free-running multivibrator. It necessarily provides square wave as its output.

Astable multivibrator is called so because both the states present here are unstable i.e., quasi-stable. Here, the successive transition is made from one quasi-state to other after some pre-decided time interval.

CIRCUIT DIAGRAM



MODEL GRAPH



PROCEDURE:

1. Give the circuit connections as per the circuit diagram.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.

4. Observe the output from CRO.
5. Sketch the capacitor and output waveforms.
6. Measure the time period of the output voltage waveform and compare it with the designed value.
7. Repeat the procedure for different duty cycles.

DESIGN:

Use $R2 = 1.16R1$ for equation $f_o = \frac{1}{2RC}$ to be used

Let $R1 = 10k\Omega$ Then

R2= 11.6kΩ

Choose C=0.05μF and find R

R=10kΩ

OBSERVATION:

	No: of Divisions		Time/div (ms)	Volt/div (V)	Amp(V)	Time Period (ms)
	X axis	Y axis				
Output Voltage						
Voltage across capacitor						

Calculations:

RESULT:

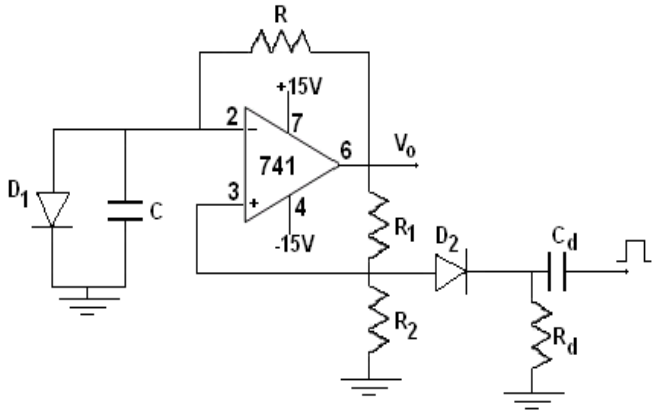
AIM 2: To design a monostable mutivibrator circuit for a pulse width of 2ms.

MONOSTABLE MULTIVIBRATOR:

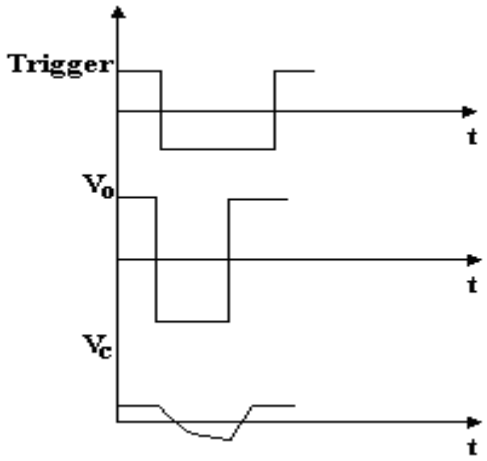
Op-amp Monostable Multivibrator (one-shot multivibrator) circuits are positive-feedback (or regenerative) switching circuits that have only one stable state, producing an output pulse of a specified duration T.

An external trigger signal is applied for it to change state and after a set period of time, either in microseconds, milliseconds or seconds, a time period which is determined by RC components, the monostable circuit then returns back to its original stable state where it remains until the next trigger input signal arrives.

CIRCUIT DIAGRAM



MODEL GRAPH



PROCEDURE:

1. Construct the circuit connections as per the circuit diagram.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Adjust the signal generator to produce a 2V p-p, 200Hz square wave at the trigger input.
5. Observe the output from CRO.
6. Sketch the input and output waveforms.

7. Measure the pulse width of the output voltage waveform and compare it with the designed value.

DESIGN:

Assume R1=R2 so that β=0.5

Where $\beta=\frac{R_2}{R_1+R_2}$

Thus, pulse width is given by

T= 0.69RC

The differentiator is designed by

RdCd ≤ 0.0016T

Let T= 3ms and Cd = 0.01 μF; then Rd = 470Ω

D1 & D2 are diodes 1N 4001

OBSERVATION:

	No: of Divisions		**Time/div (ms)**	**Volt/div (V)**	**Amp(V)**	**Time Period (ms)**
	X axis	**Y axis**				
Output Voltage						
Voltage across capacitor						

CALCULATION:

RESULT:

EXPERIMENT-I-6

Wien bridge oscillator using Op-Amp - without & with amplitude stabilization

AIM: To design and set up a Wien Bridge oscillator with and without amplitude stabilization using an op-amp for a frequency = 2 KHz.

WIEN BRIDGE OSCILLATOR:

It is an oscillator which uses RC network so as to produce a sine wave at the output. These are basically the low-frequency oscillator that generates audio and sub audio frequency that ranges between 20 Hz to 20 KHz.

This oscillator circuit uses the Wien bridge to provide feedback with the desired phase shift. It gives highly stable oscillation frequency and does not vary much with supply or temperature variation. The Wien bridge circuit that we use is a lead-lag network as with the rise in frequency phase shift lags and with the reduction in frequency, it leads.

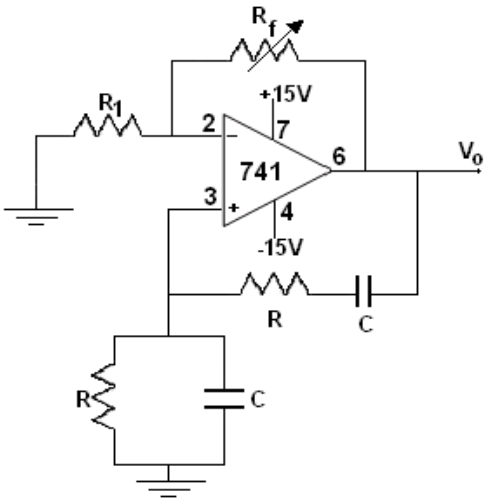
Need for Amplitude stabilization:

The Wien Bridge RC oscillators are not suitable for high frequency applications above 1MHz, due to the fact that the phase-shift through the amplifier and the phase-shift of the lead-lag circuit jointly cause resonance to occur at different frequencies other than the specified resonant frequency.

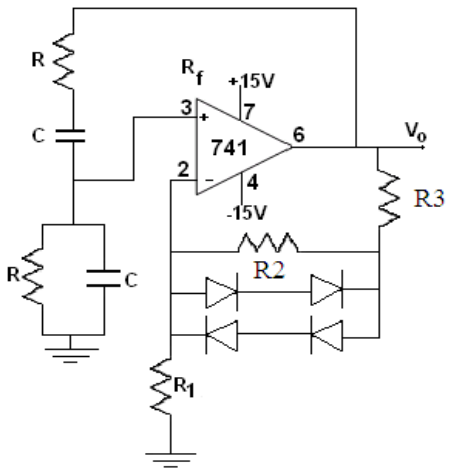
To maintain a stable amplitude for the oscillations, the resistor shown in figure is normally replaced by a non-linear resistor. This adjusts the loop gain based on the existing amplitude of oscillations. When the amplitude increases, it causes a rise in the current through R1 which in turn rises the value of R1. It actually means an increased amount of negative feedback results in a corresponding reduction in loop gain and oscillation amplitude.

CIRCUIT DIAGRAM

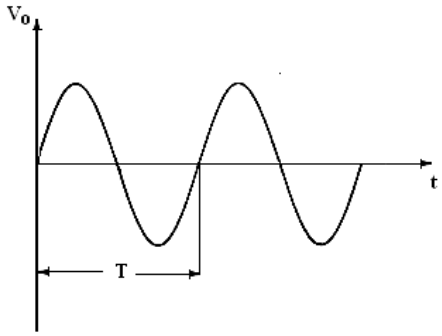
WBO without Amplitude Stabilization



WBO with Amplitude Stabilization



MODEL GRAPH:



PROCEDURE:

1. Check whether the op-amp is in good condition.
2. The circuit connections are given as per the circuit diagram.
3. Manually trace the circuit to check the correctness of physical connection.
4. Calibrate the CRO.
5. Observe the output waveform on the CRO and measure the amplitude and time period of the sine wave.
6. Plot the output waveform.
7. Set up the circuit for amplitude stabilization.
8. Adjust the potentiometer to get the sine wave without any distortion and clipping.
9. Repeat the steps 5 and 6.

DESIGN:

I) Design of Wien Bridge oscillator without amplitude stabilization

The frequency of oscillation is given by

$$f = \frac{1}{2\pi CR}$$

Assume C=0.01μF

Therefore R=1.592KΩ use approx. value 1.8KΩ

$R_f = 2R_1 = 3.6k\Omega$ Use standard value 3.3 $k\Omega$

II) Design of Wien Bridge oscillator with amplitude stabilization using Diodes

Here Rf =R2+R3

For sustained oscillation $A_V = 1 + \frac{R_F}{R_1}$ should be 3

Assuming R1=1.8KΩ we get R_F =3.6KΩ

$R_2 = \frac{2V_F}{I_1}$ Assuming I_1=1mA, R2=1.4KΩ.

Thus R3=2.2kΩ

OBSERVATION:

No: of Divisions		Time/div (ms)	Volt/div (V)	Amp(V)	Time Period (ms)
X axis	Y axis				

CALCULATION:

RESULT:

EXPERIMENT-I-7

RC Phase shift Oscillator

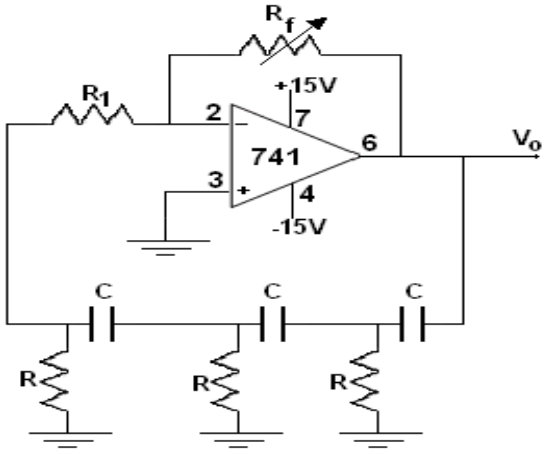
AIM: To design and set up an RC phase shift oscillator using op-amp whose frequency of oscillation = 1 KHz.

RC PHASE-SHIFT OSCILLATORS:

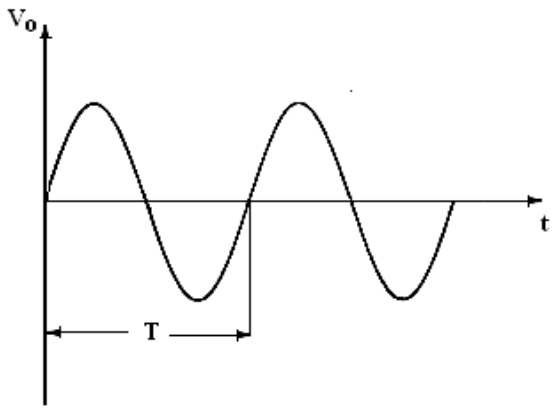
RC phase-shift oscillators use resistor-capacitor (RC) network to provide the phase-shift required by the feedback signal. They have excellent frequency stability and can yield a pure sine wave for a wide range of loads. Ideally a simple RC network is expected to have an output which leads the input by 90°.

However, in reality, the phase-difference will be less than this as the capacitor used in the circuit cannot be ideal. In oscillators, these kind of RC phase-shift networks, each offering a definite phase-shift can be cascaded so as to satisfy the phase-shift condition led by the Barkhausen's Criterion.

CIRCUIT DIAGRAM:



MODEL GRAPH:



PROCEDURE:

1. Check whether the op-amp is in good condition.
2. The circuit connections are given as per the circuit diagram.
3. Manually trace the circuit to check the correctness of physical connection.
4. Calibrate the CRO.
5. The amplitude and frequency of the sine wave is noted and the waveform is drawn.

DESIGN:

Assume C=0.1μF

The frequency of oscillation is given by

$$f_o = \frac{1}{2\pi\sqrt{6}RC}$$

Therefore R=650Ω

To prevent the RC network from loading the amplifier it is selected such that $R_1 > 10R$

Thus, we get R_1=6.5KΩ

$R_f = 29R_1$=188KΩ assume approximate value

OBSERVATION:

No: of Divisions		Time/division	Volt/division	Amp(V)	Time(ms)
X axis	Y axis				

CALCULATIONS:

RESULT:

EXPERIMENT-I-8

Active second order filters using Op-Amp (LPF, HPF, BPF and BSF).

AIM 1: To design and set up a second order low pass filter for a cut off frequency f_o = 1 KHz.

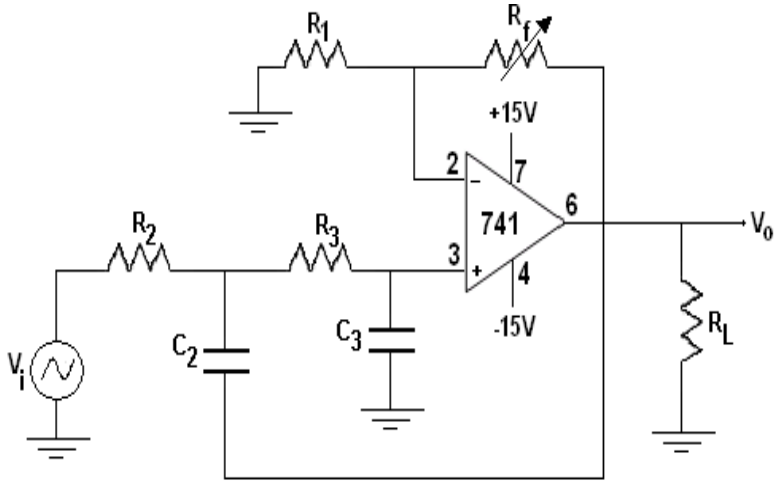
ACTIVE FILTER:

An active filter is a type of filter that includes one or more active circuit components such as a transistor or an operational amplifier (Op-Amp). They derive their energy from an external source of energy and use it to increase or amplify the signal output.

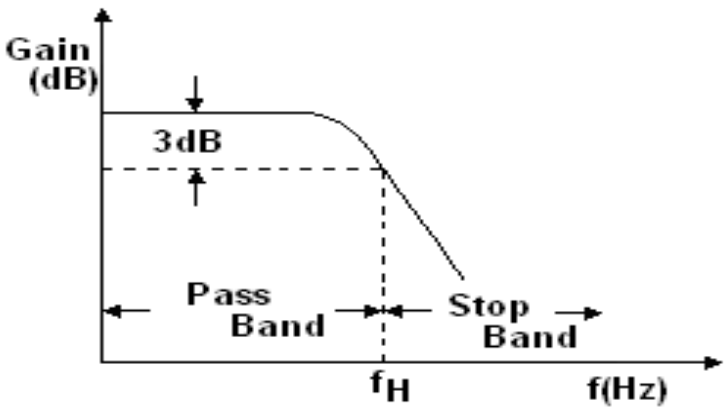
ACTIVE LOW PASS FILTER:

If an active filter permits only low-frequency components and denies all other high-frequency components, then it is termed as an Active Low Pass Filter. Active low pass filters are made up of Op-Amp. The input to the Op-Amp is high impedance signals, which produces a low impedance signal as output.

CIRCUIT DIAGRAM



MODEL GRAPH



DESIGN:

Assume $C_2 = 0.01\mu$ F, f = 1K Hz

$XC_1 = R_2.$

$$\frac{1}{2\Pi f C_2} = R_2.$$

$$R_2 = \frac{1}{2\Pi f C_2} \Rightarrow R_2. = 11.6K\Omega$$

$$R_3 = R_2. = 11.6K\Omega \cong 10K\Omega + 1K\Omega$$

$$C2 = C_3 = 0.01\mu \text{ F}$$

for second order

$$\left[1 + \frac{RF}{R1}\right] = 1.586$$

Assume $R1 = 10K\Omega$

$\Rightarrow$ then $RF = 5.86K\Omega \cong 5.6K\Omega + 270\Omega$

PROCEDURE:

1. Construct the second order low pass filter circuit shown in the figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply a 1V, 100 Hz sinusoidal input signal and note down the output displayed on the oscilloscope.
5. Keeping the input amplitude constant increase the frequency of the input signal.
6. Record the output voltage and frequency on the tabular column.
7. Plot the frequency response characteristics and mark the filter cut off frequency.

OBSERVATION:

V_{in}=1V

f(Hz)	Vo (V)	Av(dB)

CALCULATIONS:

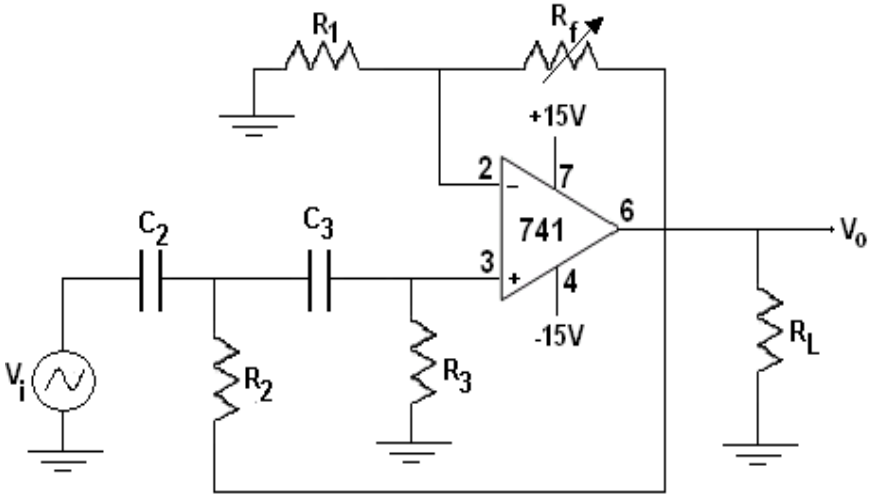
RESULT:

AIM 2: To design and set up a second order high pass filter for a cut off frequency f_o = 1 KHz.

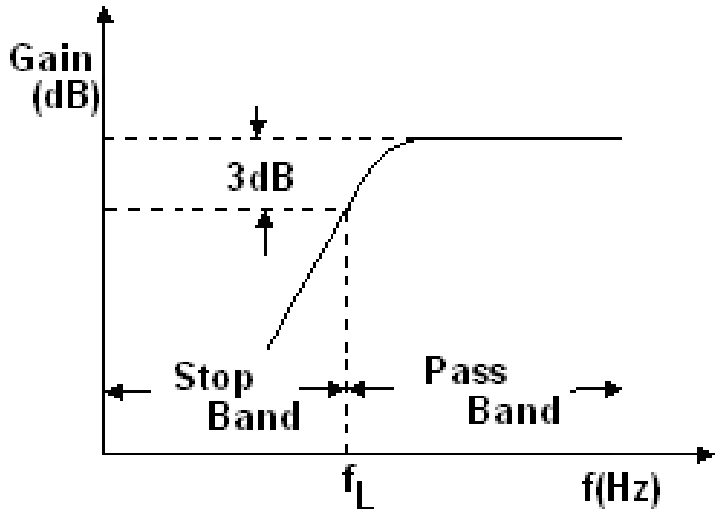
ACTIVE HIGH PASS FILTER:

An active high pass filter is nothing but a circuit contains an active component such as a transistor, an operational amplifier(op-amp), etc. These components are mainly used for better performance or better amplification.

CIRCUIT DIAGRAM:



MODEL GRAPH:



DESIGN:

Assume $C_2 = 0.01\mu$ F, f = 1K Hz

$XC_1 = R_2.$

$$\frac{1}{2\Pi f C_2} = R_2.$$

$$R_2 = \frac{1}{2\Pi f C_2} \Rightarrow R_2. = 11.6K\Omega$$

$$R_3 = R_2. = 11.6K\Omega \cong 10K\Omega + 1K\Omega$$

$$C2 = C_3 = 0.01\mu \text{ F}$$

for second order

$$\left[1 + \frac{RF}{R1}\right] = 1.586$$

Assume $R1 = 10K\Omega$

$\Rightarrow$ then $RF = 5.86K\Omega \cong 5.6K\Omega + 270\Omega$

PROCEDURE:

1. Construct the second order high pass filter circuit shown in the figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply a 1V, 100 Hz sinusoidal input signal and note down the output displayed on the oscilloscope.
5. Keeping the input amplitude constant increase the frequency.
6. Record the output voltage and frequency on the tabular column.
7. Plot the frequency response characteristics and mark the filter cut off frequency.

OBSERVATION:

V_{in}=1V

f(Hz)	Vo (V)	Av(dB)

CALCULATIONS:

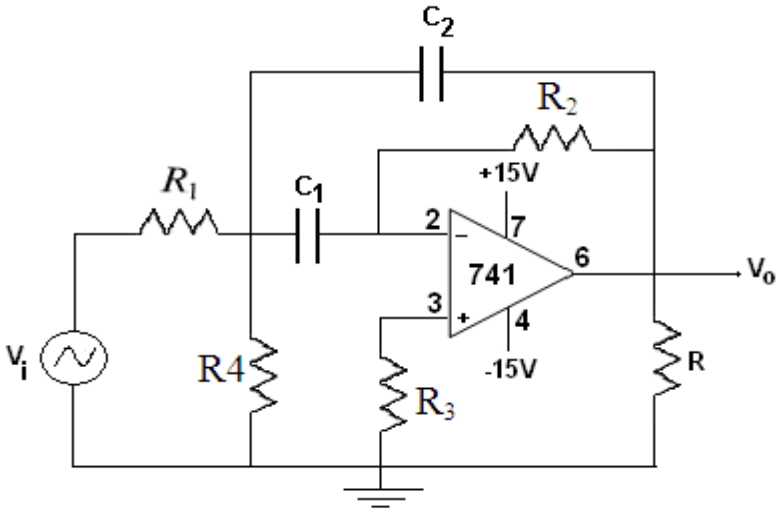
RESULT:

AIM 3: To design and set up a second order band pass filter for a center frequency f_o = 1 KHz and a pass band of Approximately $\pm 33Hz$ on each side of 1 KHz.

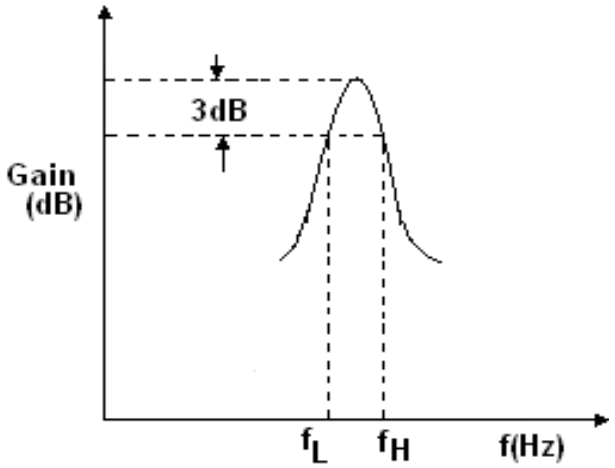
BANDPASS FILTER:

A bandpass filter is an electronic device or circuit that allows signals between two specific frequencies to pass, but that discriminates against signals at other frequencies. Some bandpass filters require an external source of power and employ active components such as transistors and integrated circuits; these are known as active bandpass filters. Other bandpass filters use no external source of power and consist only of passive components such as capacitors and inductors; these are called passive bandpass filters.

CIRCUIT DIAGRAM:



MODEL GRAPH:



DESIGN:

$$R_1 = \frac{R_2}{2}$$

$\boldsymbol{R_2 = 2QX_C}$ at f_o

$$R_4 = \frac{R_1}{2Q^2 - 1}$$

From given above B= 66Hz

Q= $\frac{f_o}{B} = 15.2$

Assume $R_3 = R_2$ =120KΩ

Thus C= $\frac{2Q}{2\pi f_o R_2} = 0.0403\mu F$

Choose the value of C1 = C2 = C

$$R_1 = \frac{R_2}{2}$$

= 60KΩ

$$R_4 = \frac{R_1}{2Q^2 - 1}$$

= 130.13Ω (use 150Ω standard value)

PROCEDURE:

1. Construct the second order band pass filter circuit shown in the figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply a 1V, 100 Hz sinusoidal input signal and note down the output displayed on the oscilloscope.
5. Vary the input frequency keeping the input amplitude constant.
6. Record the output voltage and frequency on the tabular column.
7. Plot the frequency response characteristics and mark the filter cut off frequency.

OBSERVATION:

V_{in}=1V

f(Hz)	Vo (V)	Av(dB)

CALCULATIONS:

RESULT:

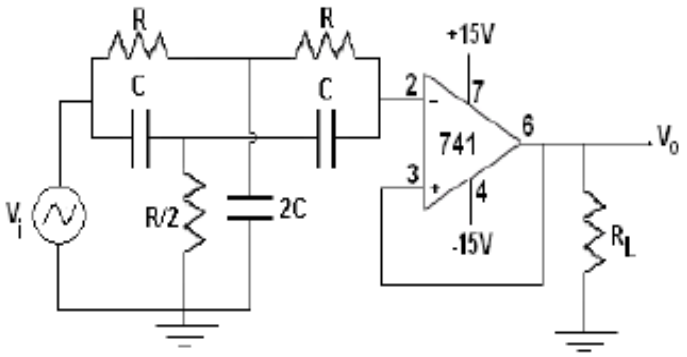
AIM 4: To design and set up a second order band pass filter for a cut off frequency $f_N = 1$ KHz

BAND STOP FILTER:

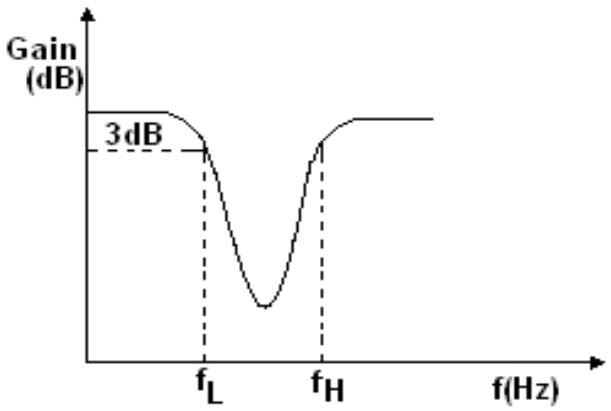
The Band Stop Filter, (BSF) is another type of frequency selective circuit that functions in exactly the opposite way to the Band Pass Filter we looked at before. The band stop filter, also known as a band reject *filter*, passes all frequencies with the exception of those within a specified stop band which are greatly attenuated.

If this stop band is very narrow and highly attenuated over a few hertz, then the band stop filter is more commonly referred to as a *notch filter*, as its frequency response shows that of a deep notch with high selectivity (a steep-side curve) rather than a flattened wider band.

CIRCUIT DIAGRAM:



MODEL GRAPH:



DESIGN:

Assume C=0.01μF

$$f_N = \frac{1}{2\pi RC}$$

The value of is calculated by

$$R = \frac{1}{2\pi f_N C}$$

For R/2 use two R resistors in parallel for 2C connect two resistors in parallel.

PROCEDURE:

1. Construct the second order notch filter circuit shown in the figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply a 1V, 100 Hz sinusoidal input signal and note down the output displayed on the oscilloscope.
5. Vary the input frequency keeping the input amplitude constant.
6. Record the output voltage and frequency on the tabular column.
7. Plot the frequency response characteristics and mark the filter cut off frequency.

OBSERVATION:

V_{in}=1V

f(Hz)	Vo (V)	Av(dB)

CALCULATIONS:

RESULT:

EXPERIMENT-I-9

Precision rectifiers using Op-Amp.

AIM: To design and set up precision half wave and full wave rectifier circuits.

Precision Rectifier:

The major limitation of conventional rectifiers is that it cannot rectify AC voltages below forward voltage drop VD (0.7V) of a diode. The precision rectifier will make it possible to rectify input voltage of a very small magnitude even less than forward voltage drop of diode. The diode can be used in AM detector where power is negligible and we want information in the signal. Rectifier circuits used for circuit detection with op-amps are called precision rectifiers.

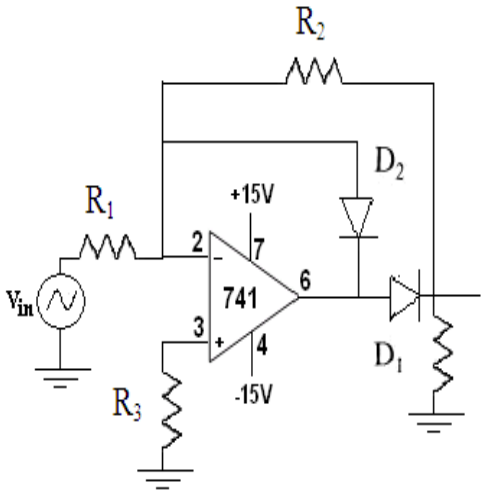
When forward biased voltage is less than 0.7V, then diode is not conducting. In case of normal power rectifier input applied is much larger than 0.7V. So diode is not operated. Therefore Op-amp is used to help diode to conduct.

The precision rectifiers are classified in two categories.

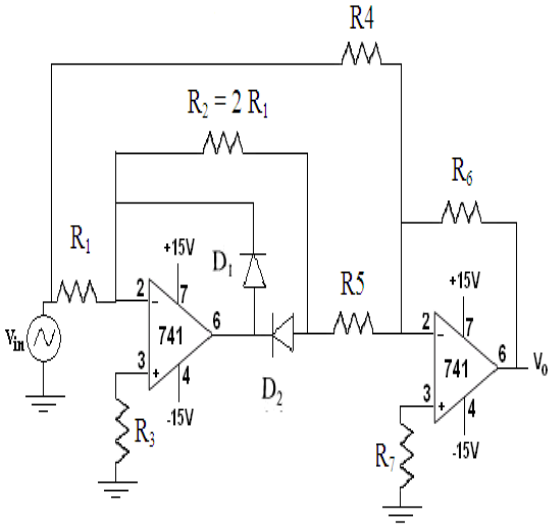
1. Precision HWR
2. Precision FWR

CIRCUIT DIAGRAM:

Half Wave Rectifier

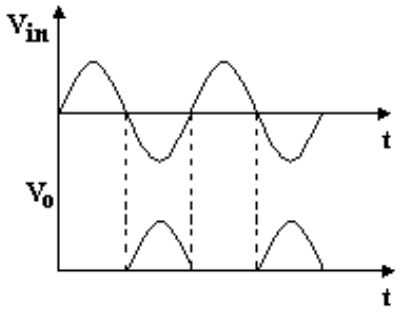


Full Wave Rectifier

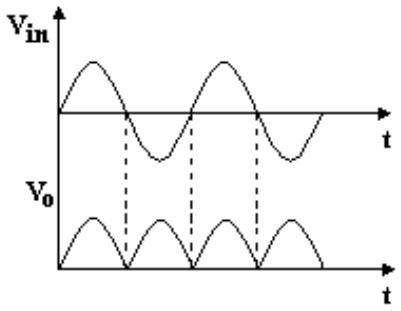


MODEL GRAPH:

Half Wave Rectifier



Full Wave Rectifier



DESIGN:

I) For Half Wave Rectifier

To produce a 2V peak output from a sine wave input with a peak value of 0.5V and frequency of 1 KHz.

Let $I_1 = 500\mu A$

$$R_1 = \frac{Vi}{I_1} = \frac{0.5V}{500\mu A} = 1k\Omega \quad \text{and} \quad R_2 = \frac{Vo}{I_1} = \frac{2V}{500\mu A} = 4k\Omega \text{ (use } 3.9k\Omega \text{ standard value)}$$

$R_3 = R1 \,||\, R_2 = 1k\Omega \,||\, 3.9k\Omega = 796\Omega$ (use 820Ω standard value).

II) For Full Wave Rectifier

To produce a 2V peak output from a sine wave input with a peak value of 0.5V and frequency of 1 KHz.

Let $I_1 = 500\mu A$

$$R_1 = \frac{Vi}{I_1} = \frac{0.5V}{500\mu A} = 1k\Omega \text{ and } \quad R_2 = 2\,R_1 = 2K\Omega \text{ (use } 1.8K\Omega \text{ standard value)}$$

$R_3 = R1 \,||\, R_2 = 1k\Omega \,||\, 2k\Omega = 670$ (use 680Ω standard value)

$R_4 = R_5 = R_1 = 1K\Omega$

For the output to be 2V when the input is 0.5V

$$R_6 = \frac{Vo}{V_I} \times R_5 = \frac{2V}{0.5V} \times 1K\Omega = 4k\Omega \text{ (use } 3.9k\Omega \text{ standard value)}$$

$$R_7 = R4 \,||\, R_5 \,||\, R_6 = 1k\Omega \,||\, 1k\Omega \,||\, 3.9k\Omega = 443\Omega \text{ (use } 470\Omega \text{ standard value)}$$

PROCEDURE:

a) Half Wave Rectifier

1. The connections are given as per the circuit diagram.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. A sine wave input in the order of mill volts is fed from the function generator.
5. The voltage and time period of the input and rectified waveforms are measured.
6. Plot the input and output waveforms.

b) Full Wave Rectifier

1. The connections are given as per the circuit diagram.
2. A sine wave input in the order of mill volts is fed from the function generator.
3. The voltage and time period of the input and rectified waveforms are measured.
4. Plot the input and output waveforms.

OBSERVATION:

No: of Divisions		Time/div (ms)	Volt/div (V)	Amp(V)	Time Period (ms)
X axis	Y axis				

CALCULATIONS:

RESULT:

II. Application circuits of 555 Timer / Regulator (IC 723) ICs

EXPERIMENT-II-1

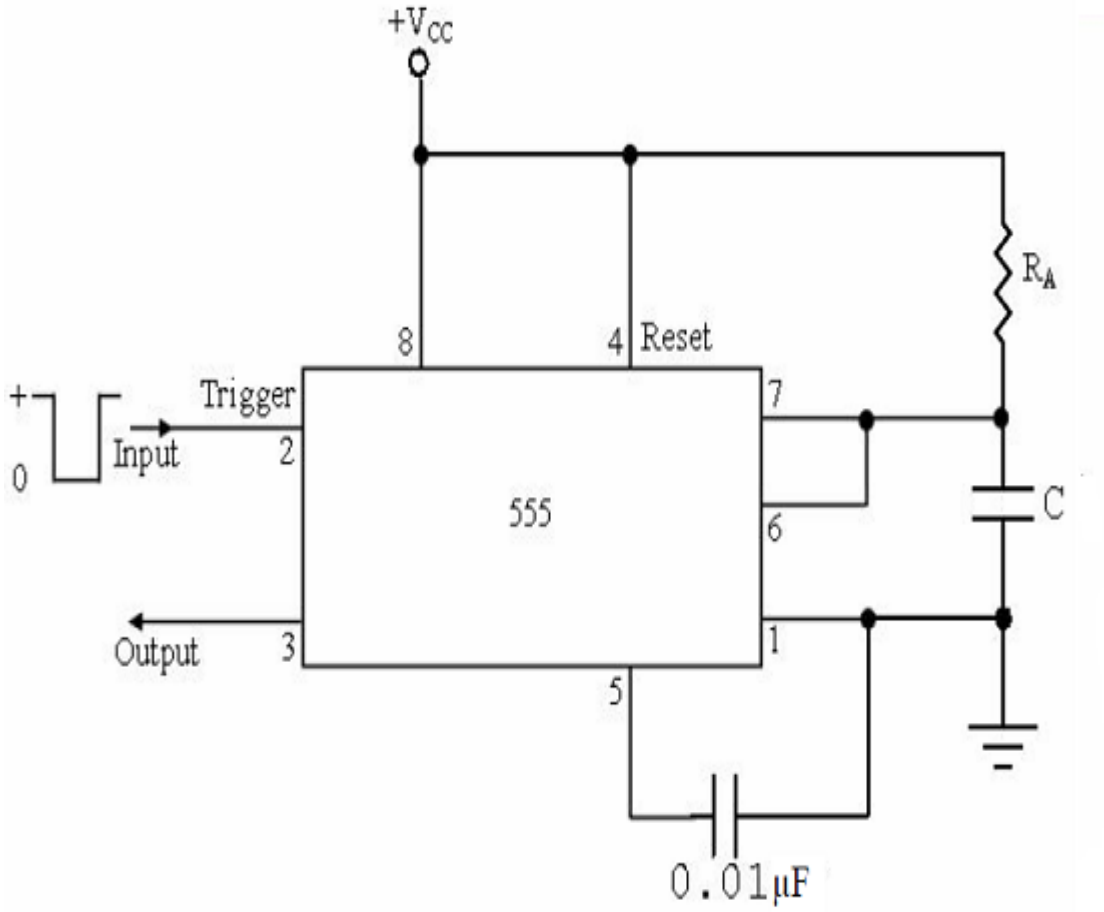
Astable and Monostable multivibrator using Timer IC NE555

NE555 Timer IC:

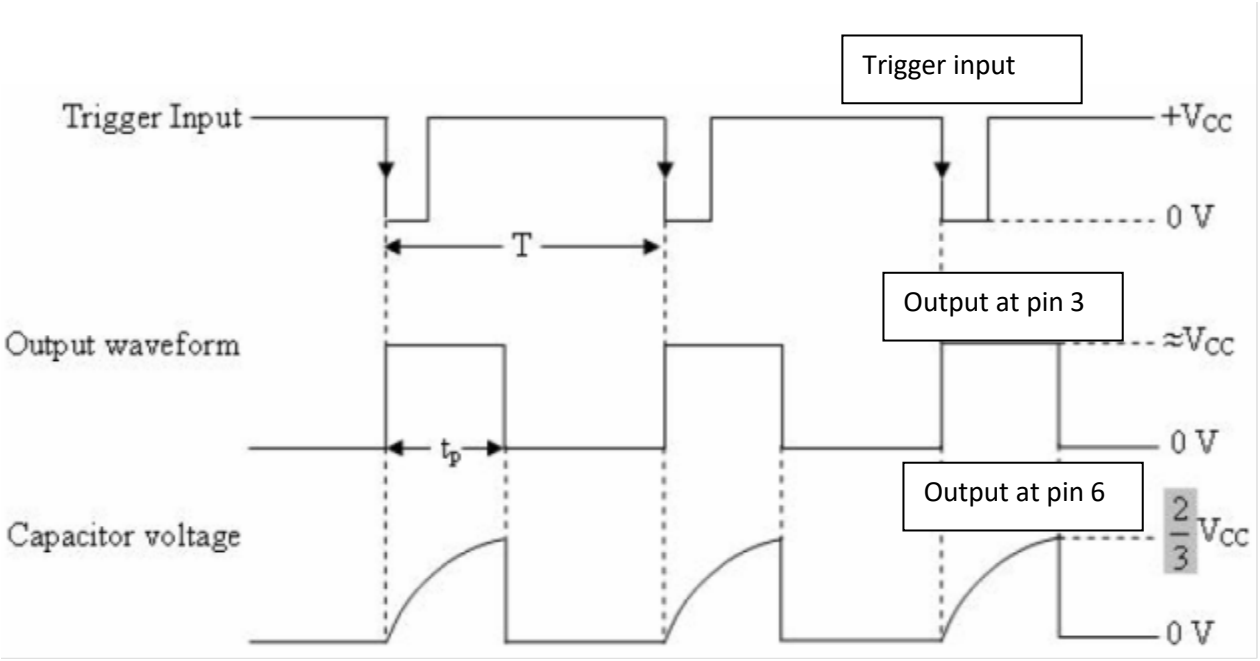
The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For Astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

AIM 1: To design and set up a monostable multivibrator using 555 timer Ic to obtain a 70% duty cycle.

CIRCUIT DIAGRAM



MODEL GRAPH:



DESIGN: Monostable multivibrator for T = 1ms

$$T \Rightarrow 1.1RC$$
$$C = 0.1\mu F$$
$$R_A = \frac{1m}{0.1\mu * 1.1} \approx 10K\Omega$$

PROCEDURE:

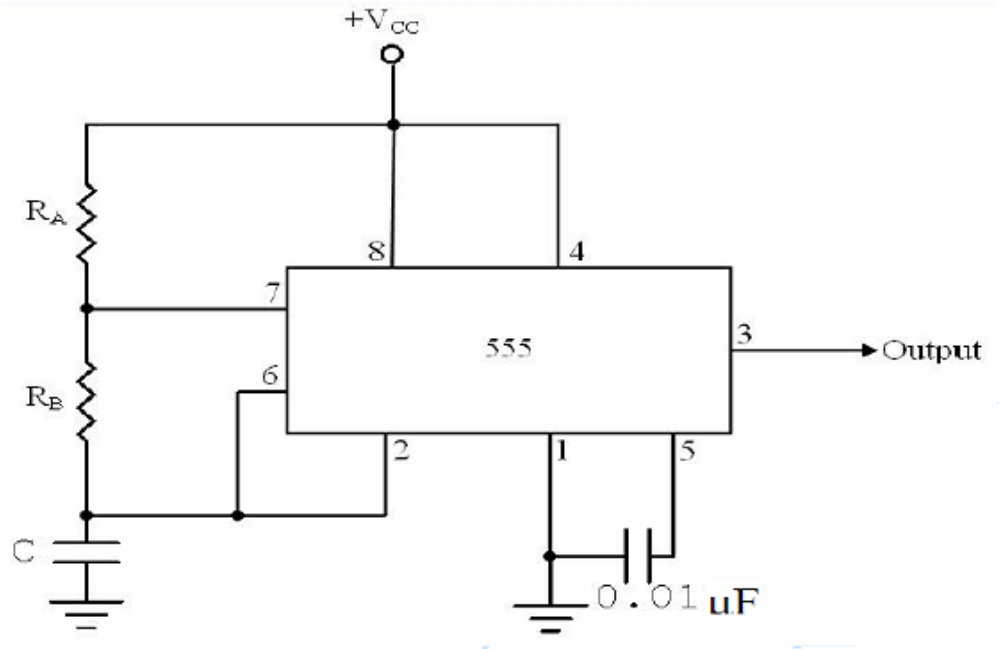
1. Assemble the circuit as illustrated in figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Observe the corresponding output of the op amp for different digital inputs.

CALCULATION:

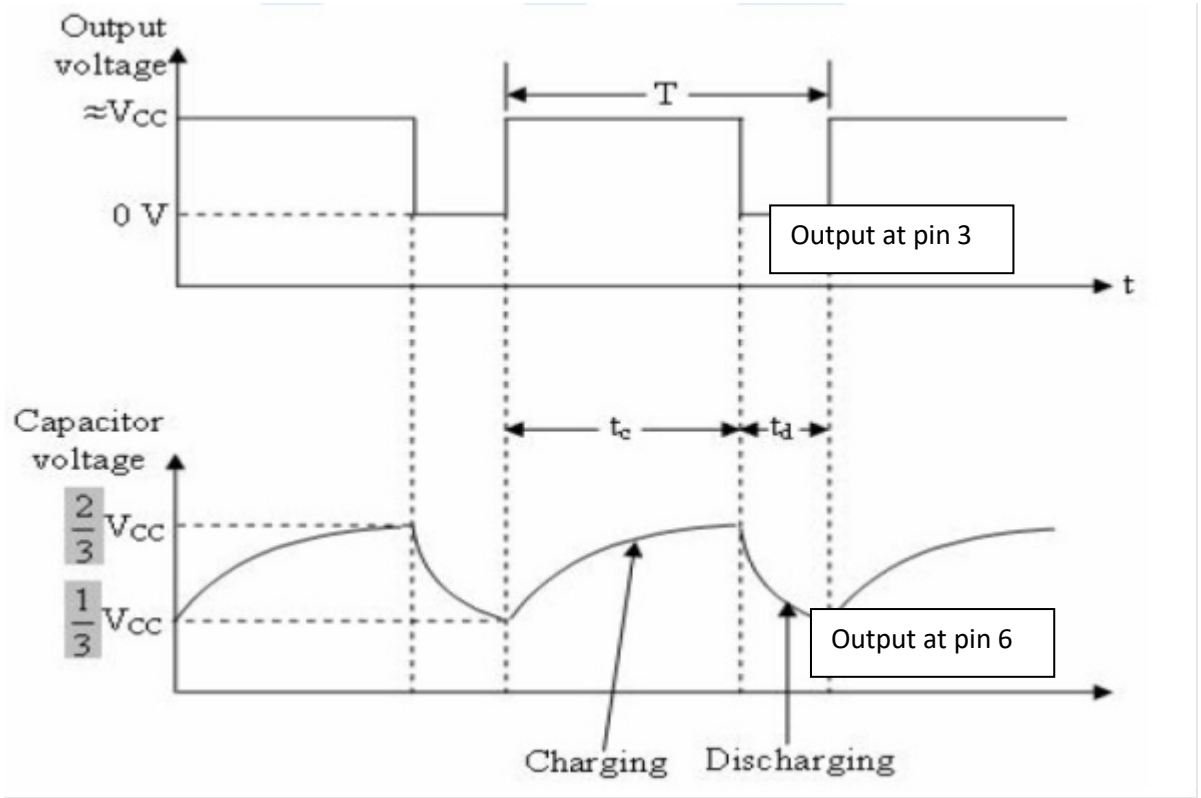
RESULT:

AIM 2: To design and set up a Astable multivibrator using 555 timer Ic.

CIRCUIT DIAGRAM:



MODEL GRAPH:



DESIGN:

Design Astable Multivibrator for T=1ms

$$T_{ON} = 0.69(R_A + R_B)*C$$

$$T_{OFF} = 0.69\,R_B * C$$

$$T = T_{ON} + T_{OFF}$$

$$T = 0.69(R_A + 2R_B)*C$$

$$f = 1/T = \frac{1.45}{(R_A + 2R_B)C}$$

$$\%\ \text{Duty cycle } D = \frac{T_{OFF}}{T} * 100$$

$$D = \frac{R_B}{(R_A + 2R_B)} \times 100$$

Let T_{ON} =0.7 m sec and T_{OFF} =0.3ms

Choose C = 0.1μf

We get R_A =6.8KΩ and R_B =4.7 KΩ

PROCEDURE:

1. Assemble the circuit as illustrated in figure.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Observe the corresponding output of the op amp for different digital inputs.

CALCULATION:

RESULT:

EXPERIMENT-II-2

DC power supply using IC 723: Low voltage and high voltage configurations, short circuit and Fold-back protection

723 GENERAL PURPOSE VOLTAGE REGULATORS:

The IC 723 is a general purpose, extremely versatile voltage regulator IC, which can be used for making various types of regulated power supplies such as:

- Positive Voltage Regulator
- Negative Voltage Regulator
- Switching Regulator
- Foldback Current Limiter

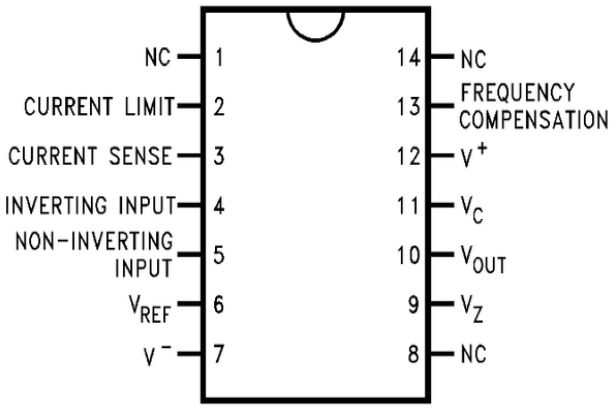
Main Features

- The minimum voltage that can be achieved from IC 723 Regulator Circuit is 2 V, and the maximum is around 37 V.
- The peak voltage that can handled by the IC is 50 V in pulsed form, and 40 V is the maximum continuous voltage limit.
- The maximum output current from this IC is 150 mA which can be upgraded to as high as10 amps through an external series pass transistor integration.
- The maximum tolerable dissipation of this IC 500 mW, therefore it should be mounted on a suitable heatsink in order to allow optimal performance from the device.
- Being a linear regulator, the IC 723 needs an input supply that should be at least 3 V higher than the desired output voltage, and the maximum difference between the input and the output voltage should never be allowed to exceed 37 V.

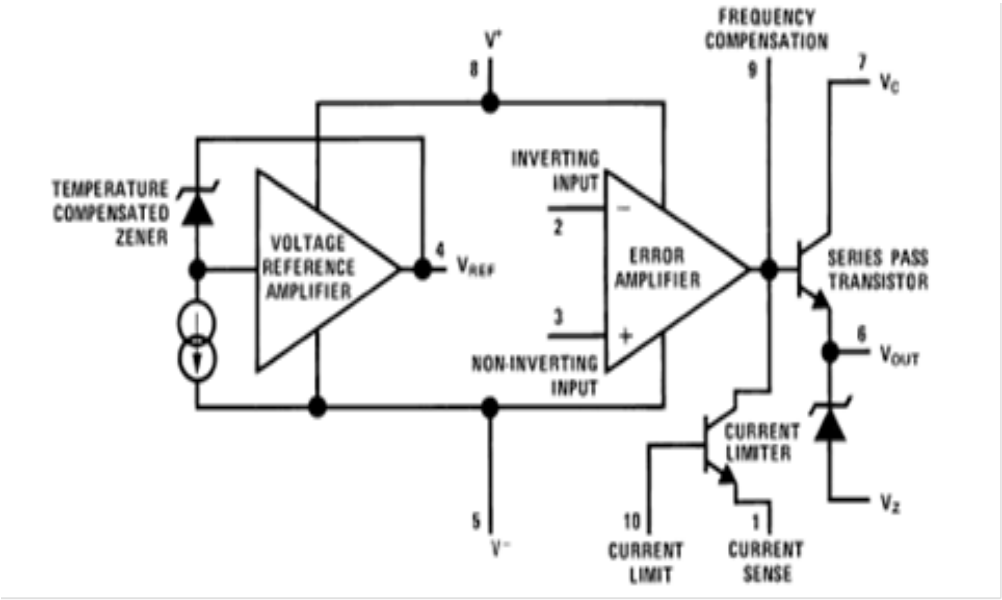
Absolute Maximum Ratings

- Pulse Voltage from V+ to V- (50 ms) = 50V
- Continuous Voltage from V+ to V- = 40V
- Input-Output Voltage Differential = 40V
- Maximum Amplifier Input Voltage (Either Input) = 8.5V
- Maximum Amplifier Input Voltage (Differential) = 5V
- Current from Vz 25 mA Current from VREF = 15 mA
- Internal Power Dissipation Metal Can = 800 mW
- CDIP = 900 mW
- PDIP = 660 mW
- Operating Temperature Range LM723 = -55°C to +150°C
- Storage Temperature Range Metal Can = -65°C to +150°C P DI P -55°C to +150°C
- Lead Temperature (Soldering, 4 sec. max.) Hermetic Package = 300°C Plastic
- Package 260°C ESD Tolerance = 1200V (Human body model, 1.5 k0 in series with 100 pF)

PINOUT DIAGRAM:



EQUIVALENT CIRCUIT:



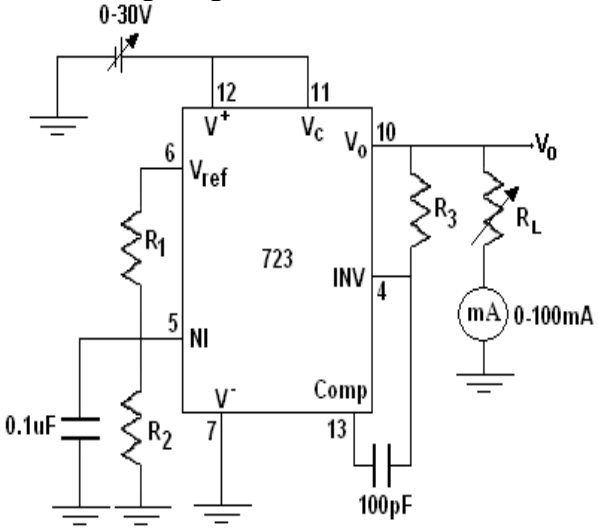
INFORMATION FROM DATASHEET:

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

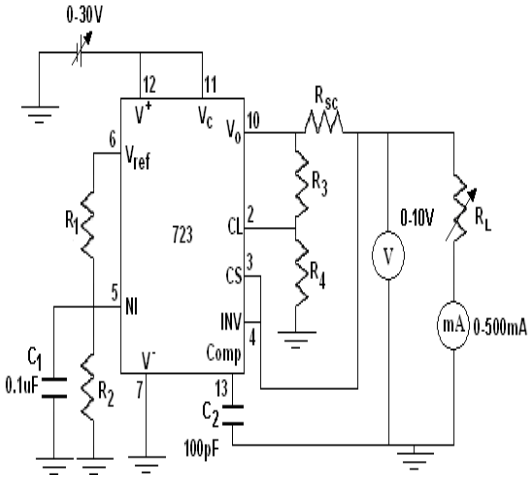
AIM 1: To design and set up low voltage regulator and fold back voltage regulator using 723 voltage regulator IC. Output voltage = 6 V.

CIRCUIT DIAGRAM:

Low Voltage Regulator

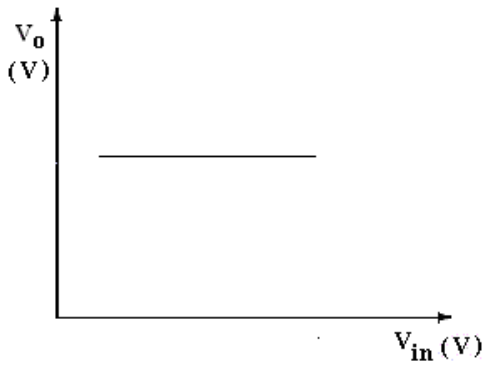


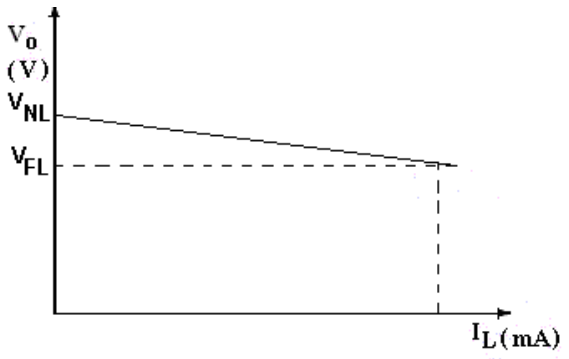
LVR with Current Fold Back



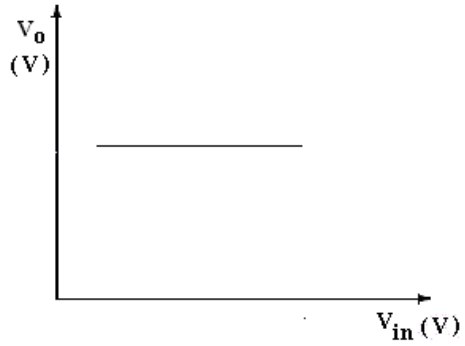
MODEL GRAPH:

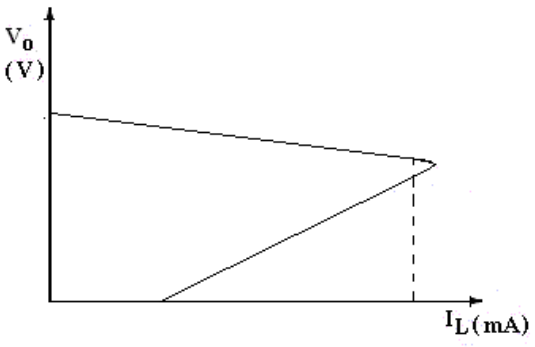
Low Voltage Regulator





LVR with Fold Back





DESIGN:

Vref = 7.15v

$$\text{Vout} = \text{Vref}\frac{R_2}{R_2 + R_1}$$

$$R_3 = R_1 \| R_2$$

Assume I_{limit} =0.5A

$$I_{limit} = \frac{V_{sense}}{R_{sc}}$$

PROCEDURE:

1. Check the IC and set up the circuit on the bread board as shown.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.
4. Apply V_{in} from an unregulated power supply.
5. Connect a milli-ammeter and a rheostat in series with the output and connect a voltmeter in parallel.
6. To obtain the load regulation, vary the input and note down the corresponding variation in the output voltage.
7. To obtain the line regulation, vary the rheostat from no load to full load and observe the corresponding current and voltage.
8. The line and load regulation characteristics can be plotted from the readings.
9. The same procedure can be repeated for fold back regulator.
10. For fold back regulators load regulation, after a particular point the voltage and current decreases suddenly from a point. Note this point correctly.
11. Calculate the % load regulation using the expression:

$\frac{VNL-VFL}{VNL}$ x 100.

OBSERVATION:

Low voltage regulator

Line Regulation

V_{in}(V)	V_o(V)

Load Regulation

I_L(mA)	V_o(V)

Low voltage regulator using fold back

Line Regulation

V_{in}(V)	V_o(V)

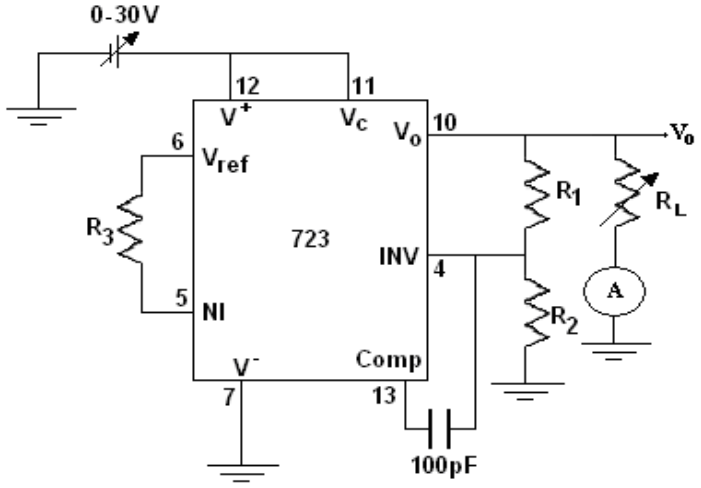
Load Regulation

I_L(mA)	V_o(V)

RESULT:

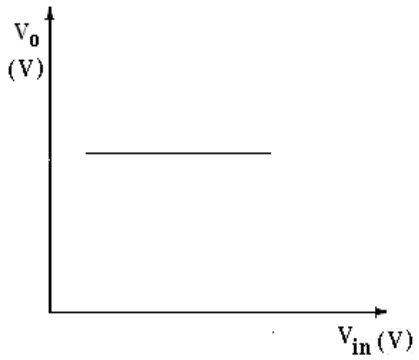
AIM 2: To design and set up high voltage regulator and fold back voltage regulator using 723 voltage regulator IC. Output voltage = 12 V.

CIRCUIT DIAGRAM:

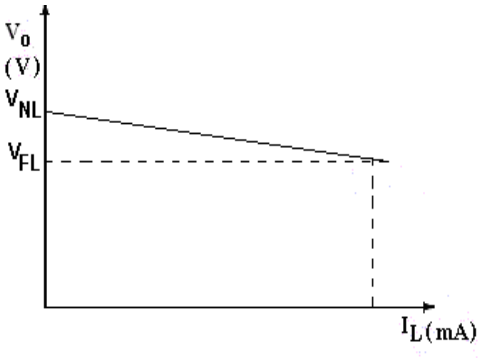


MODEL GRAPH:

Line Regulation



Load Regulation



DESIGN:

Vref = 7.15v

$$\text{Vout}=\text{Vref}\frac{R_2 + R_1}{R_2}$$

$$R_3 = R_1 R_2$$

PROCEDURE:

1. Check the IC and set up the circuit on the bread board as shown.
2. Manually trace the circuit to check the correctness of physical connection.
3. Calibrate the CRO.

4. Apply V_{in} from an unregulated power supply.
5. To obtain the load regulation, vary the input and note down the corresponding variation in the output voltage.
6. To obtain the line regulation, vary the rheostat from no load to full load and observe the corresponding current and voltage.
7. The line and load regulation characteristics can be plotted from the readings.

OBSERVATION:

Line Regulation

V_{in}(V)	V_o(V)

Load Regulation

I_L(mA)	V_o(V)

CALCULATION:

RESULT:

EXPERIMENT-II-3

D/A Converters - R-2R ladder circuit

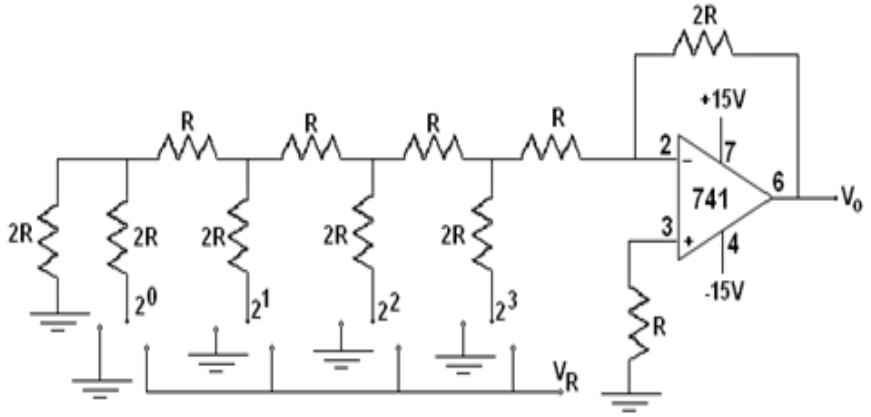
AIM: To design and set up an R- 2R ladder DAC circuit.

R-2R Resistive Ladder Network:

As its name implies, the "ladder" description comes from the ladder-like configuration of the resistors used within the network. A R-2R resistive ladder network provides a simple means of converting digital voltage signals into an equivalent analogue output. Input voltages are applied to the ladder network at various points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier.

Then a R-2R resistive ladder network is nothing more than long strings of parallel and series connected resistors acting as interconnected voltage dividers along its length, and whose output voltage depends only on the interaction of the input voltages with each other.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the trainer to the mains and switch on the power supply.

2. Measure the supply voltages of the circuit as +15V & -15V.

3. Calculate theoretically Vo for all digital Input data using formula.

   V=-Rf/R (1/2 D3+1/4D2+1/8D1+1/16D0)

4. In this experiment Rf = 22kΩ & R= 10kΩ.

5. Note down Output voltages for different combinations of digital inputs and compare it with theoretical values

OBSERVATION:

Digital Input				Output
2^3	2^2	2^1	2^0	

RESULT:

III. Simulation experiments using Multisim

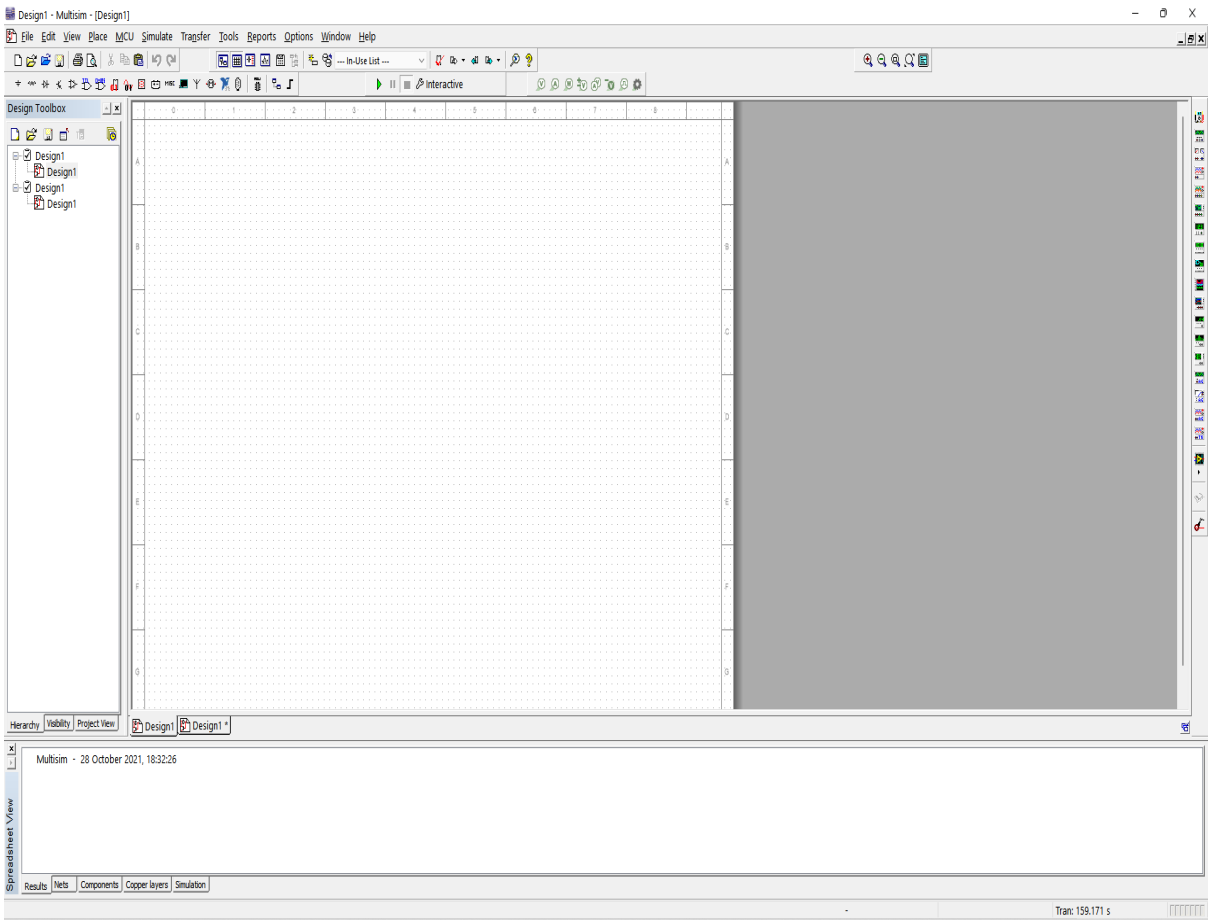
EXPERIMENT-III-1

Simulation of any three circuits from Experiments in section I

Multisim Simulation of Electronic Circuits:

Multisim is the schematic capture and simulation application of National Instruments Circuit Design Suite, a suite of EDA (Electronic Design Automation) tools. It is similar to PSpice, but it is easier to use in practical sense and has lots of features to make circuit drawing/simulating, a really simple task. Here is window of multisim, as it appears first time when you start the software

Multisim 14.2 Window:



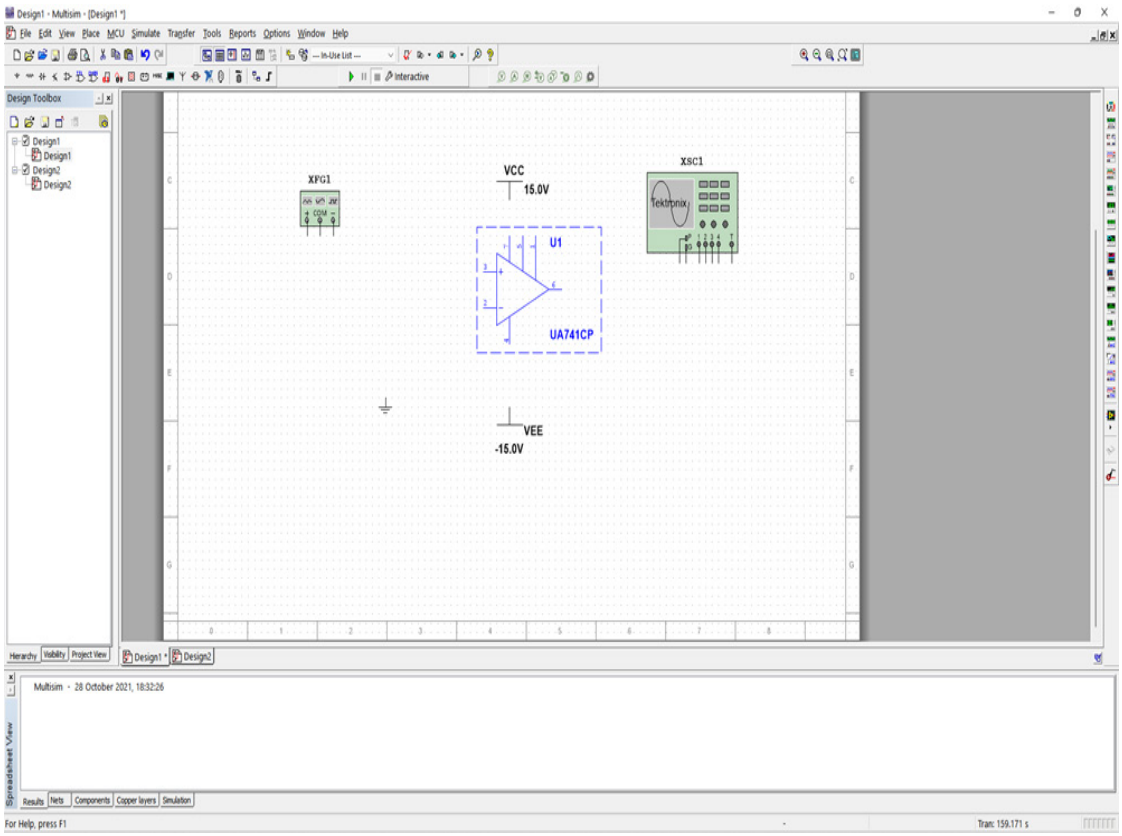
1. The **Menu Bar** is where you find commands for all functions.
2. The **Design Toolbox** lets you navigate through the different types of files in a project (schematics,PCBs, reports), view a schematic's hierarchy and show or hide different layers.
3. The **Component** toolbar contains buttons that let you select components from the Multisim databases for placement in your schematic.
4. The **Standard** toolbar contains buttons for commonly-performed functions such as Save, Print, Cut,and Paste.

5. The **View** toolbar contains buttons for modifying the way the screen is displayed.
6. The **Simulation** toolbar contains buttons for starting, stopping, and other simulation functions.
7. The **Main** toolbar contains buttons for common Multisim functions.
8. The **In Use List** contains a list of all components used in the design.
9. The **Instruments** toolbar contains buttons for each instrument.
10. **Scroll Left –right** is to ensure ease in handling larger designs.
11. The **Circuit Window** (or workspace) is where you build your circuit.
12. **Active tab** indicates the current active circuit window.

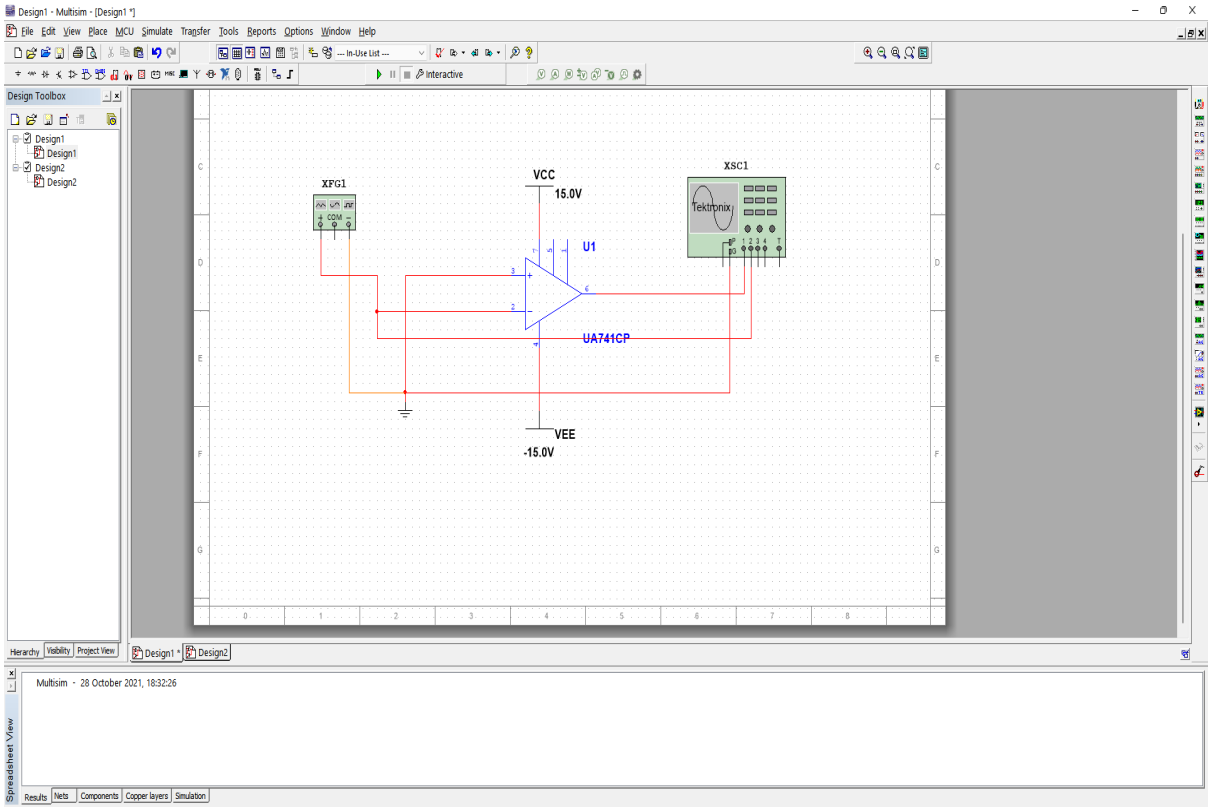
Let's take an example of a Zero crossing Detector circuit. We will simulate the circuit to obtain the output.

Please follow the steps:

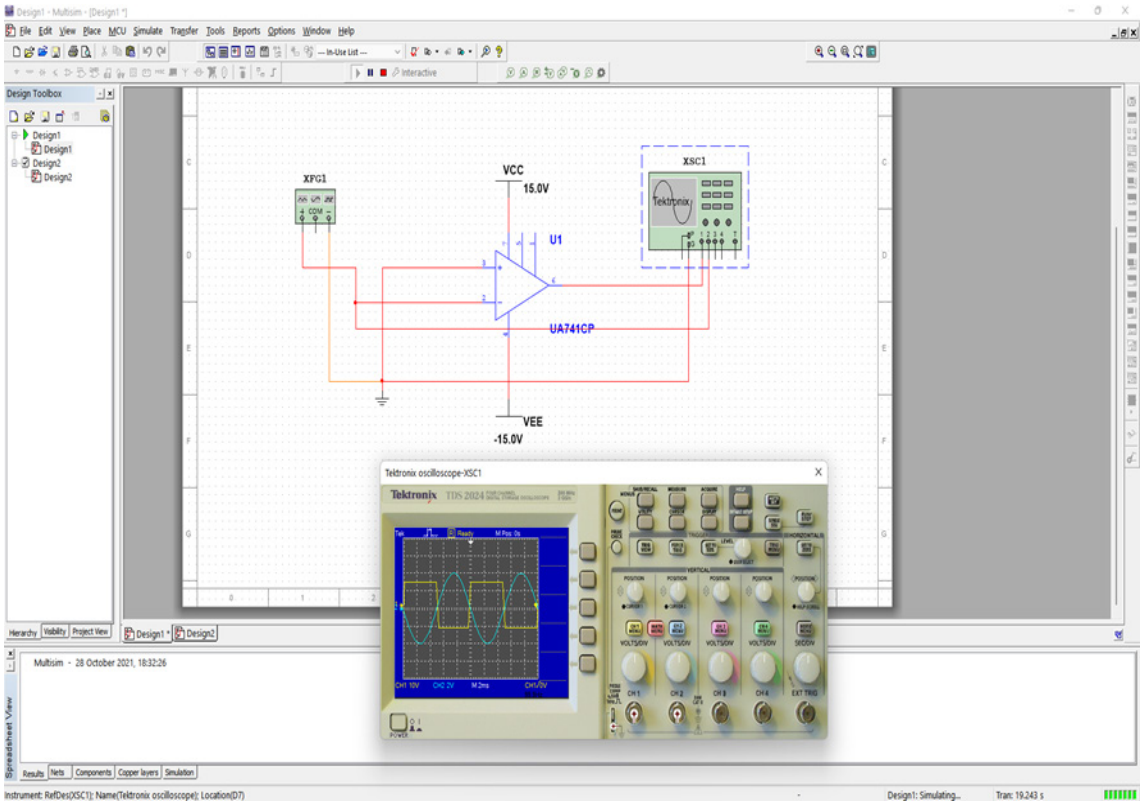
1. Click the design to continue with the implementation
2. Now select the components from the Menu as shown



3. In the above figure we are using UA741CP Op-Amp, Function generator, Oscilloscope UA741CP, VCC, VEE and ground.
4. Now perform the connections as shown.



5. Now press the green arrow to simulate in interactive environment. The green arow now becomes a red square block, indicating the beginning of simulation. Now click the Tektronics oscilloscope block. A virtual oscilloscope will appear as shown in figure.

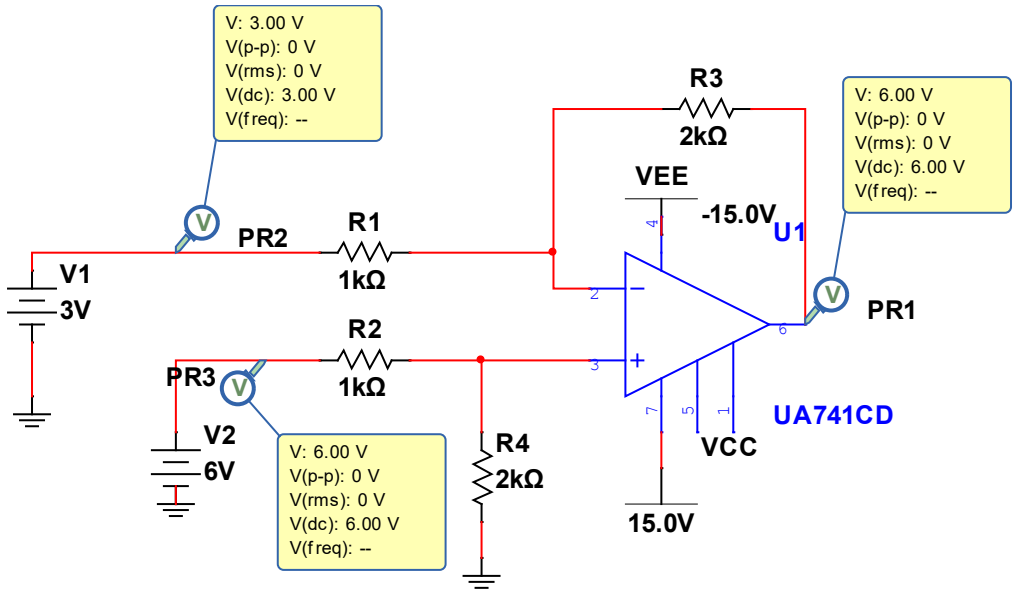


6. By adjusting the knobs in the oscilloscope, we can vary the visual aspect of the output.

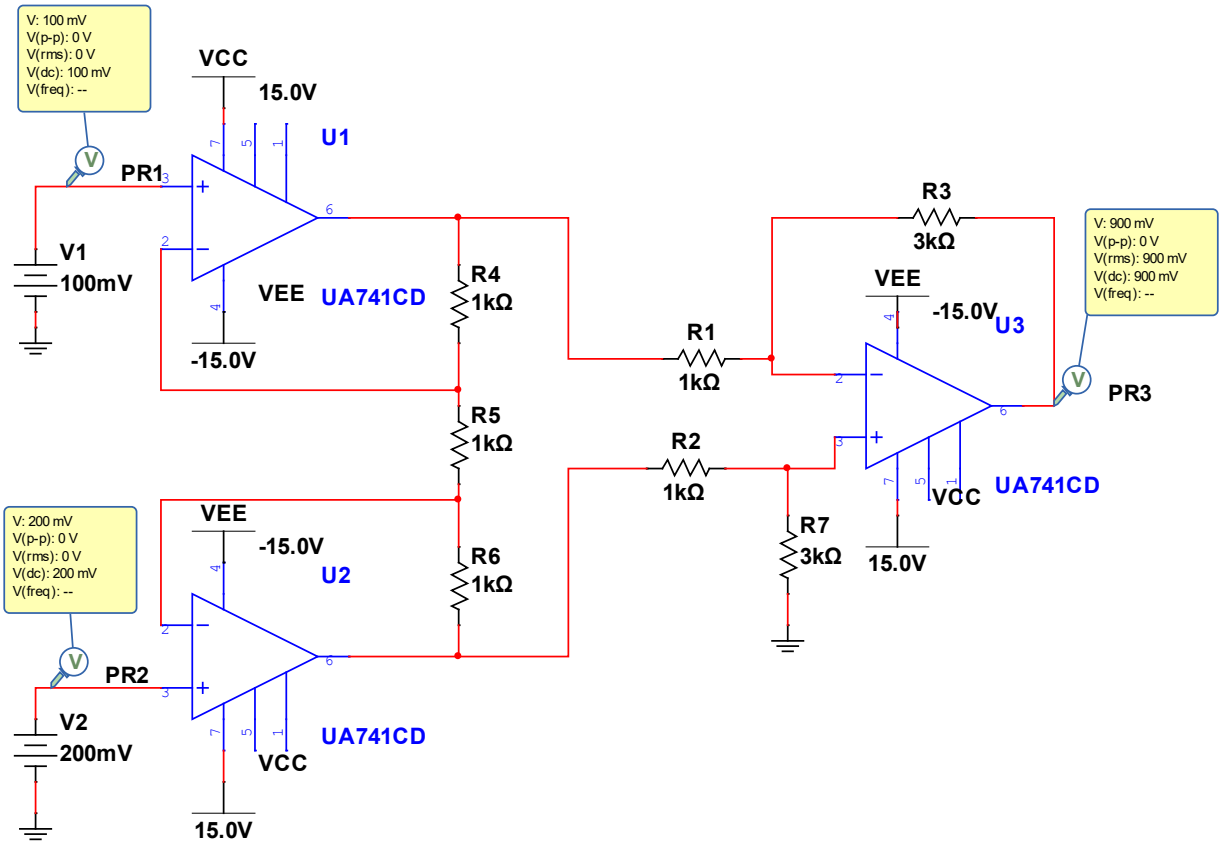
AIM 1. Simulation of three circuits from section I

Note: Students are expected to simulate these experiments using Multisim 14.2 a shown.

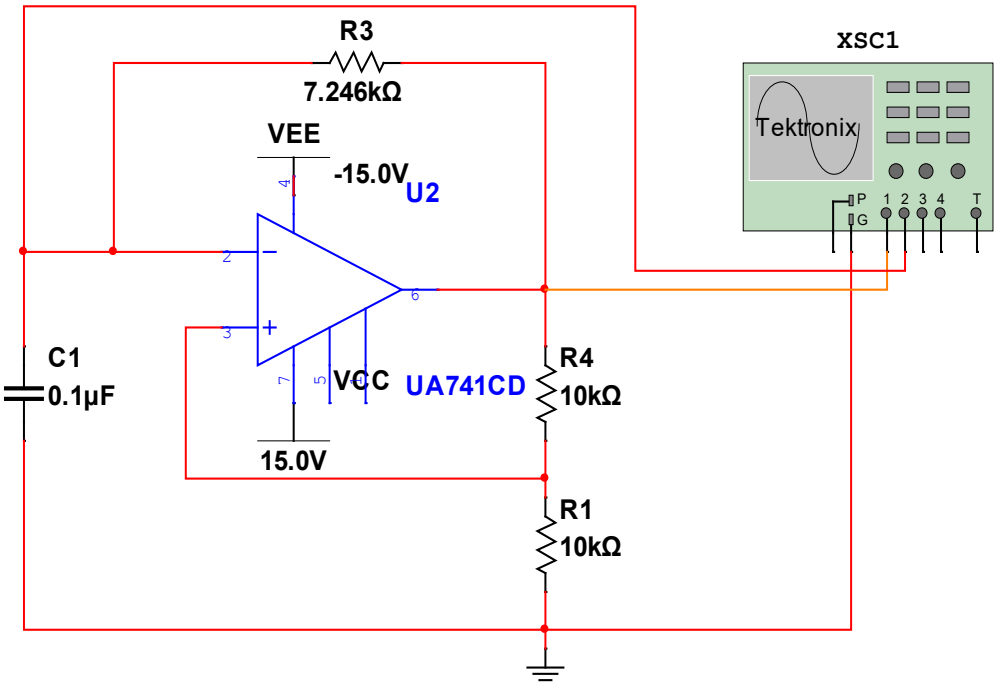
a) Difference Amp using µA741



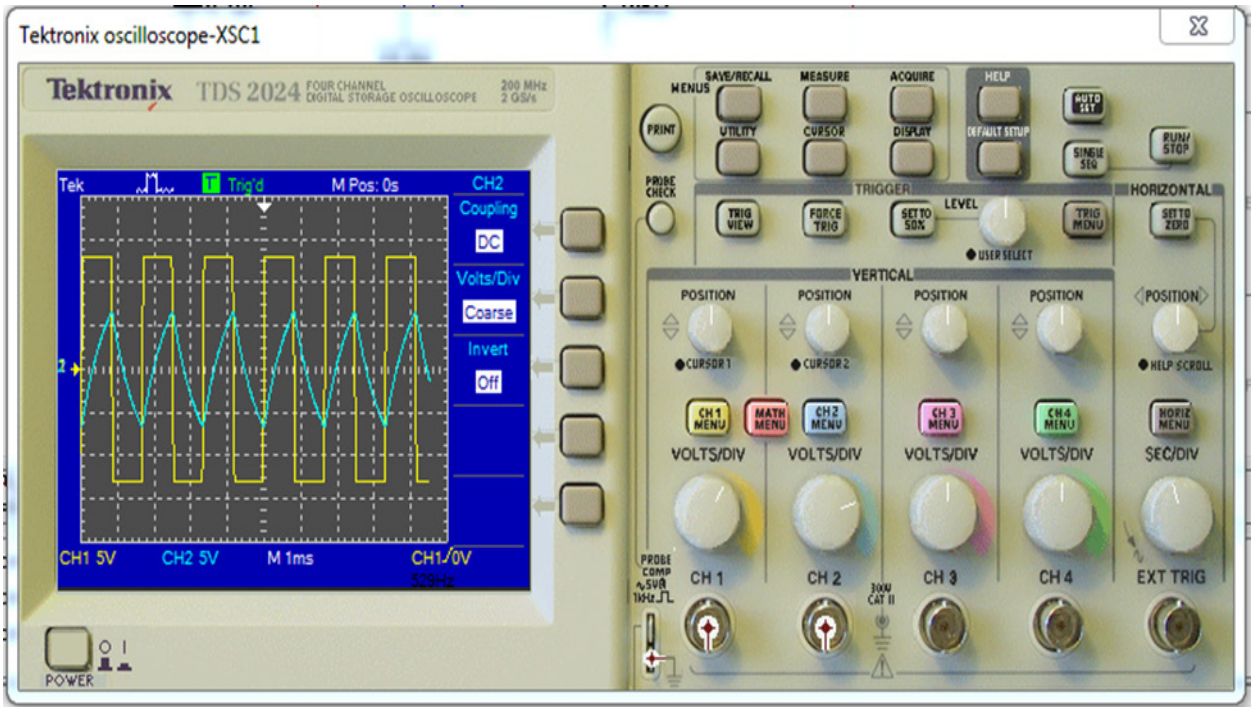
b) Instrumentation amp using µA741



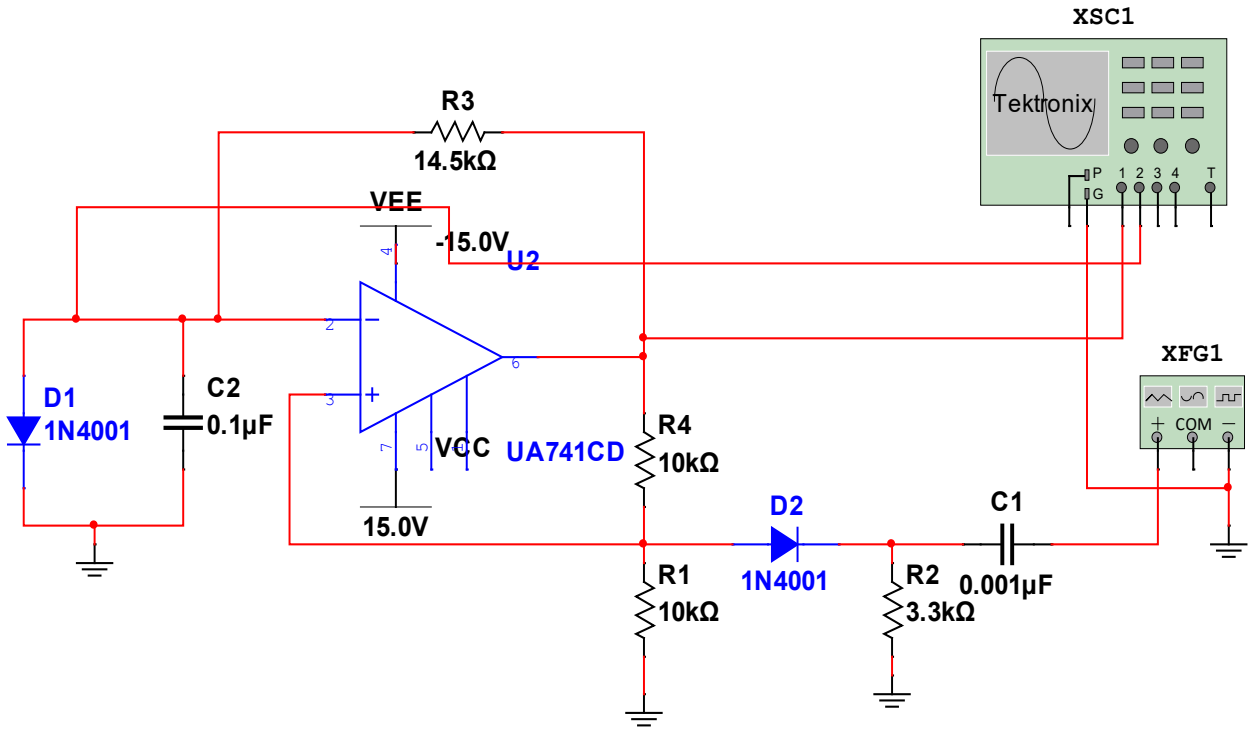
c) Astable using Op-Amp µA741



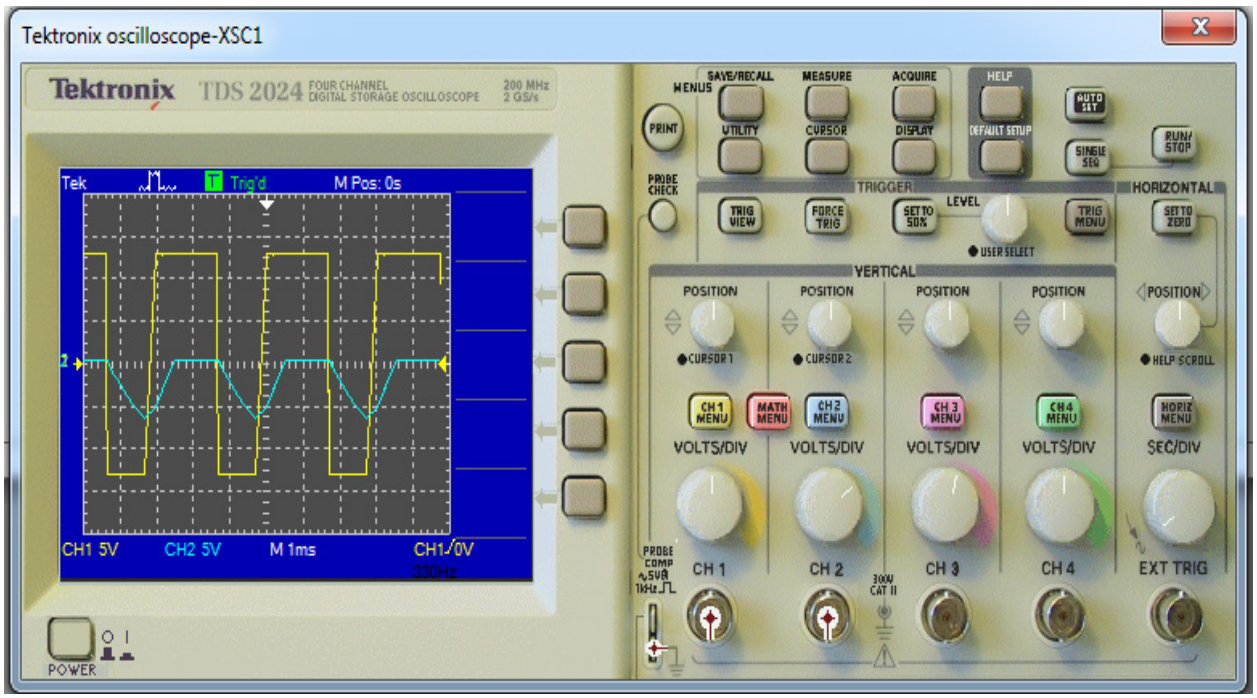
Output Waveform:



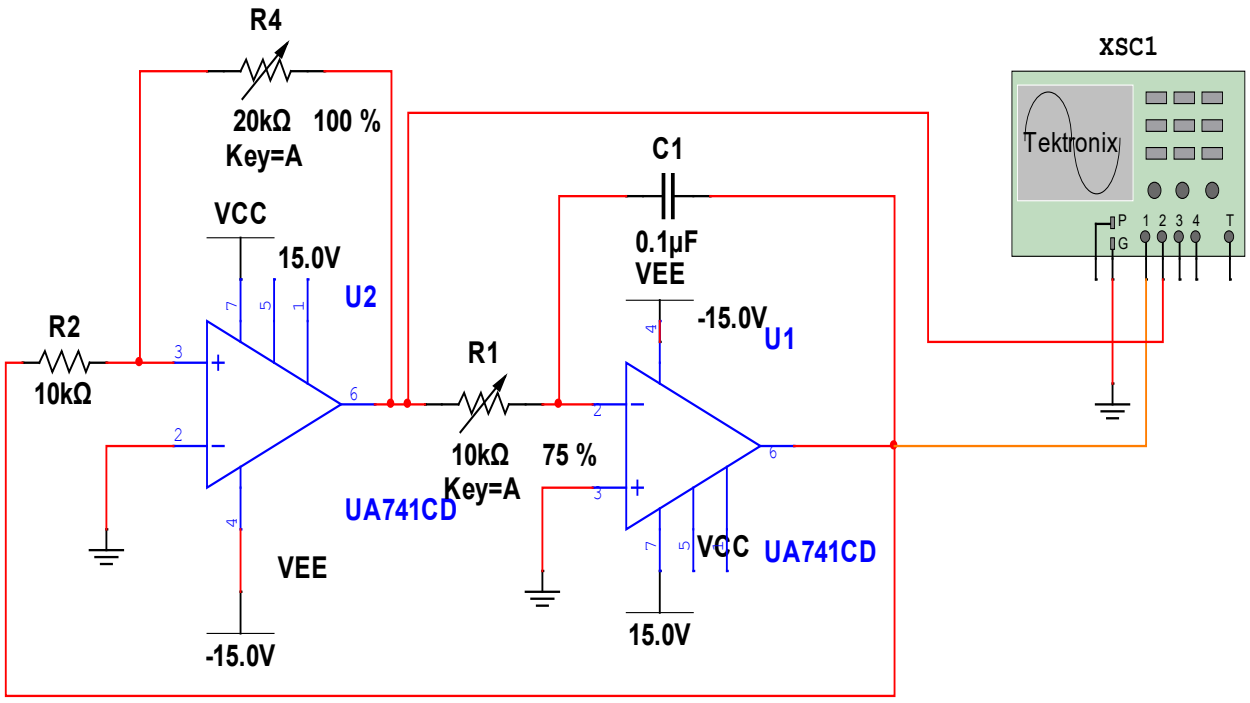
d) Monostable multivibrator using Op-Amp µA741



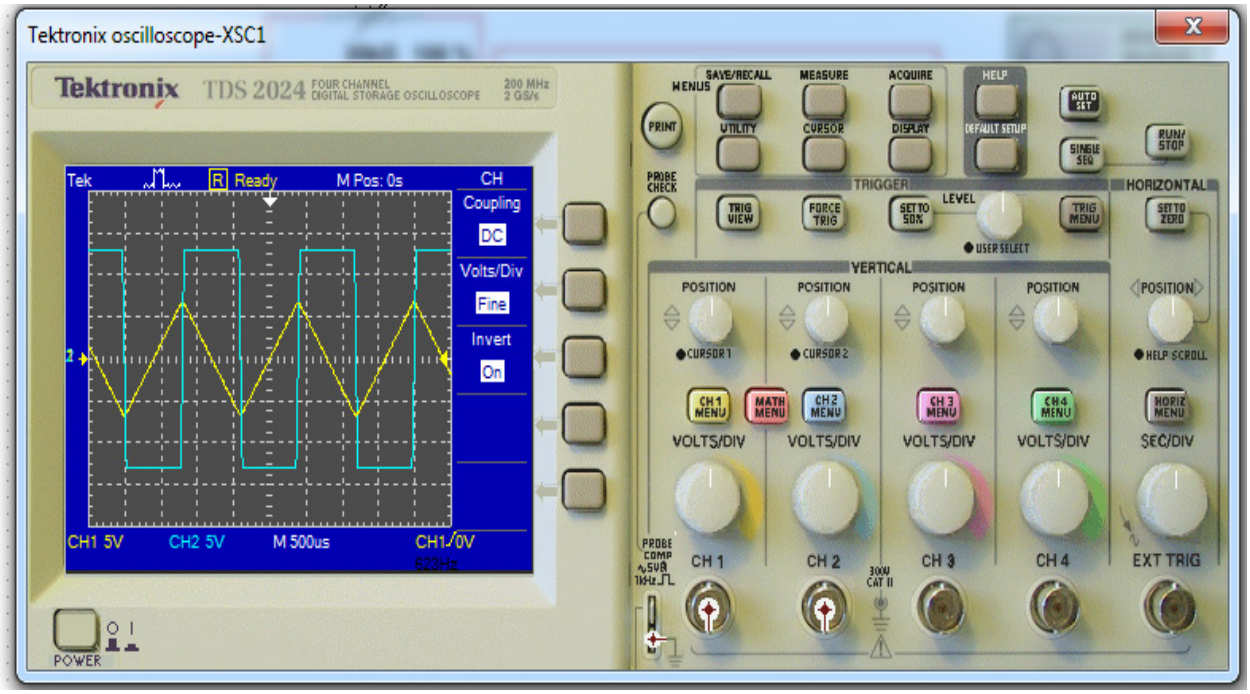
Output Waveform:



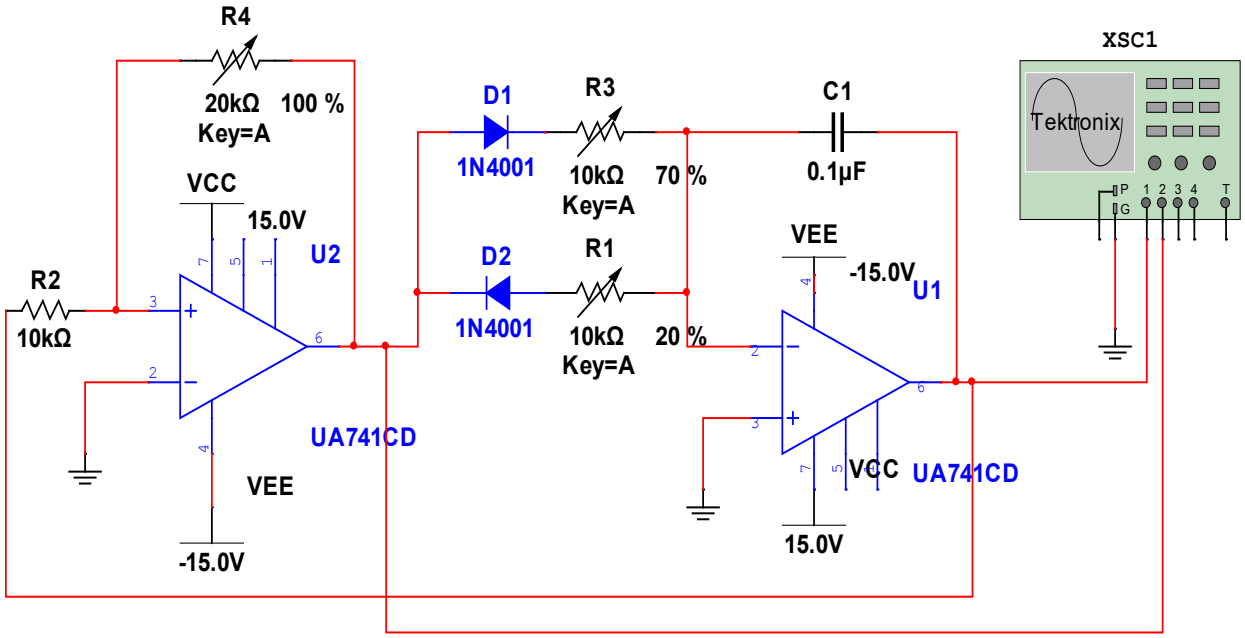
e) Waveform generators using Op-Amps - Triangular



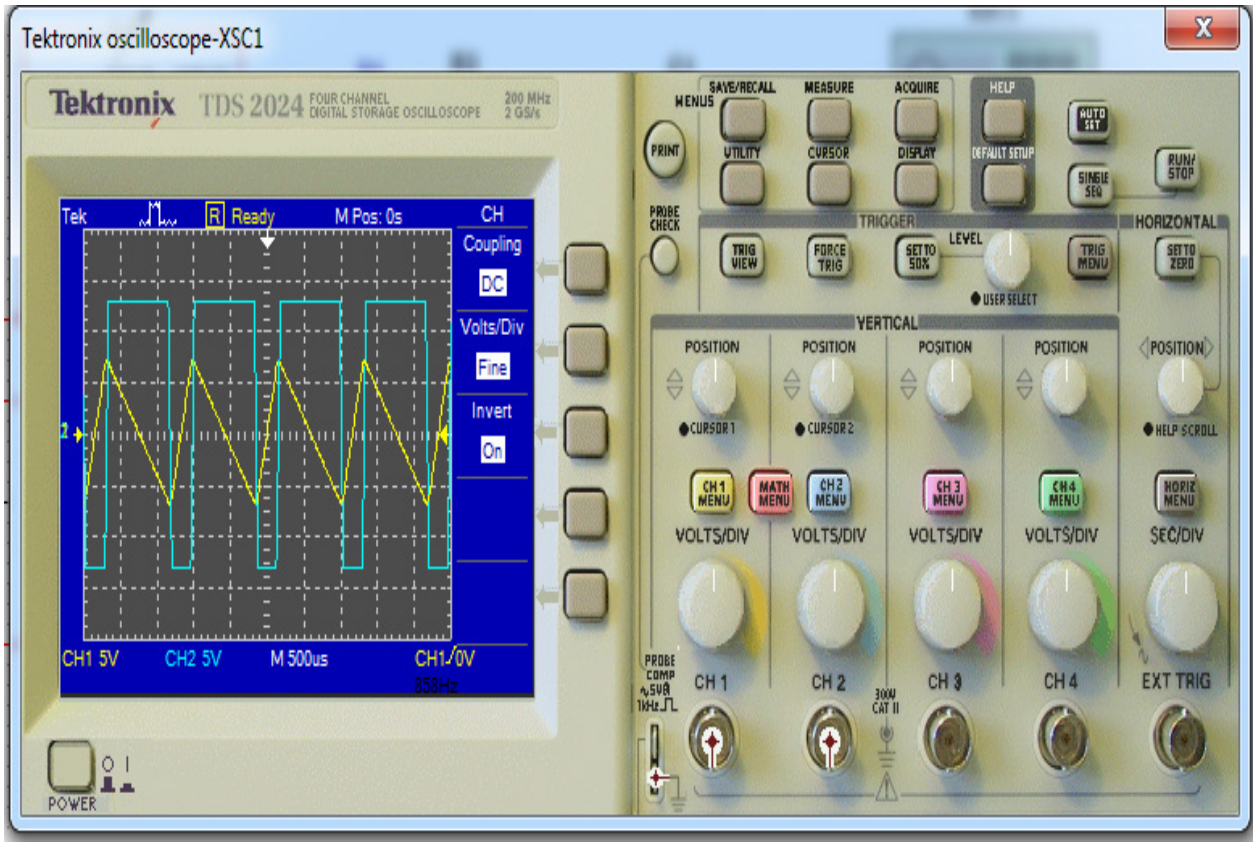
Output Waveform:



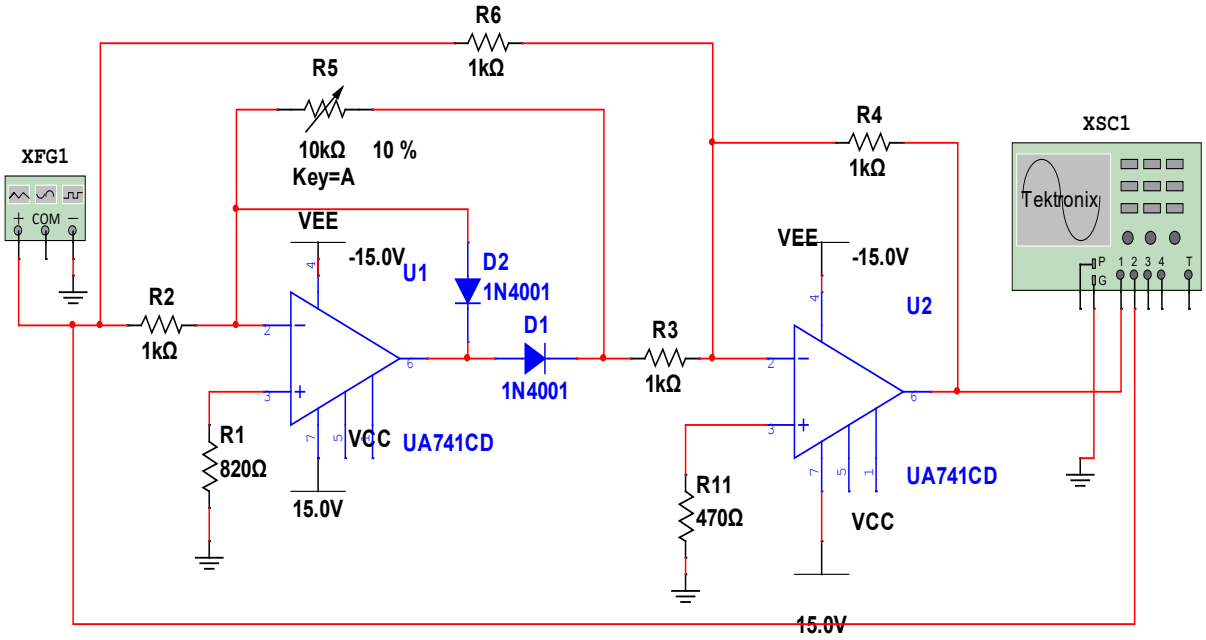
f) Waveform generators using Op-Amps - saw tooth



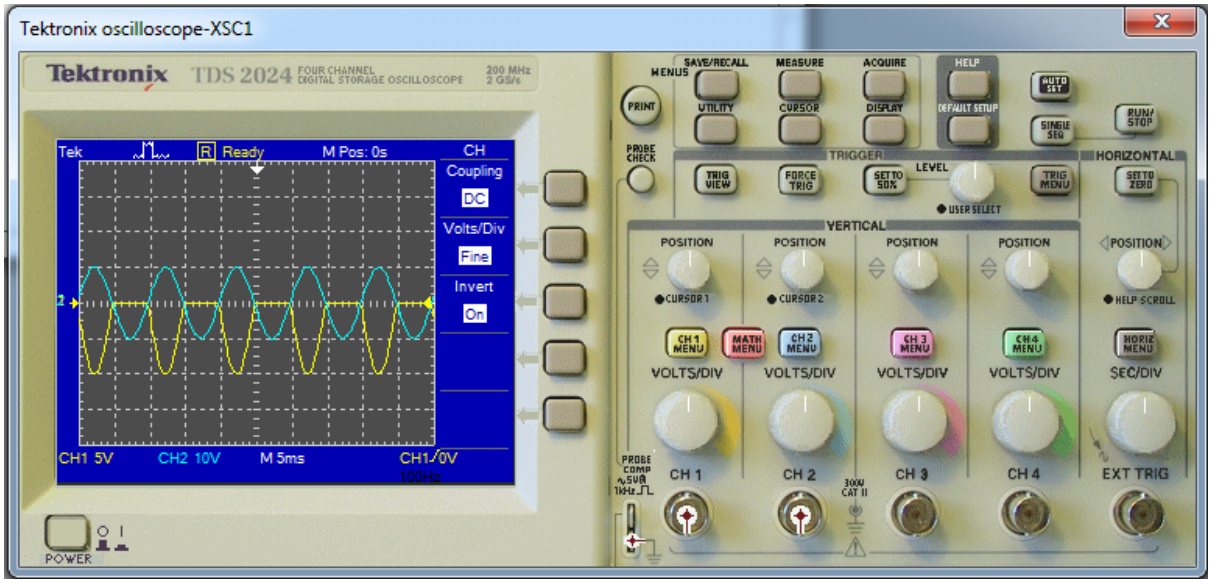
Output Waveform:



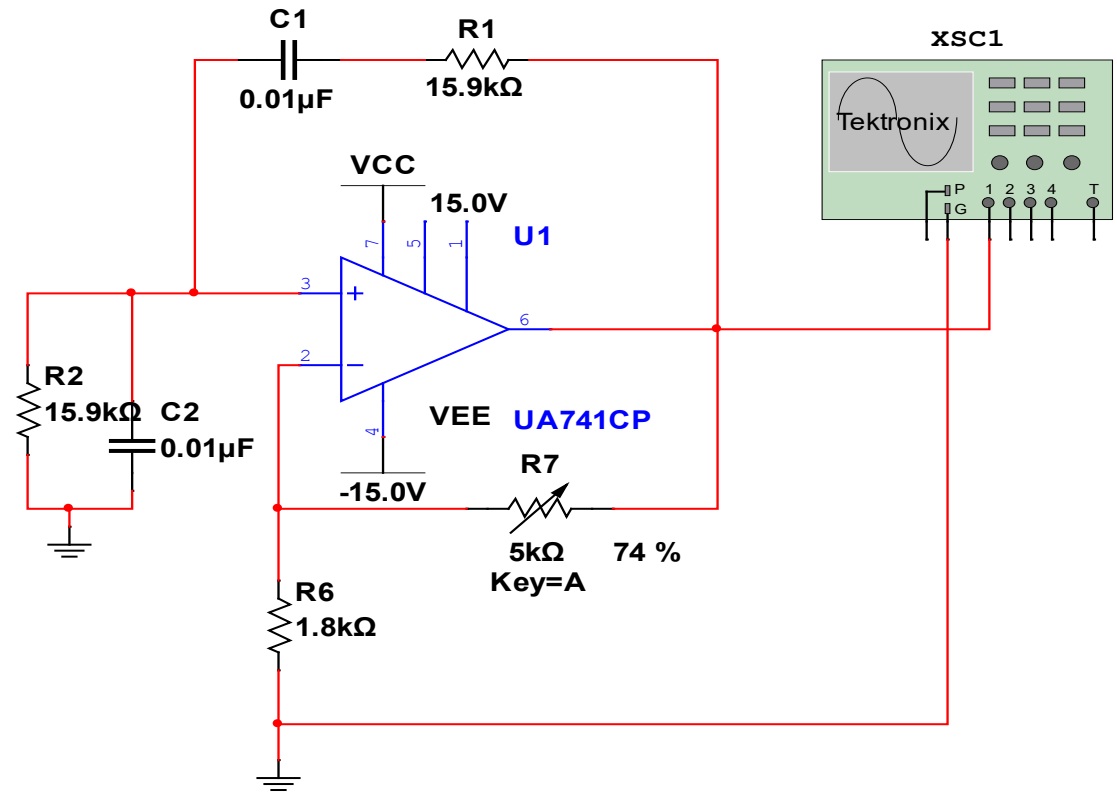
g) Precision rectifier

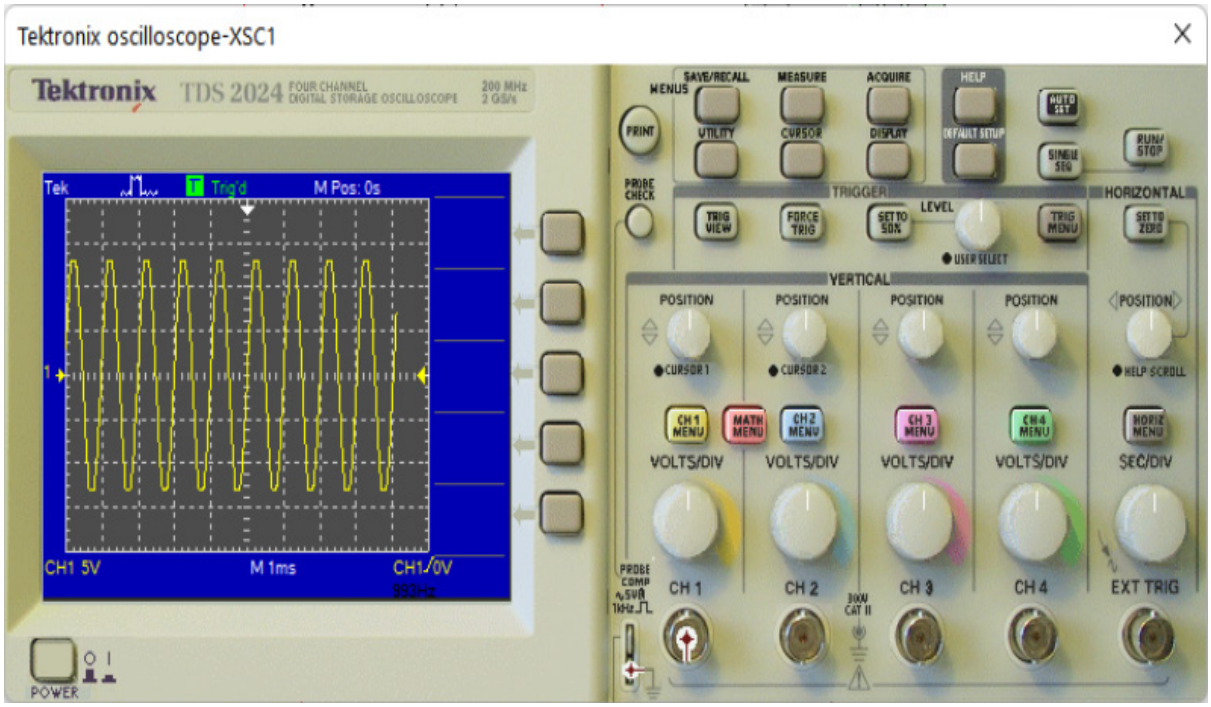


Output Waveform:

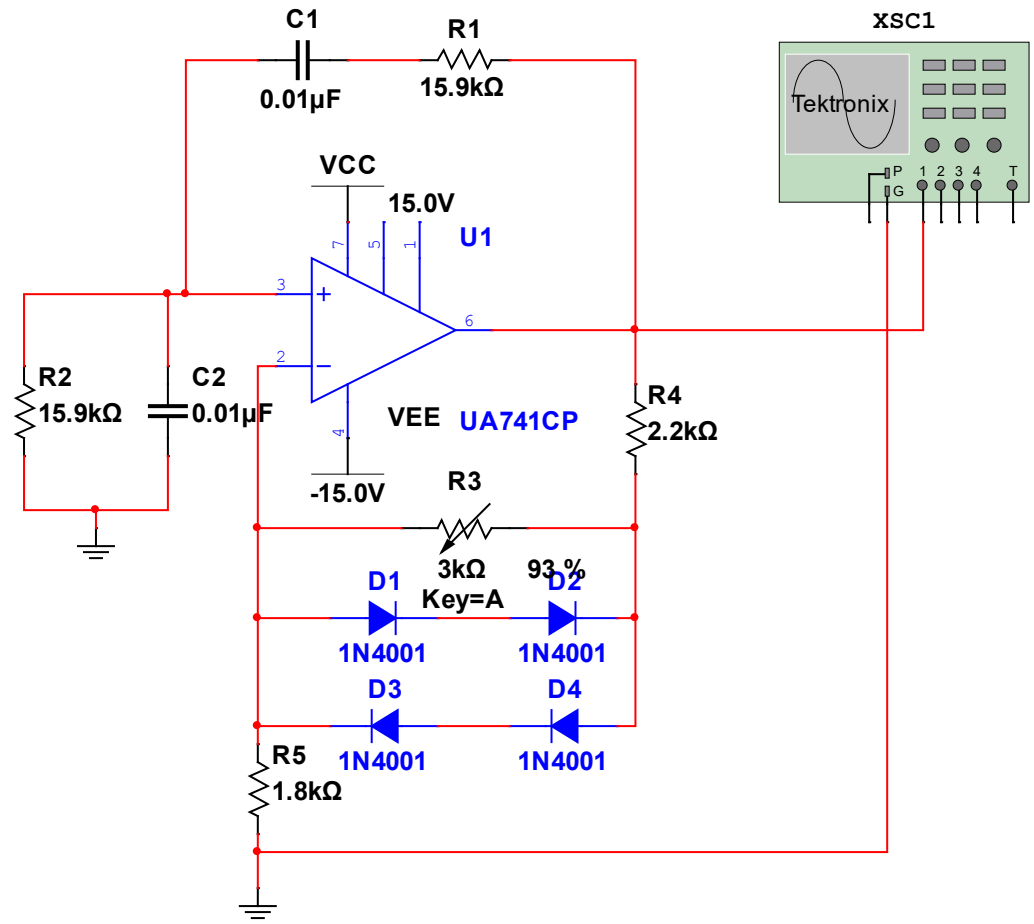


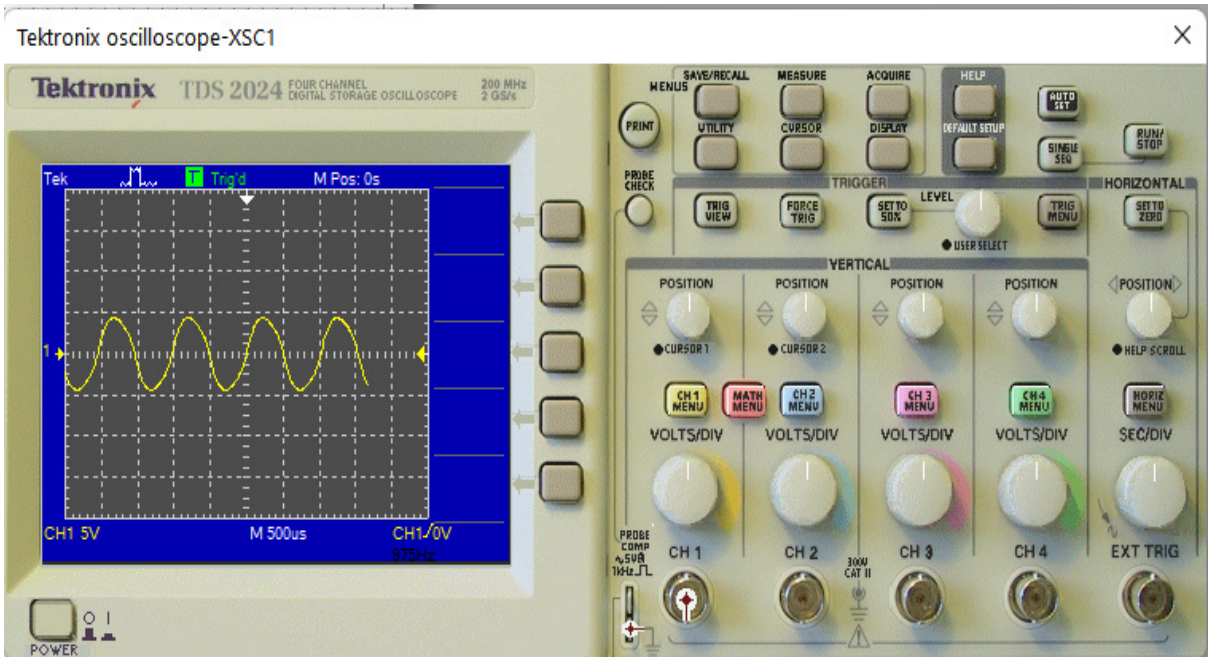
h) Wein Bridge Oscillator





i) Wein Bridge Oscillator with Amplitude stabilization

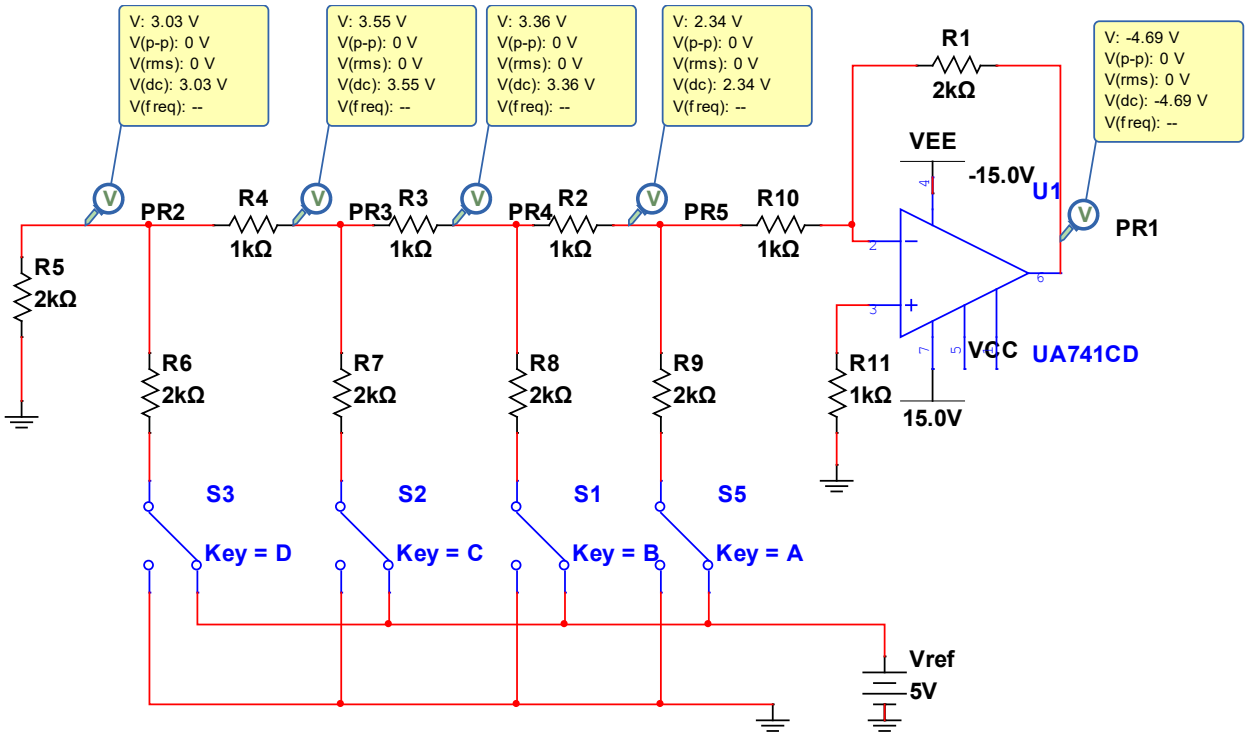




AIM 2. Simulation of Experiments 3 Or 4 from section II

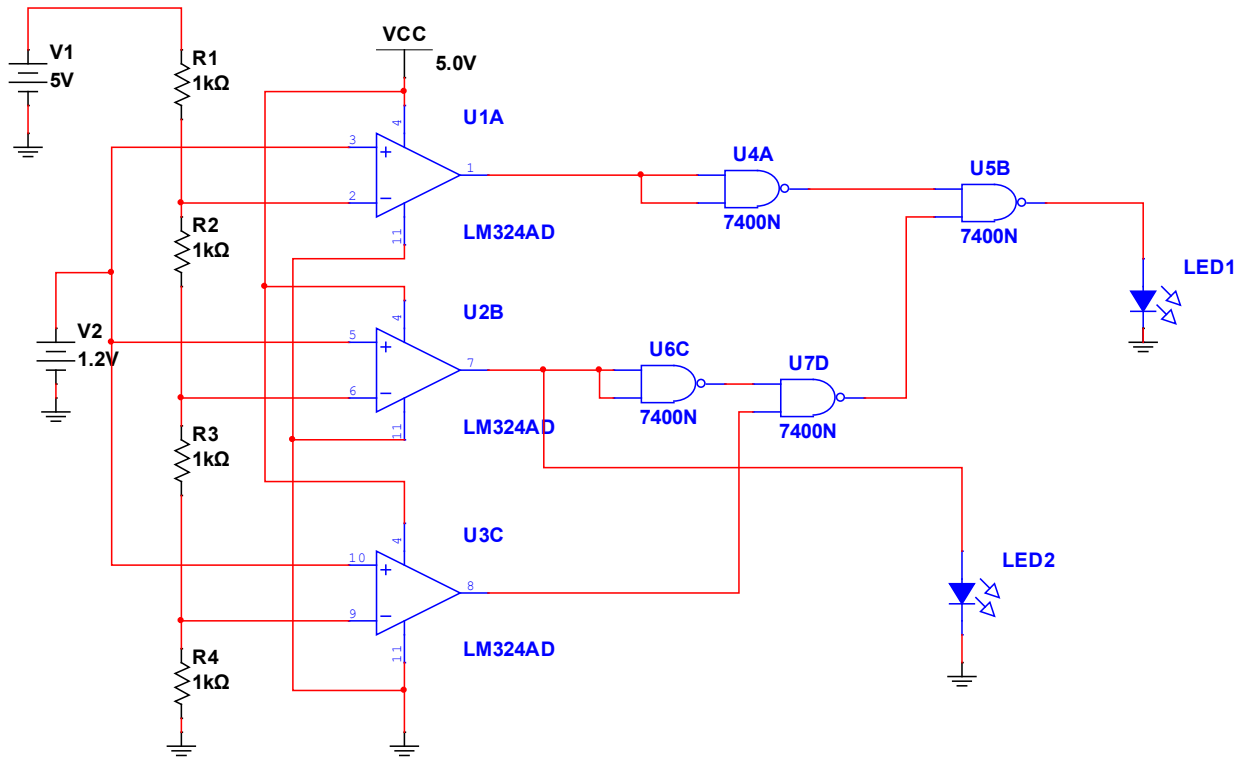
Note: Students are expected to simulate these experiments using Multisim 14.2 a shown.

a) D/A Converters - R-2R ladder circuit

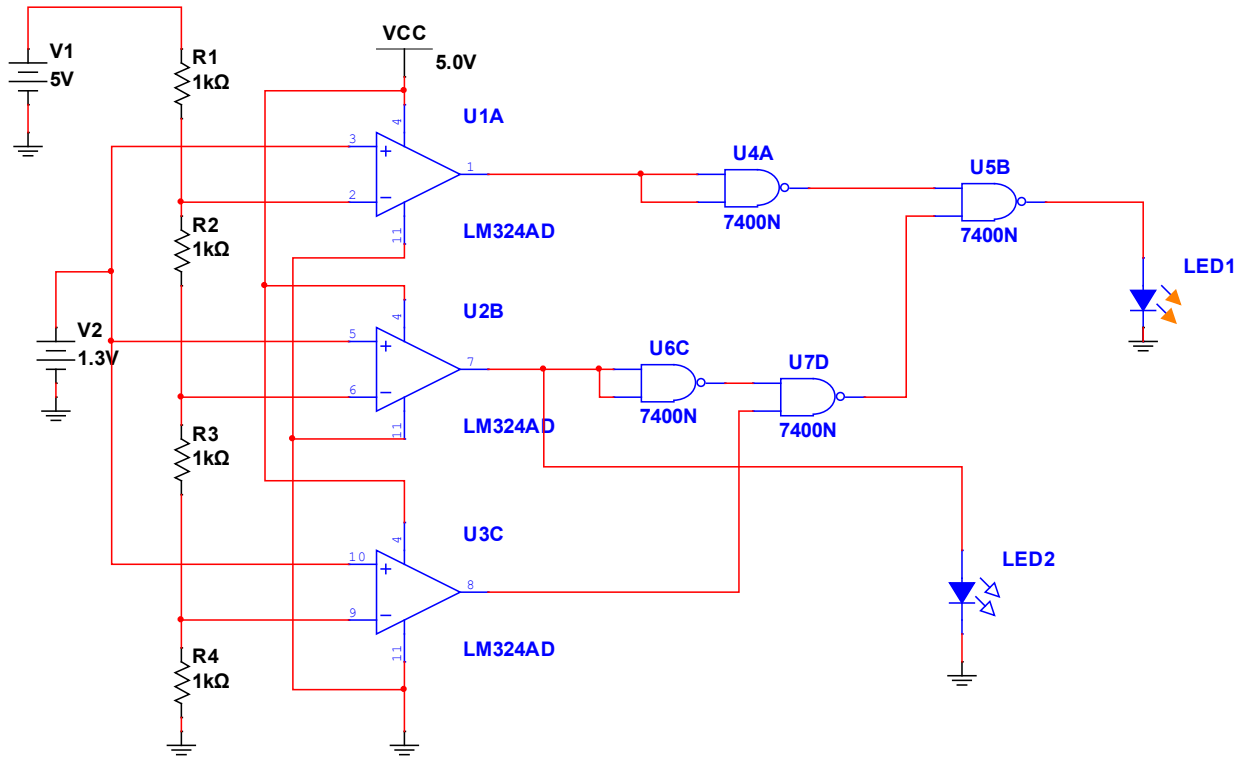


c) Flash ADC

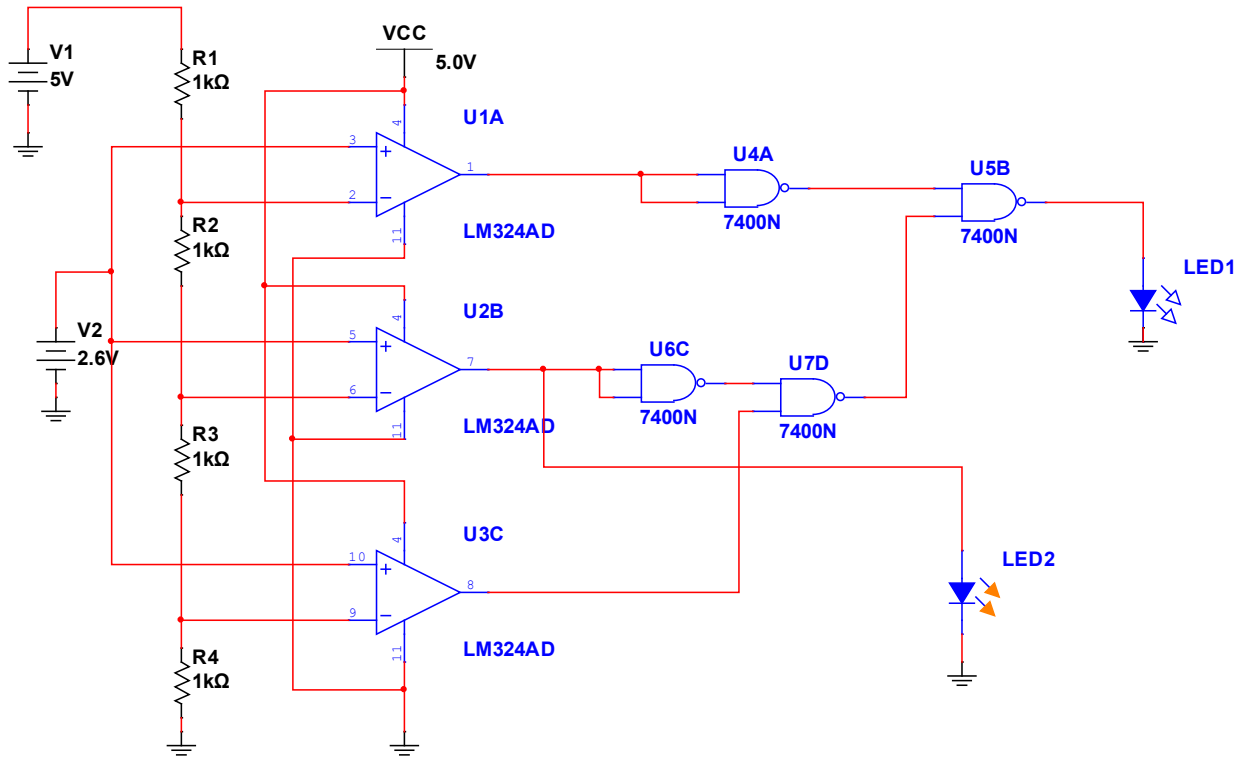
Case I: When input voltage V2 is less than 1.25V



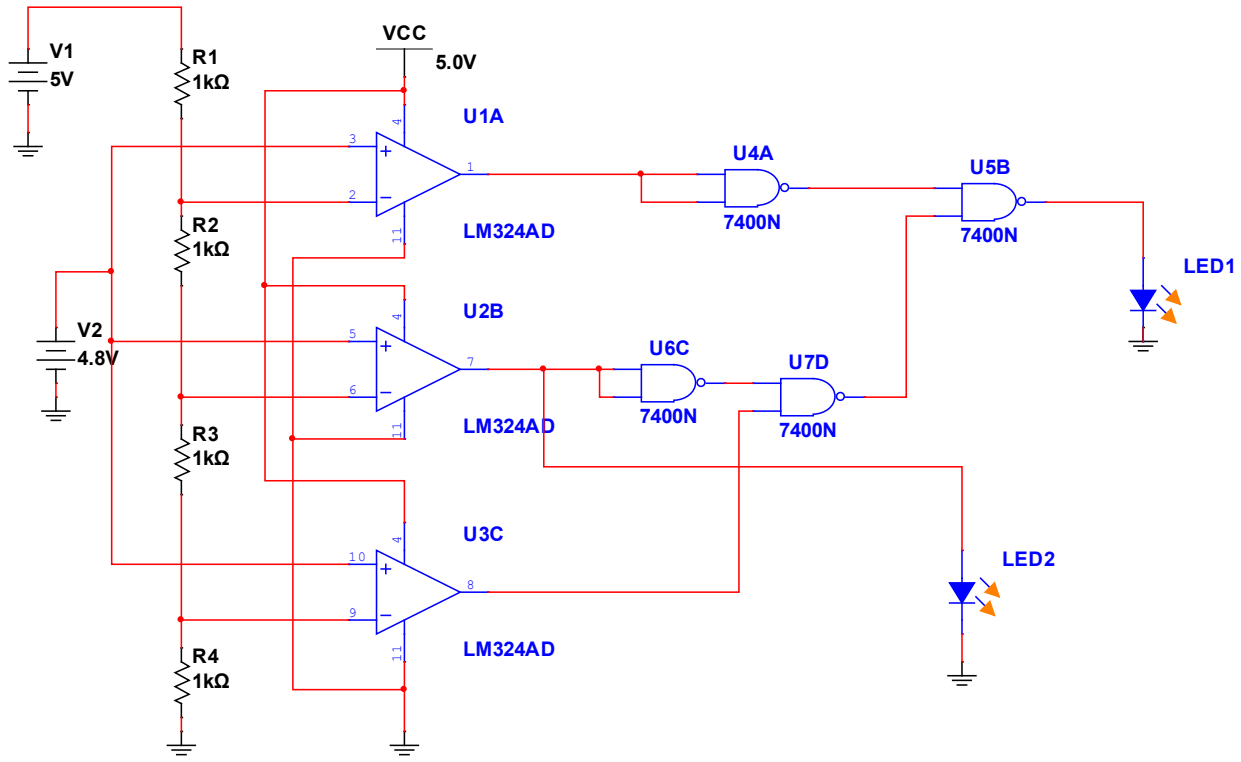
Case II: When input voltage V2 is greater than 1.25V and less than 2.5V



Case III: When input voltage V2 is greater than 2.5V and less than 3.5V



Case IV: When input voltage V2 is greater than 3.5V and less than 5V



RESULT: