VLSI Project

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2025122004.

Q1 So, we are implementing a 5-bit CLA as per the proposed structure.

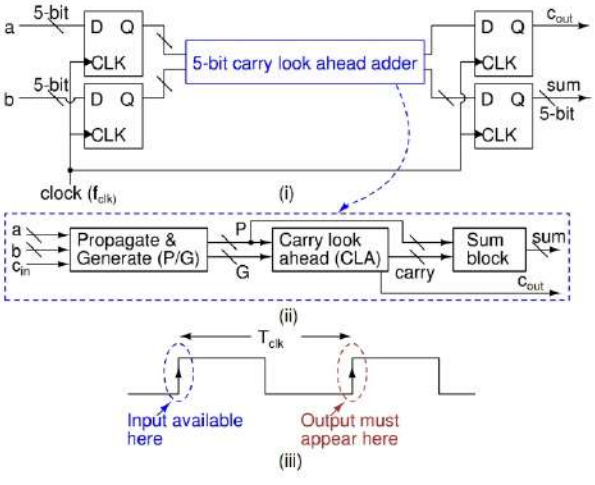


Figure 1

⇒ So, we are going to take $C_0 = 0$

⇒ The general logic $C_{i+1} = g_i + P_i C_i$

$C_1 = g_0$

$C_2 = g_1 + P_1 g_0$

$C_3 = g_2 + P_2 g_1 + P_2 P_1 g_0$

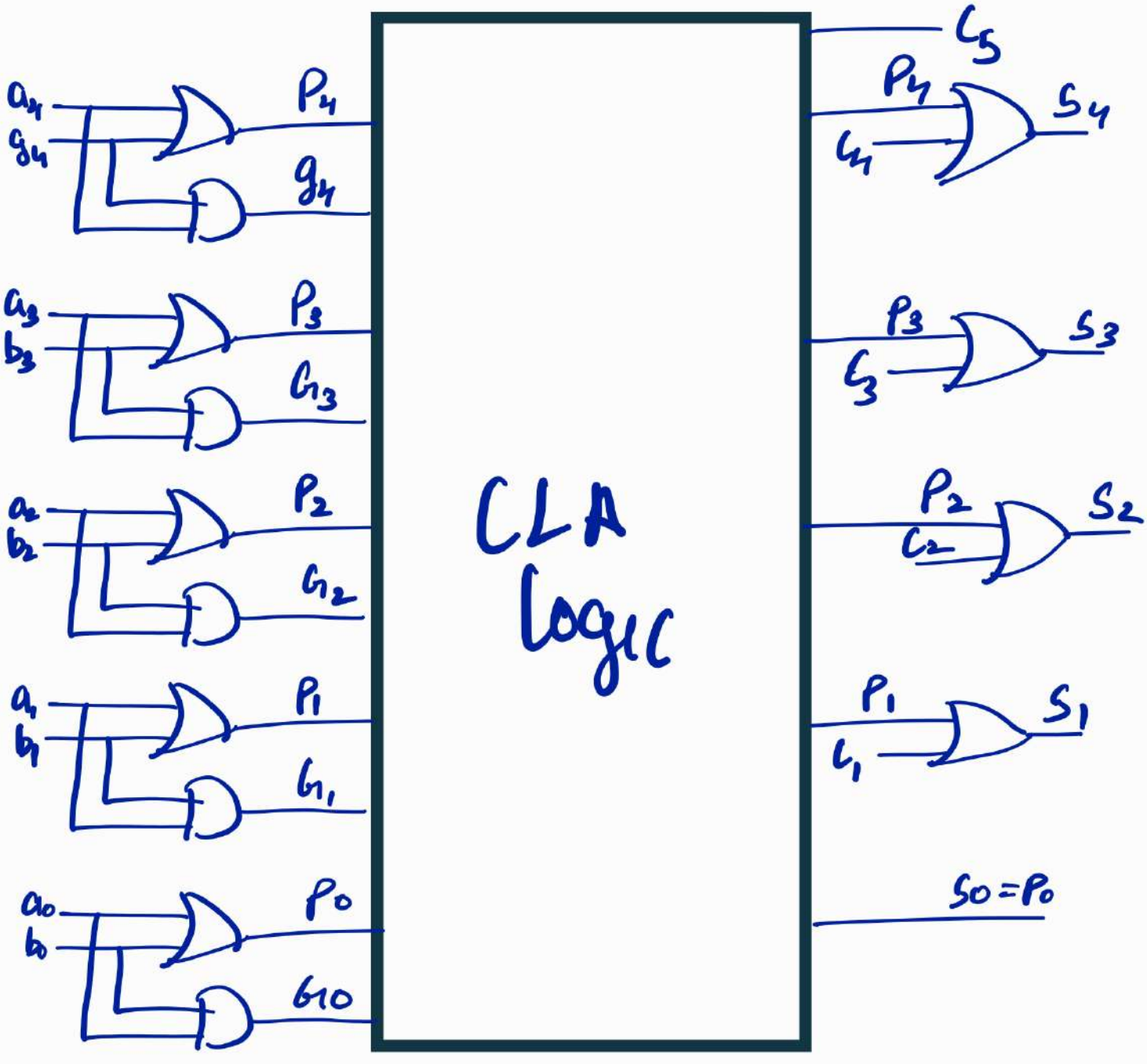
$C_4 = g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0$

$C_5 = g_4 + P_4 g_3 + P_4 P_3 g_2 + P_4 P_3 P_2 g_1 + P_4 P_3 P_2 P_1 g_0$

$g_i = a_i b_i$

$P_i = a_i \oplus b_i$

$S_i = P_i \oplus C_i$



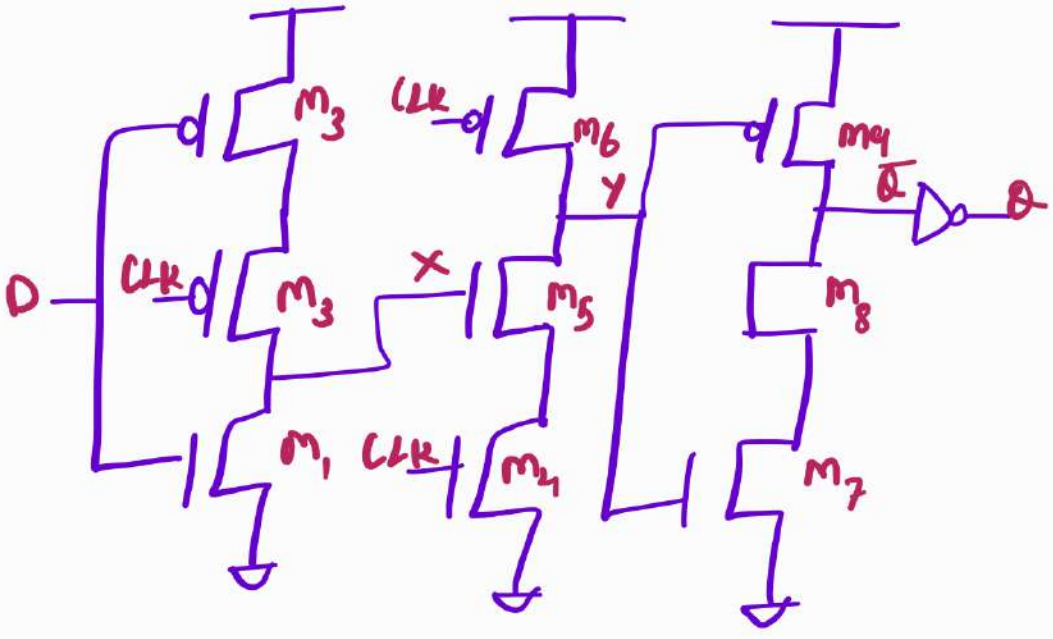
⇒ we are directly going to implement carry bits using Static CMOS style. instead of generating carry using multiple AND & OR gates.

$Y = \overline{Cout}$

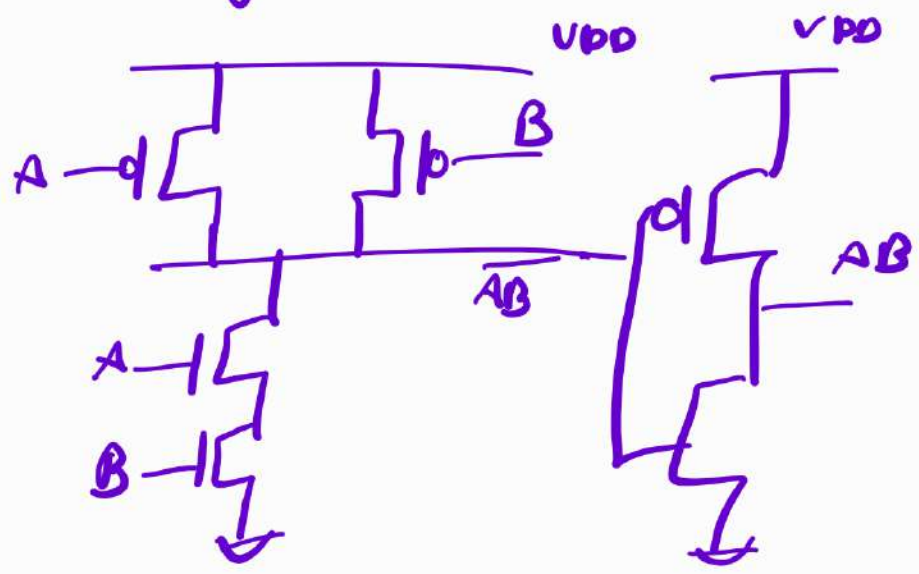
↳ directly implement in Static CMOS

(Q2) For the Sizing the DFF1 AND gates are $(W_p, W_n) = (20\lambda, 10\lambda)$ as for rest of the circuit I have done. $(W_p, W_n) = (40\lambda, 20\lambda)$. didn't focus on Sizing to minimum Inverters Since Since in Static CMOS is not ratioed logic So, only delay will increase, our main focus was on functionality.

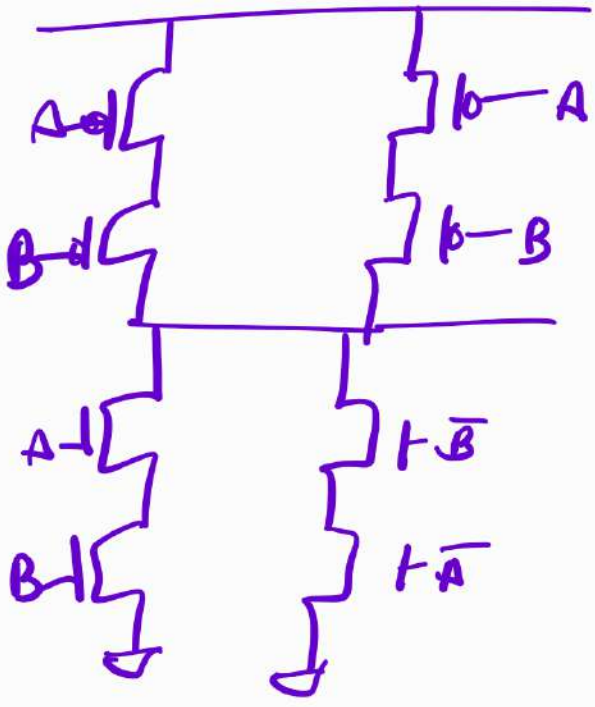
(b) DFlip Flop :-



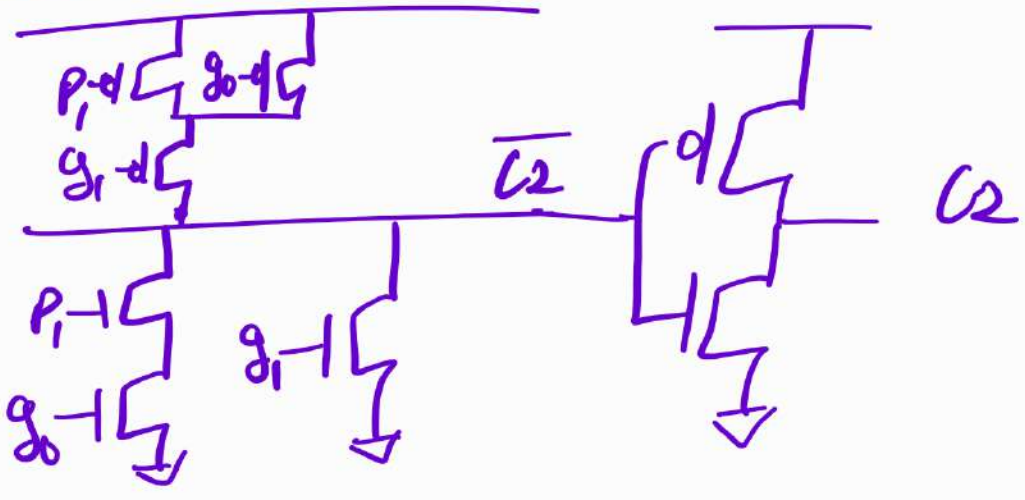
④ AND gate:-



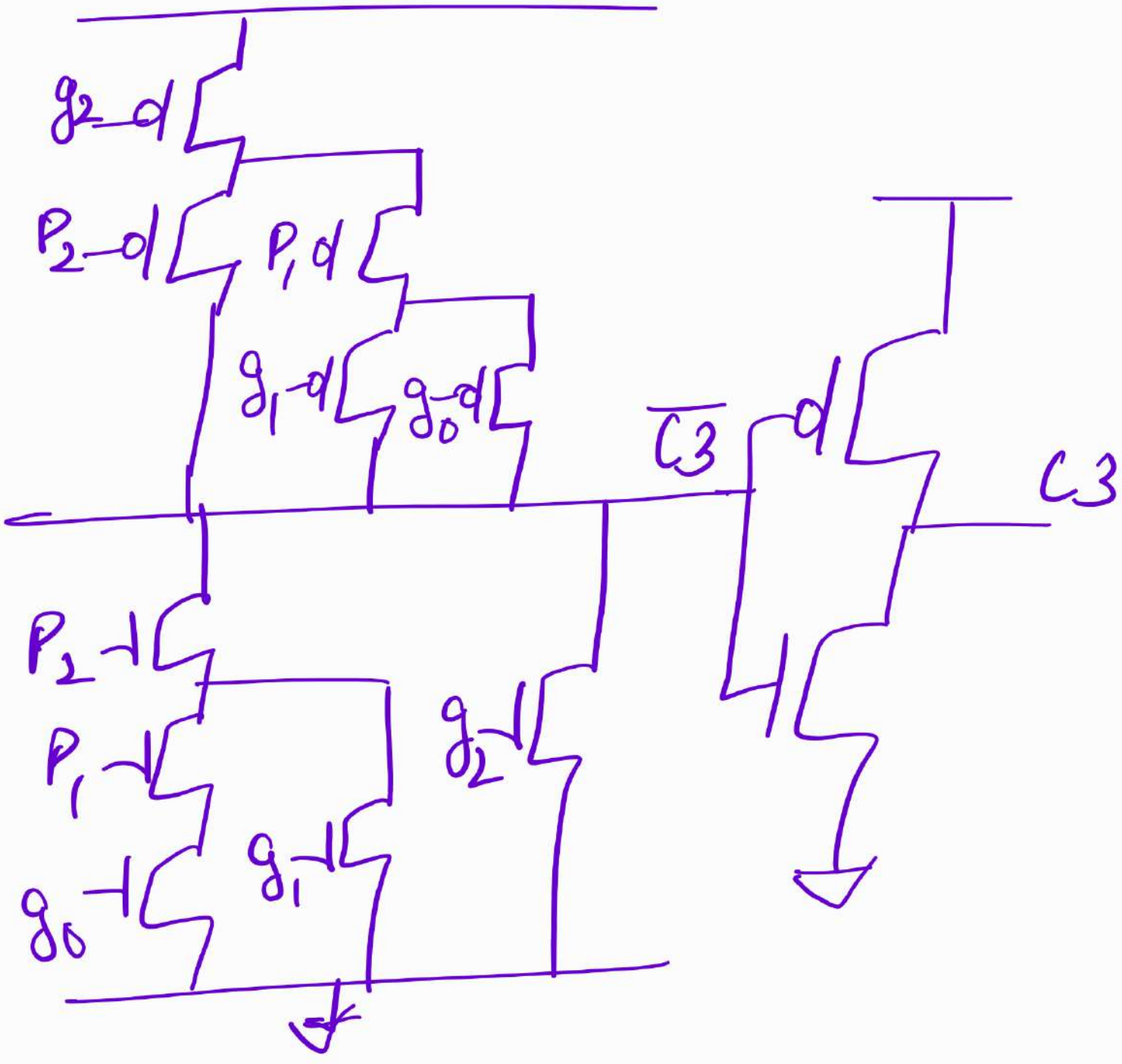
⑤ XOR



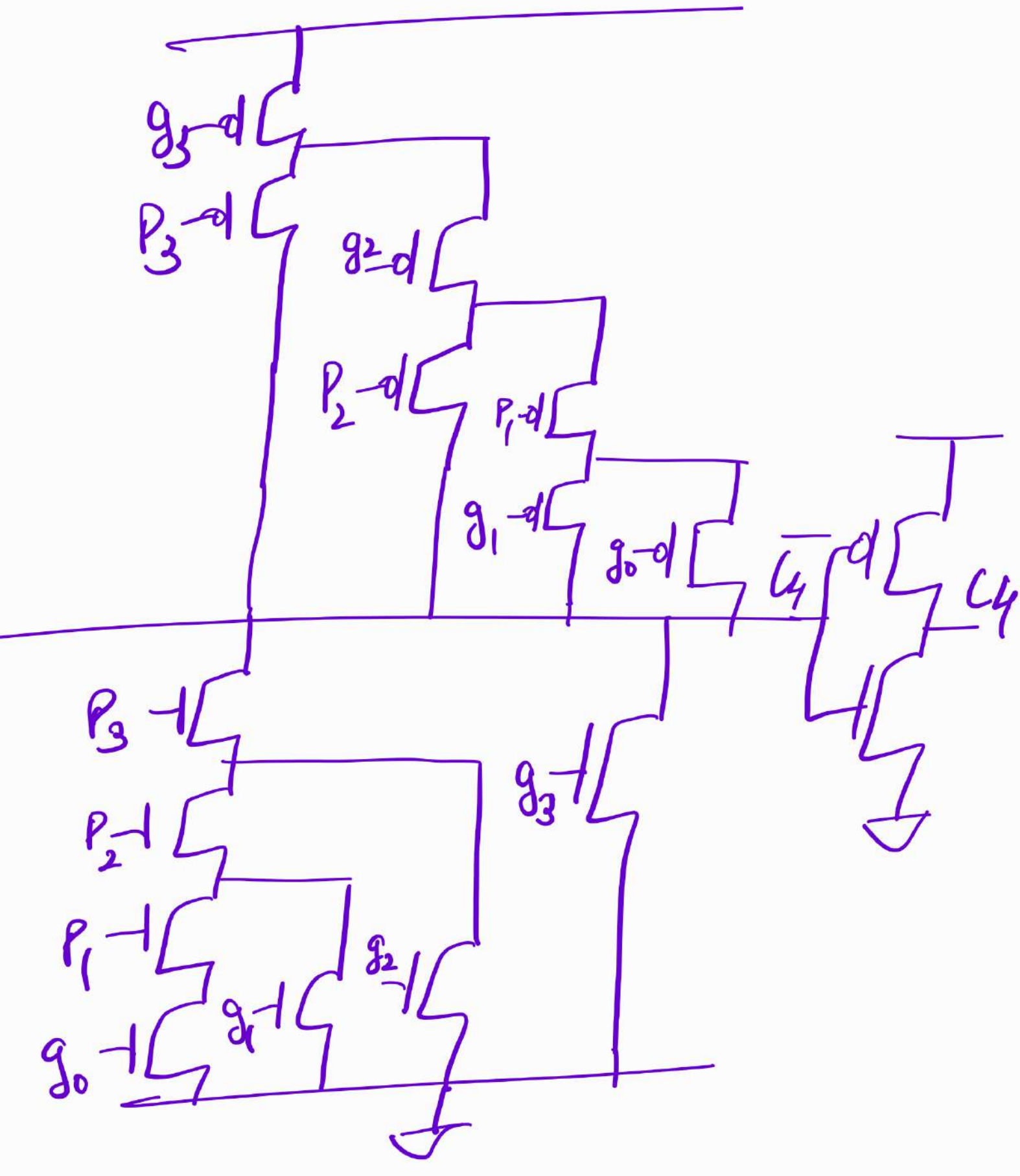
⑥ C2



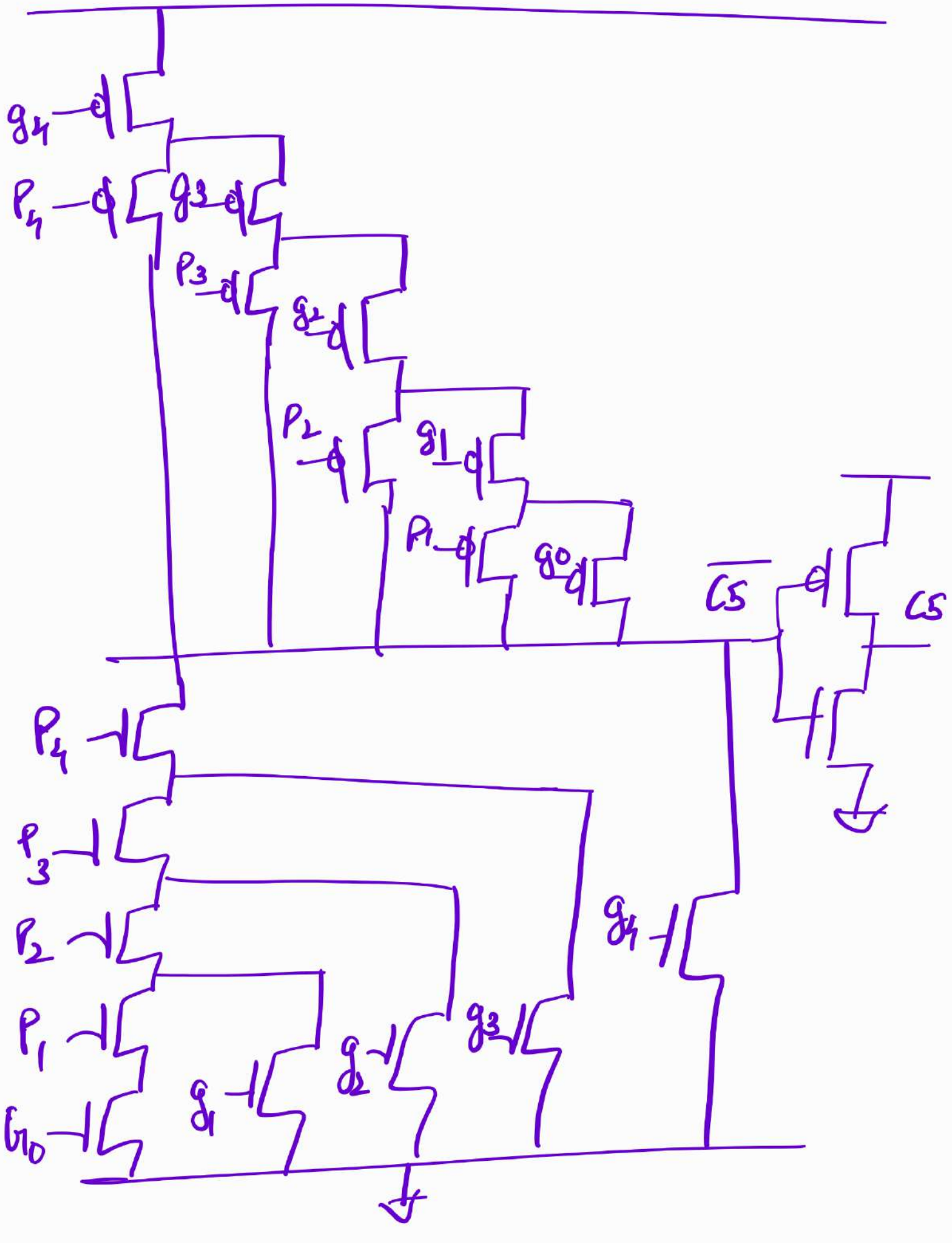
(d) C3 :-



(d) C_4 :-

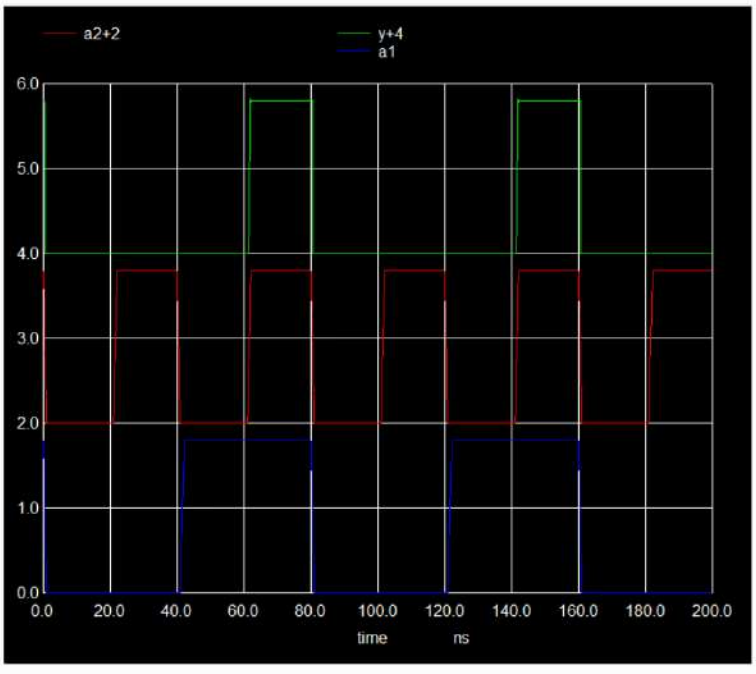


⊛ C5 :-



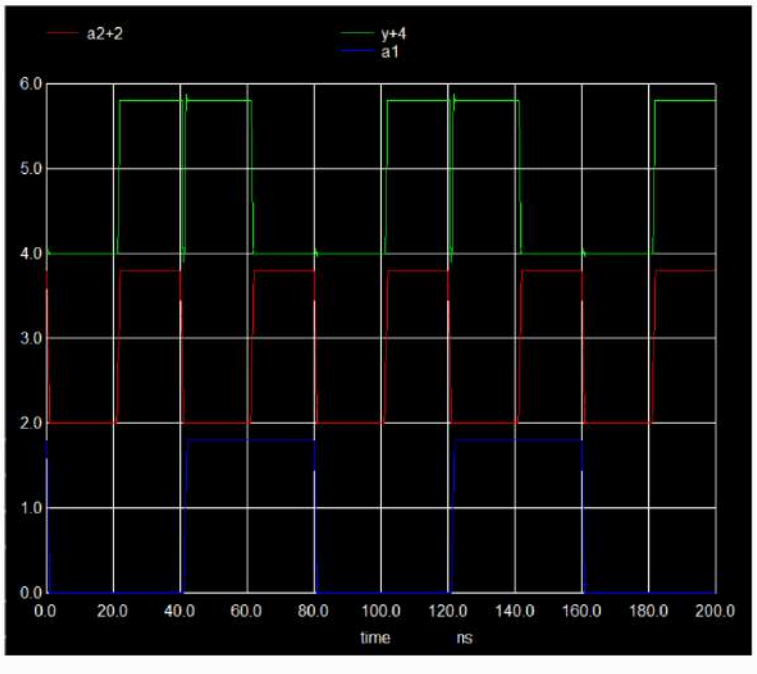
Q3 ① AND2 :-

```
.include TSMC_180nm.txt
.include INV.sp
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VA2 A2 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VA1 A1 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
Vdd vdd gnd 'SUPPLY'

.subckt and2 Y A B vdd gnd
.param width_N={20*LAMBDA}
.param width_P={20*LAMBDA}

M1 Y_bar A n1 gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 n1 B gnd gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 Y_bar A vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M4 Y_bar B vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

x_and2 Y Y_bar vdd gnd inv
.ends and2

x_and Y A2 A1 vdd gnd and2


.tran 10n 200n

.control
set hcopypscolor = 0 *White background for saving plots
set color0=black ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=white ** color1 is used to set the grid color of the plot (manual sec:17.7))
run

plot Y+4 A2+2 A1

.endc
.end
```



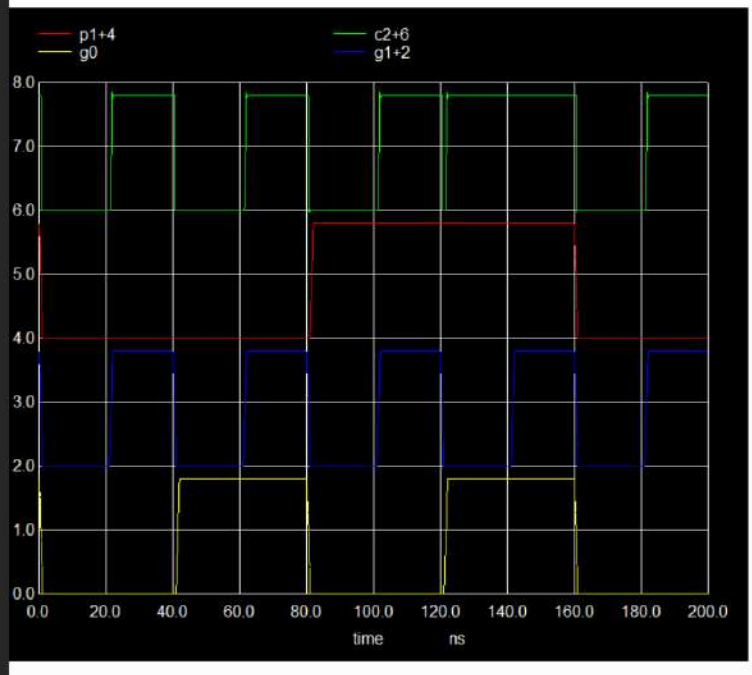
② XOR2 :-

```
.include TSMC_180nm.txt
.include INV.sp
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VA2 A2 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VA1 A1 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
Vdd vdd gnd 'SUPPLY'

.subckt xor2 Y A B vdd gnd
.param width_N={20*LAMBDA}
.param width_P={40*LAMBDA}

x_a A_bar A   vdd gnd inv
x_b B_bar B   vdd gnd inv

M1 n1 A vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M2 n1 B vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M3 Y A_bar n1 vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M4 Y B_bar n1 vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M5 Y A n2 gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M6 n2 B gnd gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M7 Y A_bar n3 gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M8 n3 B_bar gnd gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.ends xor2

x_and Y A2 A1 vdd gnd xor2


.tran 10n 200n

.control
set hcopypscolor = 0 *White background for saving plots
set color0=black ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=white ** color1 is used to set the grid color of the plot (manual sec:17.7))
run

plot Y+4 A2+2 A1

.endc
.end
```



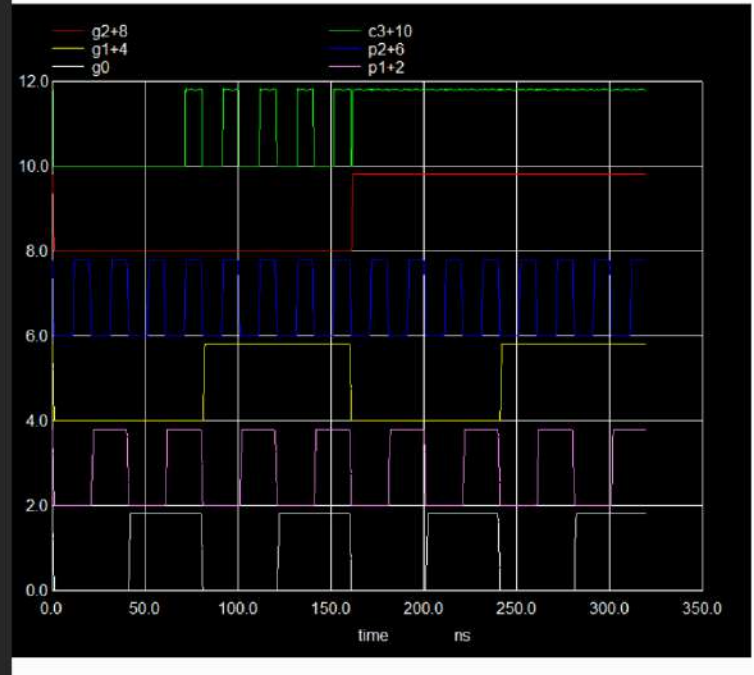
② Carry 2 :-

```
.include TSMC_180nm.txt
.include INV.sp
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VG1 G1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
Vdd vdd gnd 'SUPPLY'

.subckt carry2 C2 G1 P1 G0 vdd gnd
.param width_N={10*LAMBDA}
.param width_P={40*LAMBDA}

M1 C2_bar G1 n1 vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M2 n1 P1 vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
M3 n1 G0 vdd vdd CMOSP W={width_P} L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M4 C2_bar G1 gnd gnd CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M5 C2_bar P1 n2 gnd CMOSN W={width_N*2} L={LAMBDA}
+ AS={5*width_N*2*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*2*width_N*LAMBDA} PD={10*LAMBDA+2*2*width_N}
M6 n2 G0 gnd gnd CMOSN W={width_N*2} L={LAMBDA}
+ AS={5*width_N*2*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*2*width_N*LAMBDA} PD={10*LAMBDA+2*2*width_N}

x_carry2 C2 C2_bar vdd gnd inv
.ends carry2

x_and C2 G1 P1 G0 vdd gnd carry2


.tran 10n 200n

.control
set hcopypscolor = 0 *White background for saving plots
set color0=black ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=white ** color1 is used to set the grid color of the plot (manual sec:17.7))
run

plot C2+6 P1+4 G1+2 G0

.endc
.end
```



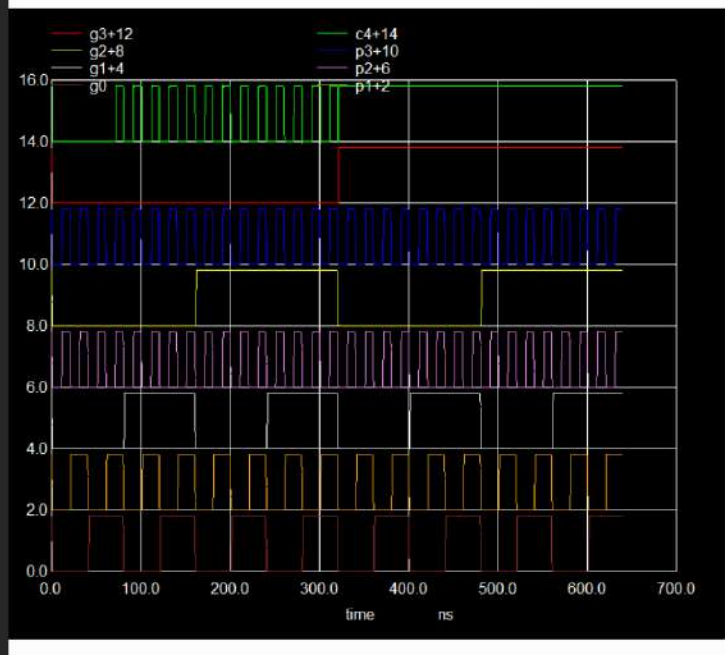
③ Carry 3 :-

```
.include TSMC_180nm.txt
.include INV.sp
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
Vdd vdd gnd 'SUPPLY'

.subckt carry3 C3 G2 P2 G1 P1 G0 vdd gnd
.param width_N={10*LAMBDA}
.param width_P_base={20*LAMBDA}

M1    C3_bar  G2      gnd     gnd     CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2    C3_bar  P2      n1_nmos gnd     CMOSN W={width_N*3} L={LAMBDA}
+ AS={5*width_N*3*LAMBDA} PS={10*LAMBDA+2*3*width_N} AD={5*3*width_N*LAMBDA} PD={10*LAMBDA+2*3*width_N}
M3    n1_nmos G1      gnd     gnd     CMOSN W={width_N*2} L={LAMBDA}
+ AS={5*width_N*2*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*2*width_N*LAMBDA} PD={10*LAMBDA+2*2*width_N}
M4    n1_nmos P1      n2_nmos gnd     CMOSN W={width_N*3} L={LAMBDA}
+ AS={5*width_N*3*LAMBDA} PS={10*LAMBDA+2*3*width_N} AD={5*3*width_N*LAMBDA} PD={10*LAMBDA+2*3*width_N}
M5    n2_nmos G0      gnd     gnd     CMOSN W={width_N*3} L={LAMBDA}
+ AS={5*width_N*3*LAMBDA} PS={10*LAMBDA+2*3*width_N} AD={5*3*width_N*LAMBDA} PD={10*LAMBDA+2*3*width_N}

M6  n1_pmos G2      vdd     vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*3*width_P_base*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
M7  C3_bar  P2      n1_pmos vdd     CMOSP W={width_P_base*2} L={LAMBDA}
+ AS={5*width_P_base*2*LAMBDA} PS={10*LAMBDA+2*2*width_P_base} AD={5*2*width_P_base*LAMBDA} PD={10*LAMBDA+2*2*width_P_base}
M8  n2_pmos G1      n1_pmos vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*3*width_P_base*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
M9  C3_bar  P1      n2_pmos vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*3*width_P_base*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
M10  C3_bar  G0      n2_pmos vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*3*width_P_base*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
x_carry3 C3 C3_bar vdd gnd inv
.ends carry3

x_and C3 G2 P2 G1 P1 G0 vdd gnd carry3
.tran 10n 320n
.control
set hcopypscolor = 0 *White background for saving plots
set color0=black ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=white ** color1 is used to set the grid color of the plot (manual sec:17.7))
run
plot C3+10 G2+8 P2+6 G1+4 P1+2 G0
.endc
.end
```



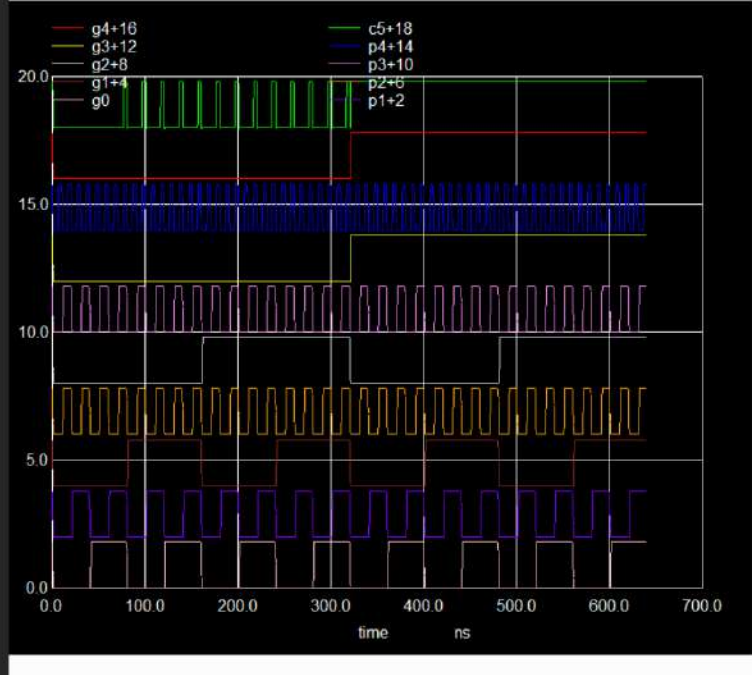
(d) Carry 4 :-

```
.include TSMC_180nm.txt
.include INV.sp
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VP3 P3 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
VG3 G3 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
Vdd vdd gnd 'SUPPLY'

.subckt carry4 C4 G3 P3 G2 P2 G1 P1 G0 vdd gnd
.param width_N={10*LAMBDA}
.param width_P_base={20*LAMBDA}

M1    C4_bar  G3      gnd     gnd     CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2    C4_bar  P3      n1_nmos gnd     CMOSN W={width_N*4} L={LAMBDA}
+ AS={5*width_N*4*LAMBDA} PS={10*LAMBDA+2*4*width_N} AD={5*width_N*4*LAMBDA} PD={10*LAMBDA+2*4*width_N}
M3    n1_nmos G2      gnd     gnd     CMOSN W={width_N*2} L={LAMBDA}
+ AS={5*width_N*2*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*width_N*2*LAMBDA} PD={10*LAMBDA+2*2*width_N}
M4    n1_nmos P2      n2_nmos gnd     CMOSN W={width_N*4} L={LAMBDA}
+ AS={5*width_N*4*LAMBDA} PS={10*LAMBDA+2*4*width_N} AD={5*width_N*4*LAMBDA} PD={10*LAMBDA+2*4*width_N}
M5    n2_nmos G1      gnd     gnd     CMOSN W={width_N*3} L={LAMBDA}
+ AS={5*width_N*3*LAMBDA} PS={10*LAMBDA+2*3*width_N} AD={5*width_N*3*LAMBDA} PD={10*LAMBDA+2*3*width_N}
M6    n2_nmos P1      n3_nmos gnd     CMOSN W={width_N*4} L={LAMBDA}
+ AS={5*width_N*4*LAMBDA} PS={10*LAMBDA+2*4*width_N} AD={5*width_N*4*LAMBDA} PD={10*LAMBDA+2*4*width_N}
M7    n3_nmos G0      gnd     gnd     CMOSN W={width_N*4} L={LAMBDA}
+ AS={5*width_N*4*LAMBDA} PS={10*LAMBDA+2*4*width_N} AD={5*width_N*4*LAMBDA} PD={10*LAMBDA+2*4*width_N}

M8  n1_pmos G3      vdd     vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}
M9  C4_bar  P3      n1_pmos vdd     CMOSP W={width_P_base*2} L={LAMBDA}
+ AS={5*width_P_base*2*LAMBDA} PS={10*LAMBDA+2*2*width_P_base} AD={5*width_P_base*2*LAMBDA} PD={10*LAMBDA+2*2*width_P_base}
M10 n2_pmos G2      n1_pmos vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}
M11 C4_bar  P2      n2_pmos vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*width_P_base*3*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
M12 n3_pmos G1      n2_pmos vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}
M13 C4_bar  P1      n3_pmos vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}
M14 C4_bar  G0      n3_pmos vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}

x_carry4 C4 C4_bar vdd gnd inv
.ends carry4
```



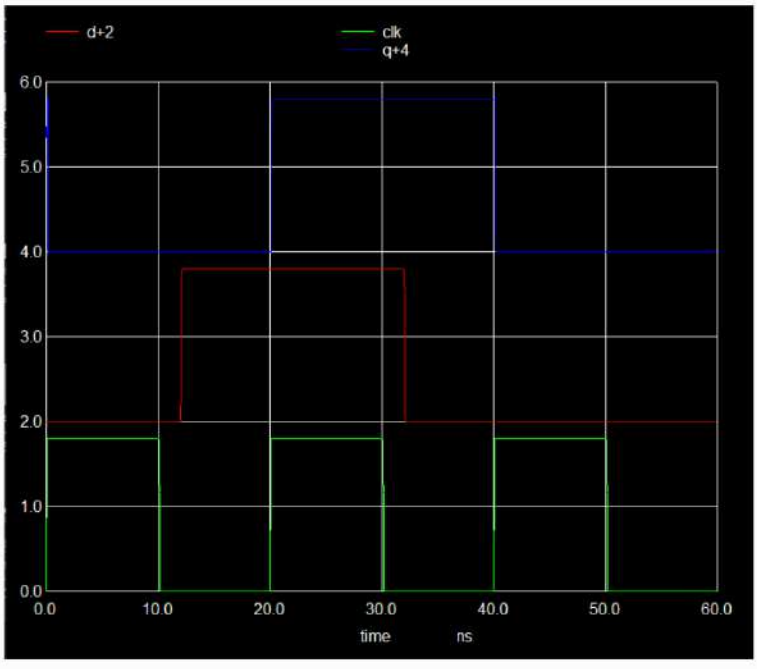
(e) Carry 5 :-

```
VP4 P4 gnd PULSE(1.8 0 0 1n 1n 5n 10n)
VP3 P3 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
VG3 G3 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
VG4 G4 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
Vdd vdd gnd 'SUPPLY'

.subckt carry5 C5 G4 P4 G3 P3 G2 P2 G1 P1 G0 vdd gnd
.param width_N={10*LAMBDA}
.param width_P_base={20*LAMBDA}

M1    C5_bar  G4      gnd     gnd     CMOSN W={width_N} L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2    C5_bar  P4      n1_nmos gnd     CMOSN W={width_N*5} L={LAMBDA}
+ AS={5*width_N*5*LAMBDA} PS={10*LAMBDA+2*5*width_N} AD={5*width_N*5*LAMBDA} PD={10*LAMBDA+2*5*width_N}
M3    n1_nmos G3      gnd     gnd     CMOSN W={width_N*2} L={LAMBDA}
+ AS={5*width_N*2*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*width_N*2*LAMBDA} PD={10*LAMBDA+2*2*width_N}
M4    n1_nmos P3      n2_nmos gnd     CMOSN W={width_N*5} L={LAMBDA}
+ AS={5*width_N*5*LAMBDA} PS={10*LAMBDA+2*5*width_N} AD={5*width_N*5*LAMBDA} PD={10*LAMBDA+2*5*width_N}
M5    n2_nmos G2      gnd     gnd     CMOSN W={width_N*3} L={LAMBDA}
+ AS={5*width_N*3*LAMBDA} PS={10*LAMBDA+2*3*width_N} AD={5*width_N*3*LAMBDA} PD={10*LAMBDA+2*3*width_N}
M6    n2_nmos P2      n3_nmos gnd     CMOSN W={width_N*5} L={LAMBDA}
+ AS={5*width_N*5*LAMBDA} PS={10*LAMBDA+2*5*width_N} AD={5*width_N*5*LAMBDA} PD={10*LAMBDA+2*5*width_N}
M7    n3_nmos G1      gnd     gnd     CMOSN W={width_N*4} L={LAMBDA}
+ AS={5*width_N*4*LAMBDA} PS={10*LAMBDA+2*4*width_N} AD={5*width_N*4*LAMBDA} PD={10*LAMBDA+2*4*width_N}
M8    n3_nmos P1      n4_nmos gnd     CMOSN W={width_N*5} L={LAMBDA}
+ AS={5*width_N*5*LAMBDA} PS={10*LAMBDA+2*5*width_N} AD={5*width_N*5*LAMBDA} PD={10*LAMBDA+2*5*width_N}
M9    n4_nmos G0      gnd     gnd     CMOSN W={width_N*5} L={LAMBDA}
+ AS={5*width_N*5*LAMBDA} PS={10*LAMBDA+2*5*width_N} AD={5*width_N*5*LAMBDA} PD={10*LAMBDA+2*5*width_N}

M10 n1_pmos G4      vdd     vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}
M11 C5_bar  P4      n1_pmos vdd     CMOSP W={width_P_base*2} L={LAMBDA}
+ AS={5*width_P_base*2*LAMBDA} PS={10*LAMBDA+2*2*width_P_base} AD={5*width_P_base*2*LAMBDA} PD={10*LAMBDA+2*2*width_P_base}
M12 n2_pmos G3      n1_pmos vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}
M13 C5_bar  P3      n2_pmos vdd     CMOSP W={width_P_base*3} L={LAMBDA}
+ AS={5*width_P_base*3*LAMBDA} PS={10*LAMBDA+2*3*width_P_base} AD={5*width_P_base*3*LAMBDA} PD={10*LAMBDA+2*3*width_P_base}
M14 n3_pmos G2      n2_pmos vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}
M15 C5_bar  P2      n3_pmos vdd     CMOSP W={width_P_base*4} L={LAMBDA}
+ AS={5*width_P_base*4*LAMBDA} PS={10*LAMBDA+2*4*width_P_base} AD={5*width_P_base*4*LAMBDA} PD={10*LAMBDA+2*4*width_P_base}
M16 n4_pmos G1      n3_pmos vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}
M17 C5_bar  P1      n4_pmos vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}
M18 C5_bar  G0      n4_pmos vdd     CMOSP W={width_P_base*5} L={LAMBDA}
+ AS={5*width_P_base*5*LAMBDA} PS={10*LAMBDA+2*5*width_P_base} AD={5*width_P_base*5*LAMBDA} PD={10*LAMBDA+2*5*width_P_base}

x_carry5 C5 C5_bar vdd gnd inv
.ends carry5

x_and C5 G4 P4 G3 P3 G2 P2 G1 P1 G0 vdd gnd carry5

.tran 1n 640n
.control
set hcopypscolor = 0 *White background for saving plots
set color0=black ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=white ** color1 is used to set the grid color of the plot (manual sec:17.7))
run
plot C5+18 G4+16 P4+14 G3+12 P3+10 G2+8 P2+6 G1+4 P1+2 G0
.endc
.end
```



(d) DFF :-

```
.include TSMC_180nm.txt
.include INV.sp
.param LAMBDA=0.09u
.global vdd gnd

Vdd vdd 0 1.8
Vclk clk 0 pulse(0 1.8 0 100p 100p 10n 20n)
Vdata D 0 pwl(0 0 12n 0 12.1n 1.8 32n 1.8 32.1n 0 60n 0)

.subckt d_flop Q D clk vdd gnd
.param Width_N = 10*LAMBDA
.param Width_P = 20*LAMBDA

M3 l1 D vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M2 X clk l1 vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M1 X D gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

M6 Y clk vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M5 Y X l2 gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}
M4 l2 clk gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

M9 Q_bar Y vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M8 Q_bar clk l3 gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}
M7 l3 Y gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

x1 Q Q_bar vdd gnd inv
.ends D_flipflop

Xdut Q D clk vdd gnd d_flop

.tran 0.01n 60n

.control
run
plot clk D+2 Q+4
.endc

.end
```



Q4 So, I implemented D-FlipFlop using the TSPC.

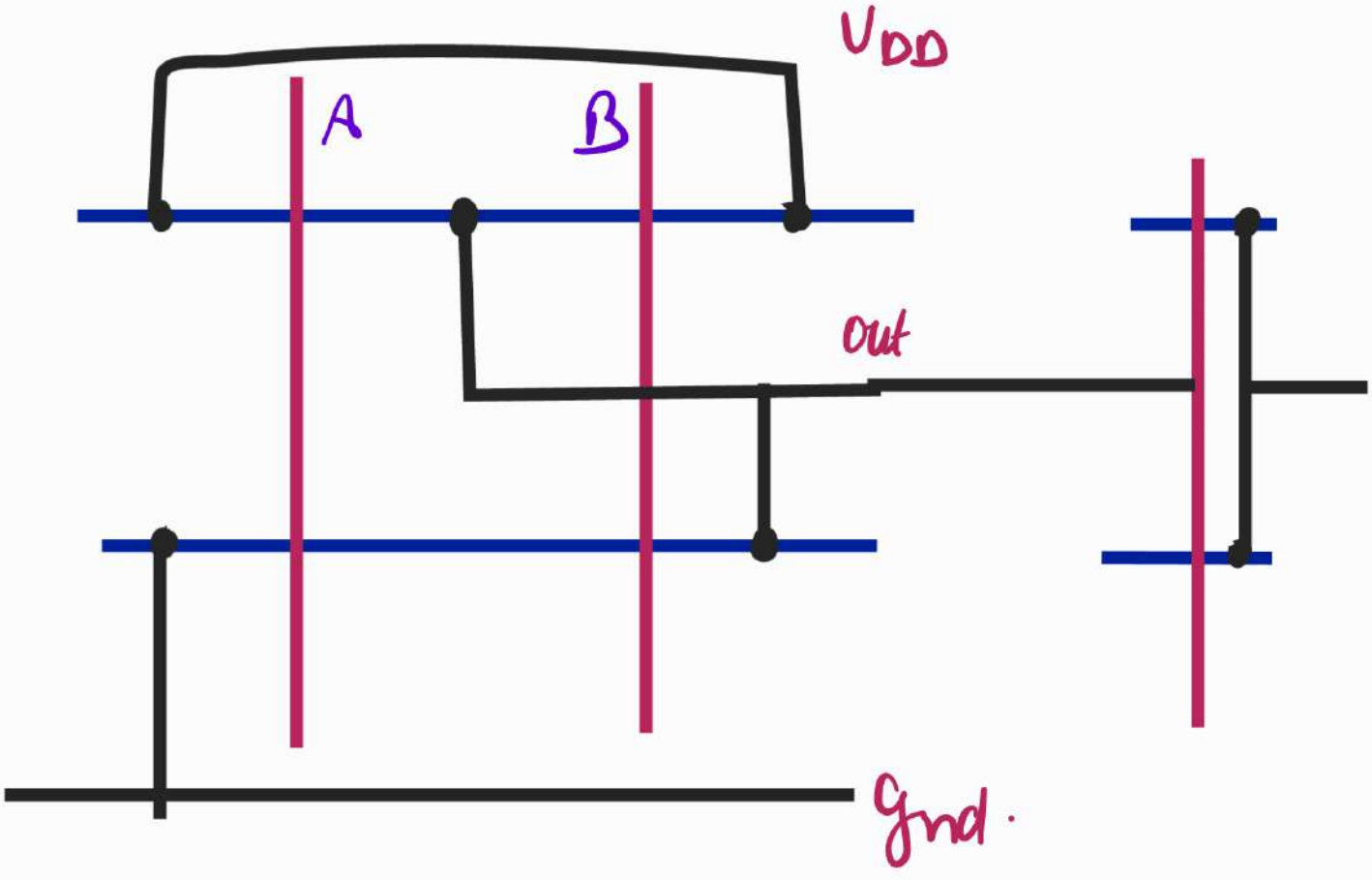
⇒ For TSPC the setup time is delay of stage one. & hold time is delay of State two.

```
.include TSMC_180nm.txt
.include INV.sp
.param LAMBDA=0.09u
.param Width_N = 10*LAMBDA
.param Width_P = 20*LAMBDA
.global vdd gnd

Vdd vdd 0 1.8
Vclk clk 0 pulse(0 1.8 0 100p 100p 10n 20n)
Vdata D 0 pwl(0 0 12n 0 12.1n 1.8 32n 1.8 32.1n 0 60n 0)


M3 11 D vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M2 X clk 11 vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M1 X D gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

M6 Y clk vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M5 Y X 12 gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}
M4 12 clk gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

M9 Q_bar Y vdd vdd CMOSP W={Width_P} L={2*LAMBDA}
+ AS={5*Width_P*LAMBDA} PS={10*LAMBDA+2*Width_P}
+ AD={5*Width_P*LAMBDA} PD={10*LAMBDA+2*Width_P}
M8 Q_bar clk 13 gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}
M7 13 Y gnd gnd CMOSN W={Width_N} L={2*LAMBDA}
+ AS={5*Width_N*LAMBDA} PS={10*LAMBDA+2*Width_N}
+ AD={5*Width_N*LAMBDA} PD={10*LAMBDA+2*Width_N}

x1 Q Q_bar vdd gnd inv


.tran 0.01n 60n
.measure tran tcpq
+ TRIG v(clk) VAL=0.9 RISE=1
+ TARG v(Q) VAL=0.9 RISE=1

.measure tran tsetup
+ TRIG v(D) VAL=0.9 RISE=1
+ TARG v(X) VAL=0.9 RISE=1

.measure tran thold
+ TRIG v(Y) VAL=0.9 RISE=1
+ TARG v(X) VAL=0.9 RISE=1

.control
run
plot clk D+2 Q+4
.endc

.end
```

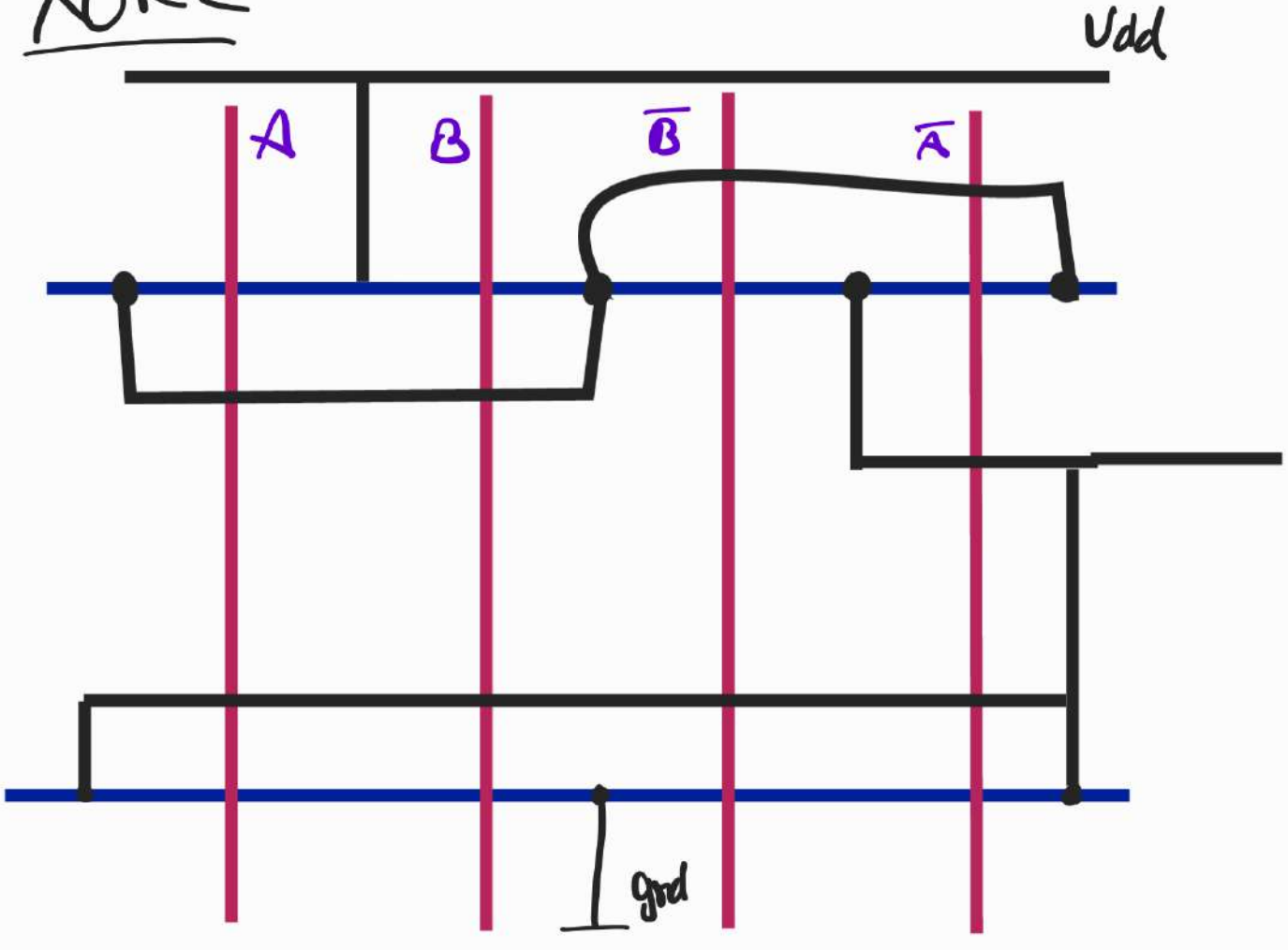
```
tcpq                =  6.852330e-11 targ=  2.011852e-08 trig=  2.005000e-08
tsetup              =  4.179198e-11 targ=  1.209179e-08 trig=  1.205000e-08
```

thold = 0, as its not dependent

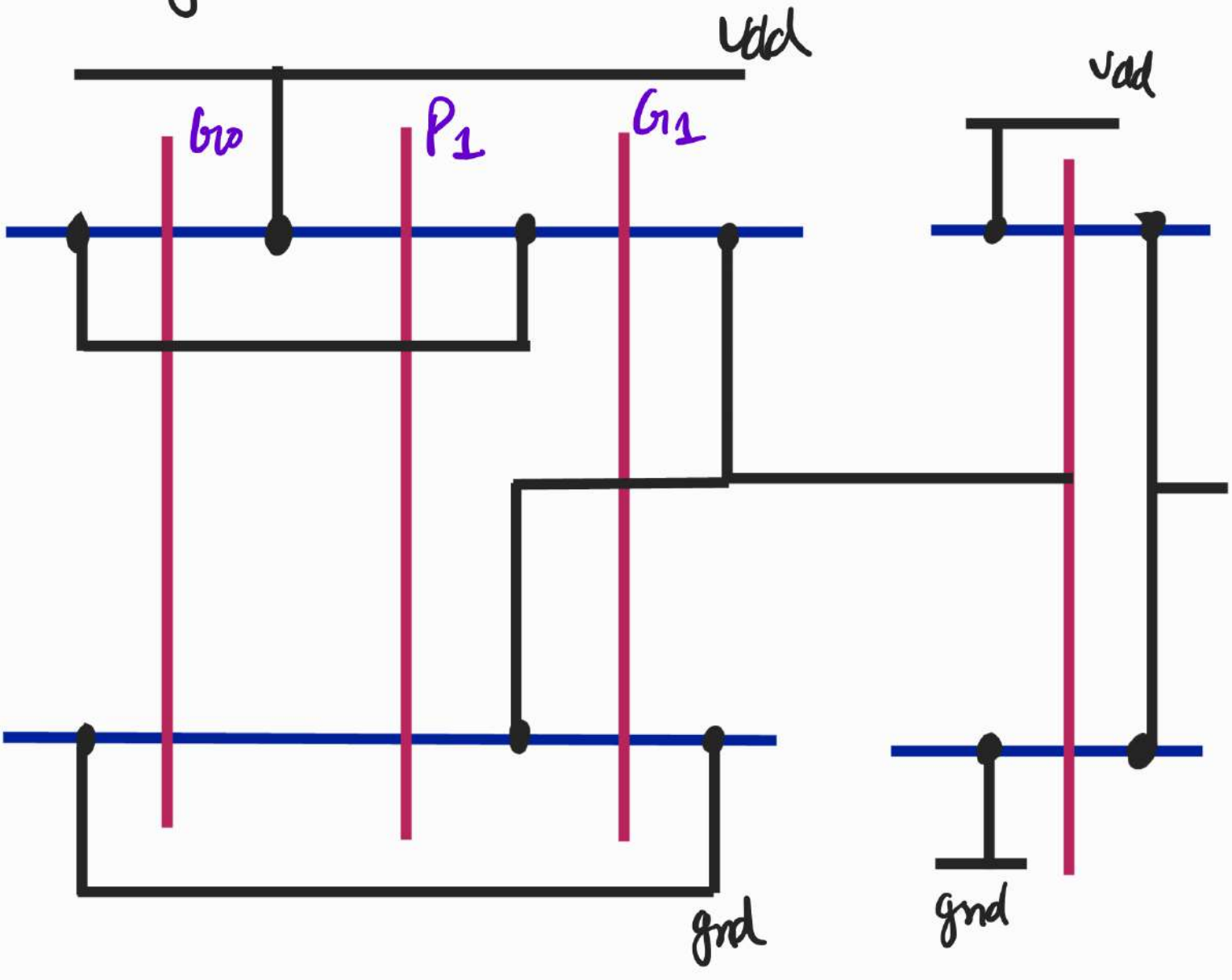
(05) AND2 :-



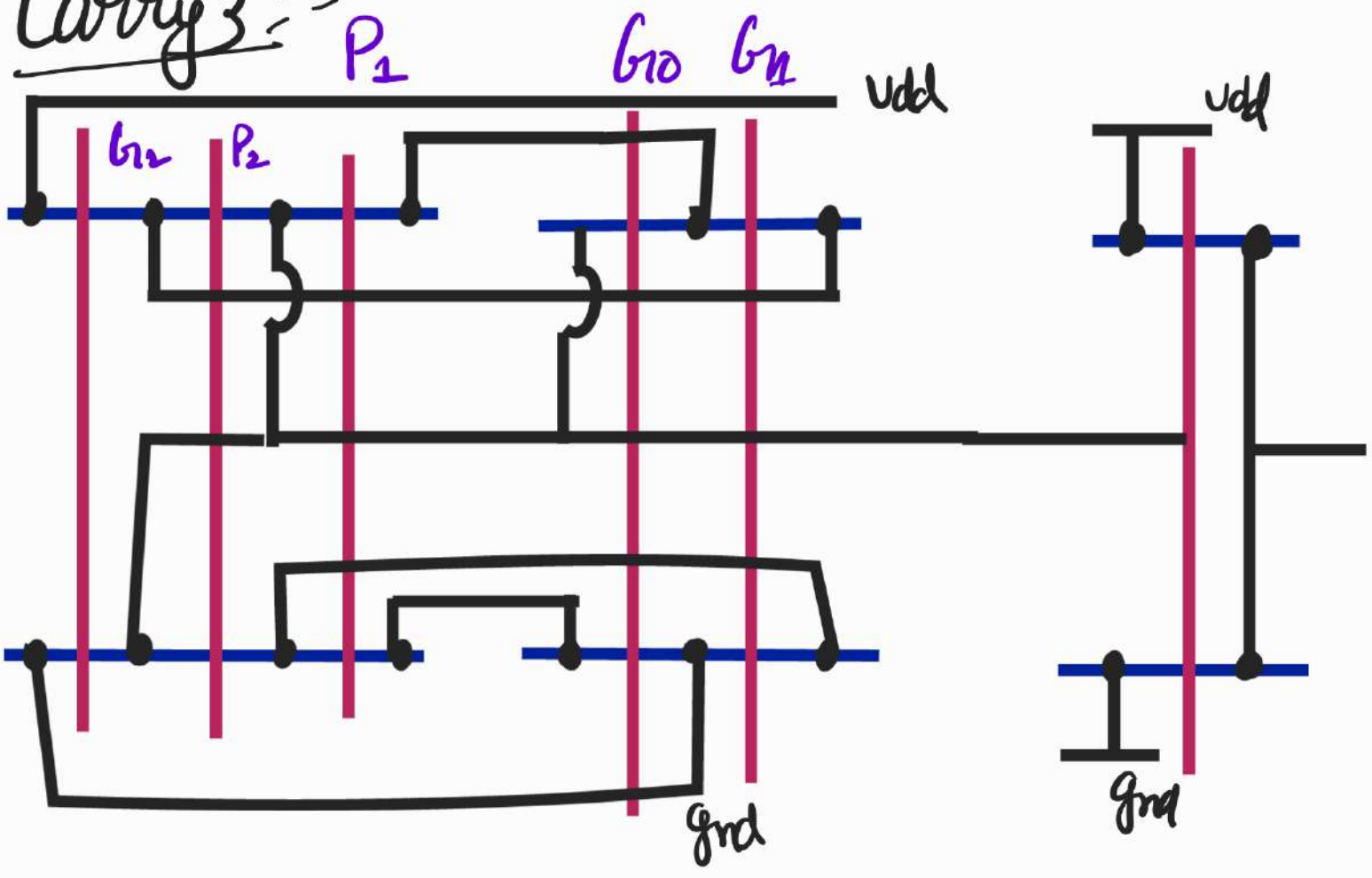
XOR2



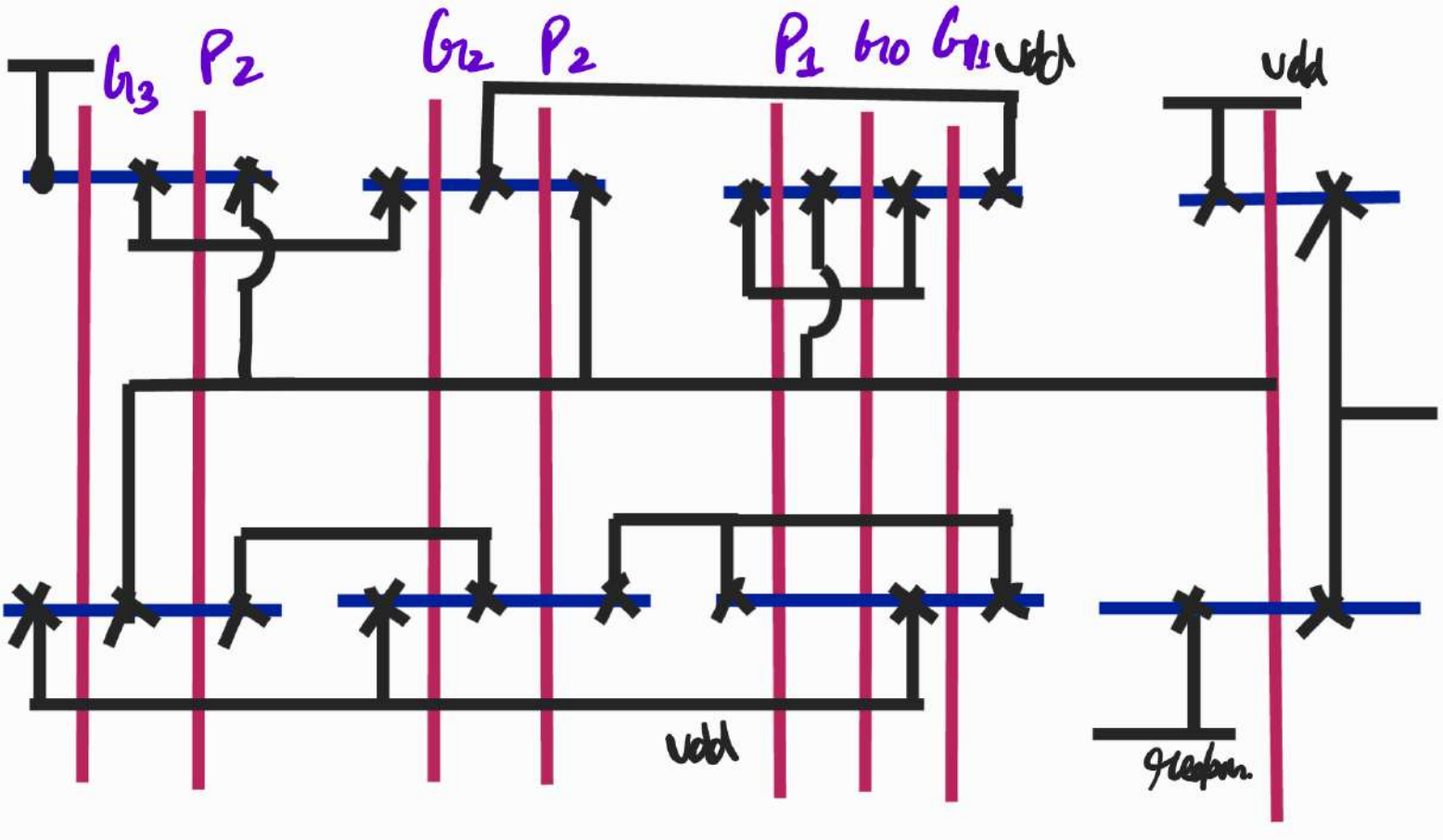
Carry2 :-



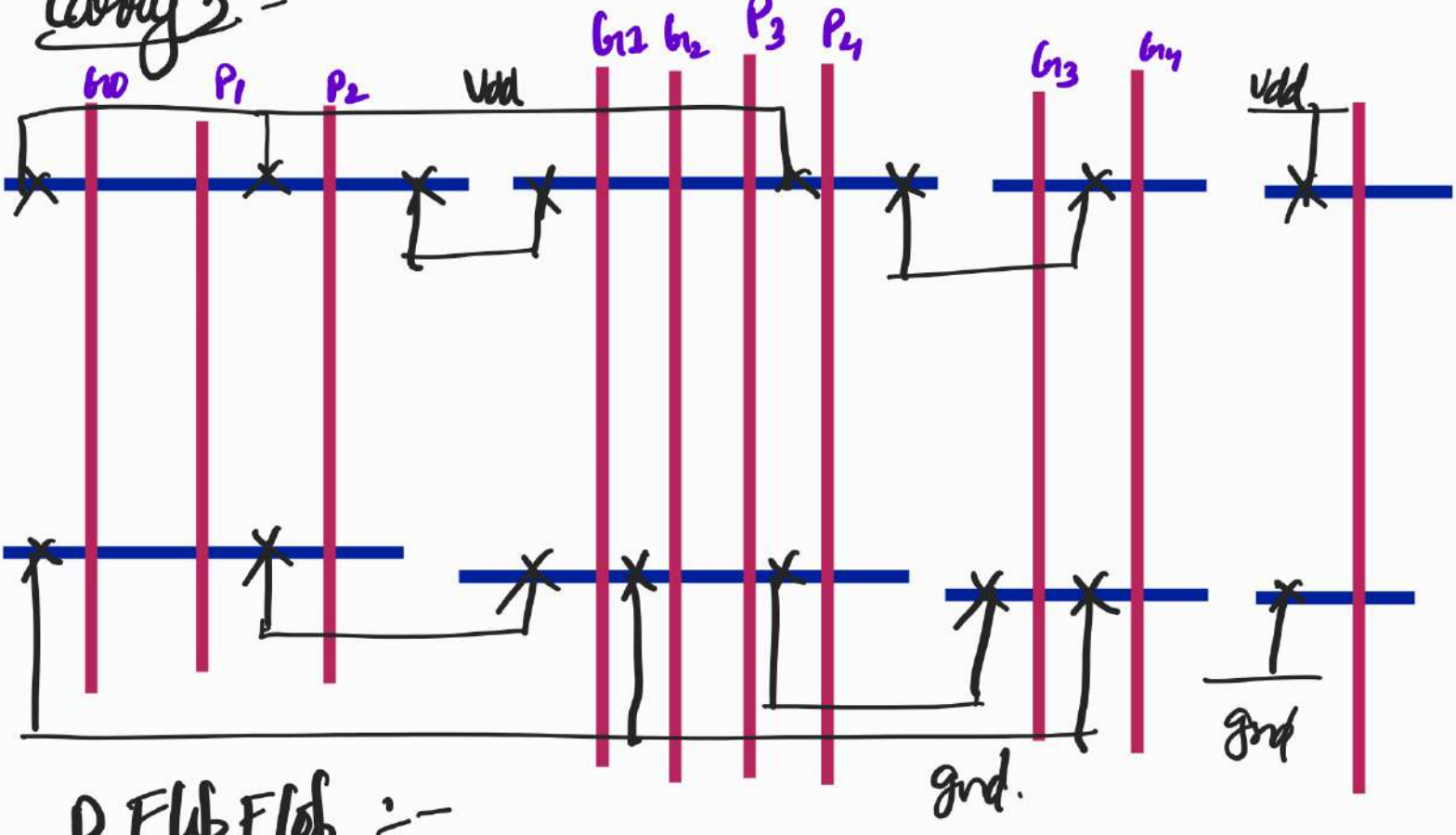
Carry 3 :-



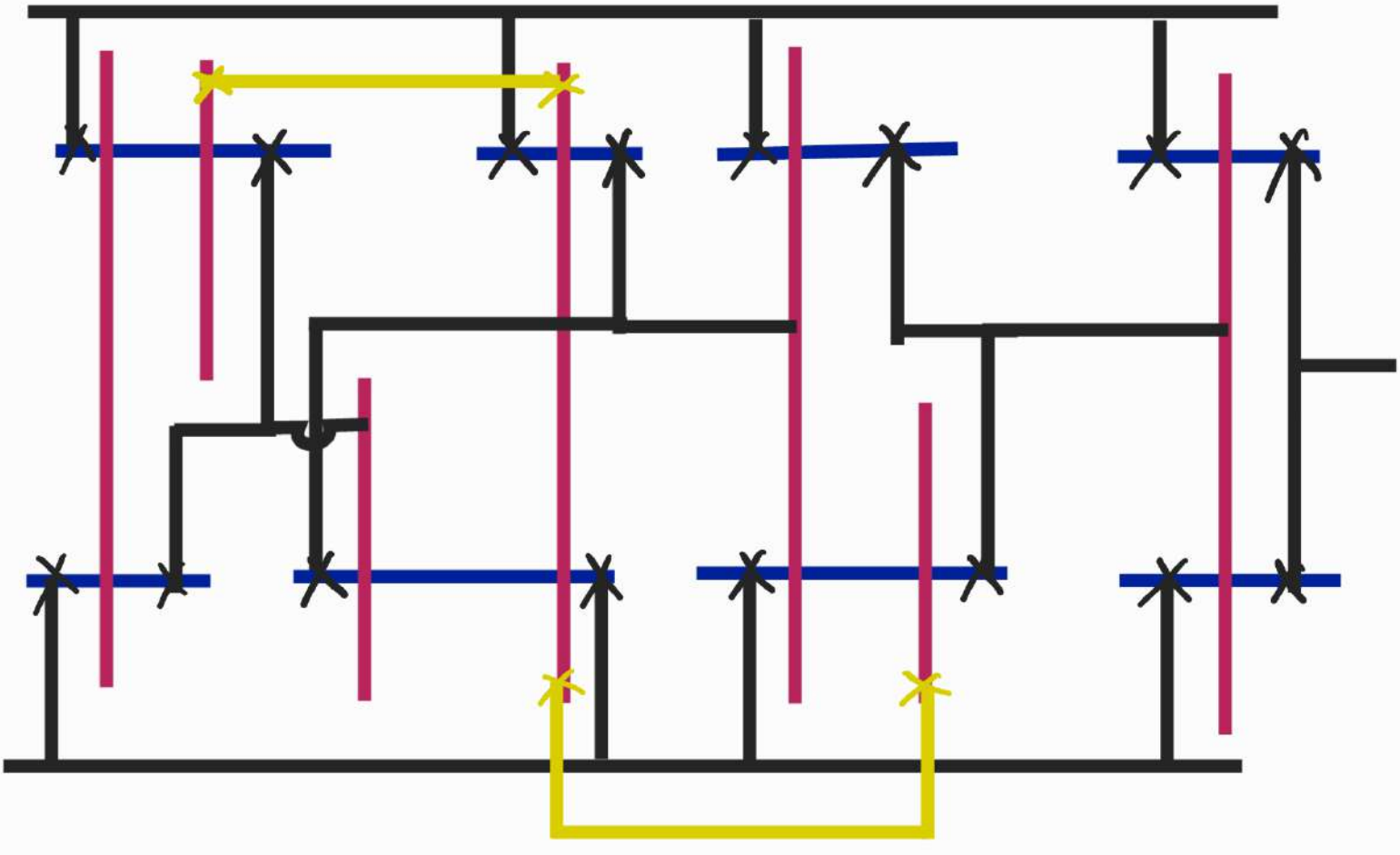
Carry 4



Carry 5 :-

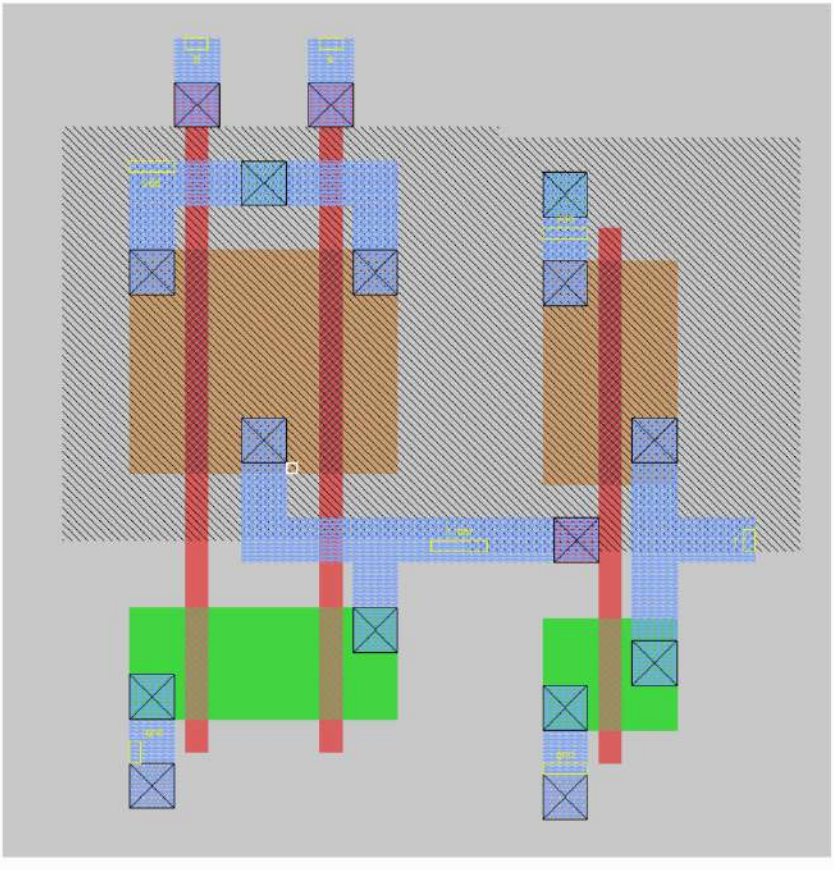


D Flip Flop :-

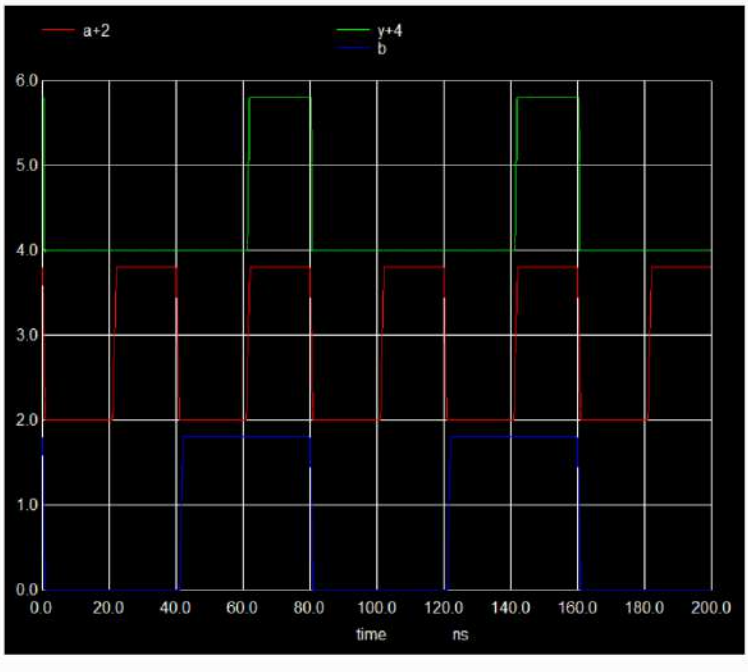


06 Post Layout :-

1 AND2 :-

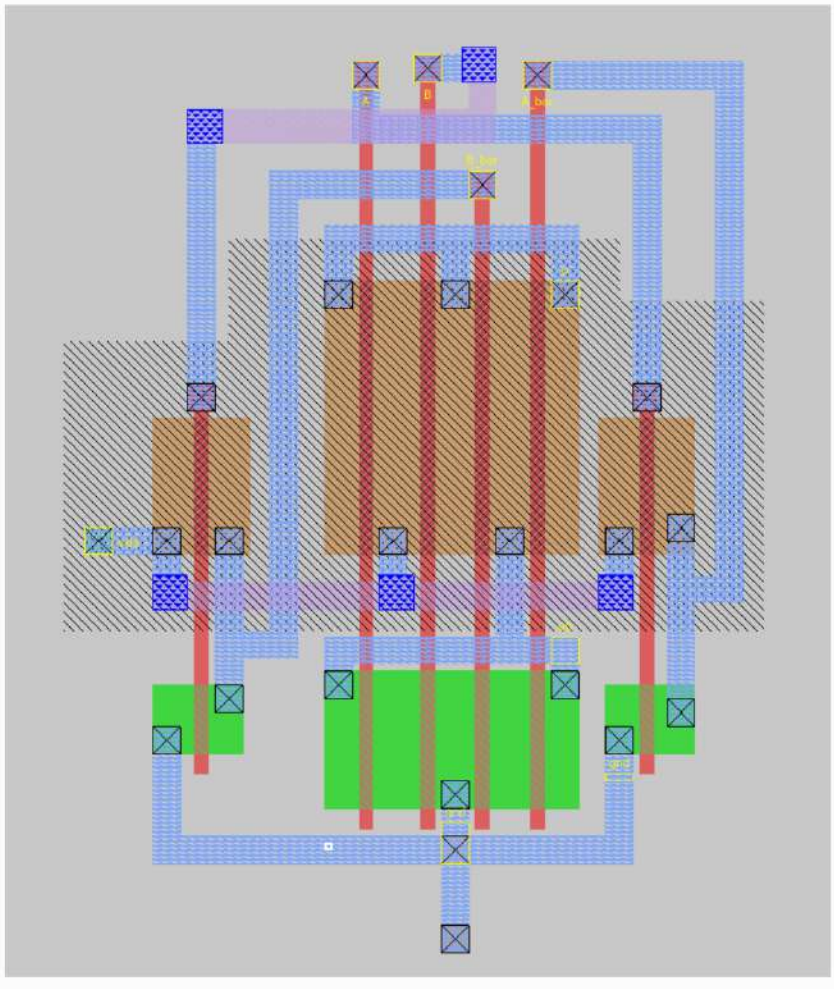


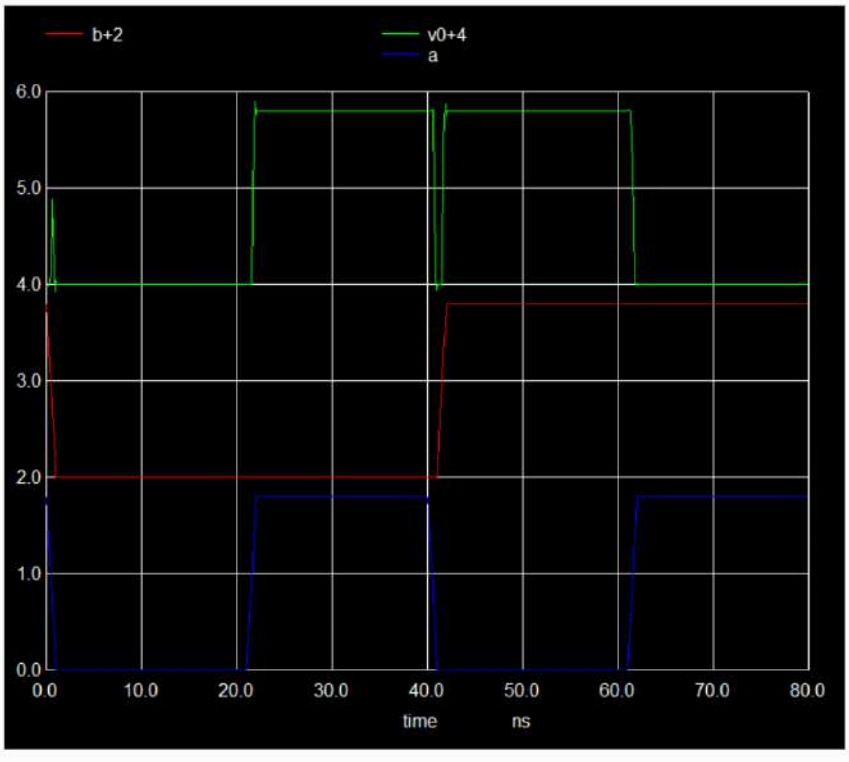
```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd
.option scale=90n

VA A gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VB B gnd PULSE(1.8 0 0 1n 1n 40n 80n)
Vdd vdd gnd 'SUPPLY'

M1000 a_n7_n22# B gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=20u as=50p ps=30u
M1001 Y_bar B vdd vdd CMOSP w=20 l=2
+  ad=100p pd=30u as=100p ps=50u
M1002 Y Y_bar gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1003 vdd A Y_bar vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=30u
M1004 Y_bar A a_n7_n22# Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=20u
M1005 Y Y_bar vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
C0 vdd Y 0.01479f
C1 B gnd 0
C2 gnd Y_bar 0
C3 B Y_bar 0.00218f
C4 Y gnd 0
C5 Y Y_bar 0.0587f
C6 Y_bar a_n7_n22# 0
C7 vdd A 0.0978f
C8 vdd B 0.0978f
C9 A Y_bar 0.00994f
C10 vdd Y_bar 0.05425f
C11 gnd 0 0.07419f
C12 Y 0 0.07523f
C13 Y_bar 0 0.25077f
C14 A 0 0.20467f
C15 B 0 0.20467f
C16 vdd 0 2.56609f


.tran 1n 200n

.control
set hcopypscolor = 0 *White background for saving plots
set color0=black
set color1=white
run

plot Y+4 A+2 B

.endc
.end
```



(4) XOR :-

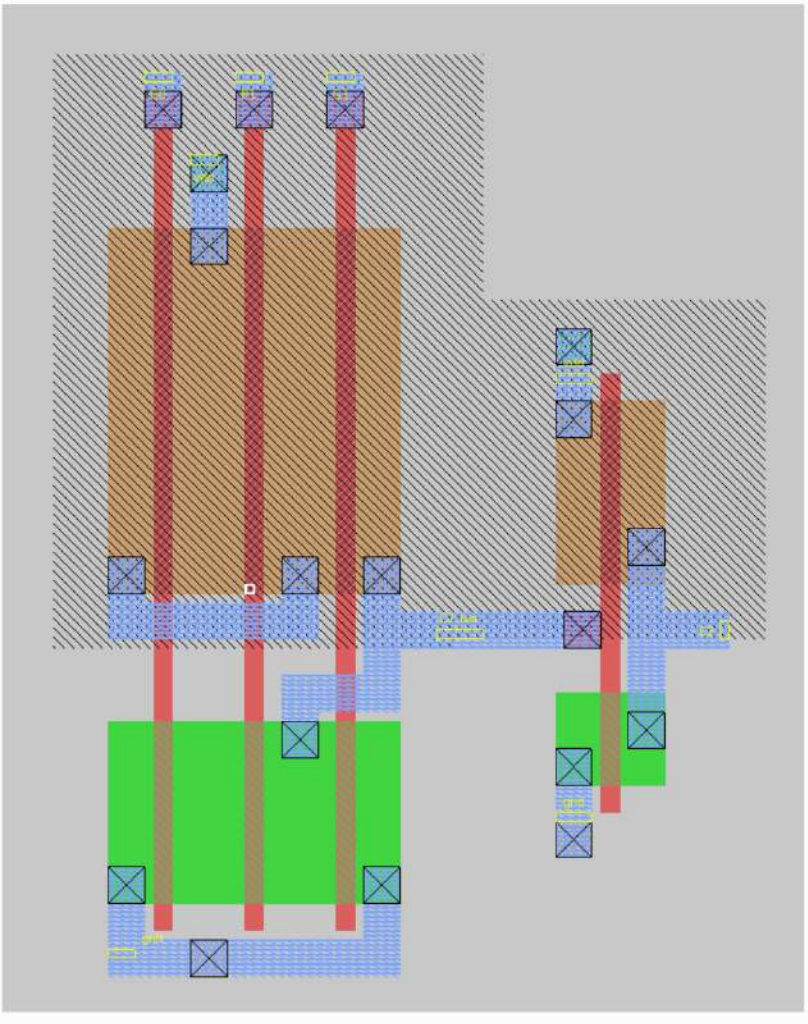
```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VA A gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VB B gnd PULSE(1.8 0 0 1n 1n 40n 80n)
Vdd vdd gnd 'SUPPLY'



.option scale=90n

M1000 B_bar B vdd vdd CMOSP w=20 l=2
+  ad=0.12n pd=52u as=0.12n ps=52u
M1001 A_bar A vdd vdd CMOSP w=20 l=2
+  ad=0.12n pd=52u as=0.12n ps=52u
M1002 gnd B a_7_6# Gnd CMOSN w=20 l=2
+  ad=60p pd=26u as=70p ps=27u
M1003 p A_bar v0 vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.12n ps=46u
M1004 B_bar B gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=60p ps=32u
M1005 v0 A_bar a_24_6# Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=60p ps=26u
M1006 A_bar A gnd Gnd CMOSN w=10 l=2
+  ad=60p pd=32u as=50p ps=30u
M1007 a_7_6# A v0 Gnd CMOSN w=20 l=2
+  ad=70p pd=27u as=100p ps=50u
M1008 p B vdd vdd CMOSP w=40 l=2
+  ad=0.12n pd=46u as=0.14n ps=47u
M1009 a_24_6# B_bar gnd Gnd CMOSN w=20 l=2
+  ad=60p pd=26u as=60p ps=26u
M1010 vdd A p vdd CMOSP w=40 l=2
+  ad=0.14n pd=47u as=0.2n ps=90u
M1011 v0 B_bar p vdd CMOSP w=40 l=2
+  ad=0.12n pd=46u as=0.12n ps=46u
C0 B_bar A 0.22378f
C1 p A 0.00809f
C2 B A 0.33344f
C3 A_bar v0 0.01043f
C4 A_bar gnd 0
C5 B_bar v0 0.04128f
C6 B_bar gnd 0.00161f
C7 A_bar vdd 0.2091f
C8 p v0 0
C9 B_bar vdd 0.24622f
C10 B v0 0.0076f
C11 B gnd 0.00234f
C12 p vdd 0.03459f
C13 a_7_6# v0 0
C14 a_7_6# gnd 0
C15 v0 A 0.00768f
C16 gnd A 0.00161f
C17 B vdd 0.08517f
C18 A_bar B_bar 0.13899f
C19 v0 a_24_6# 0
C20 a_24_6# gnd 0
C21 A_bar p 0.00825f
C22 A vdd 0.09276f
C23 B A_bar 0.03102f
C24 B_bar p 0.39035f
C25 v0 gnd 0
C26 B B_bar 0.15433f
C27 A_bar A 0.2192f
C28 B p 0.00825f
C29 v0 vdd 0.07817f
C30 gnd 0 0.38381f
C31 v0 0 0.16434f
C32 p 0 0.11038f
C33 B_bar 0 0.30773f
C34 A_bar 0 0.55832f
C35 B 0 1.07492f
C36 A 0 0.58702f
C37 vdd 0 6.11095f

.tran 1n 80n

.control
set hcopypscolor = 0 *White background for saving plots
set color0=black
set color1=white
run

plot v0+4 B+2 A

.endc
.end
```



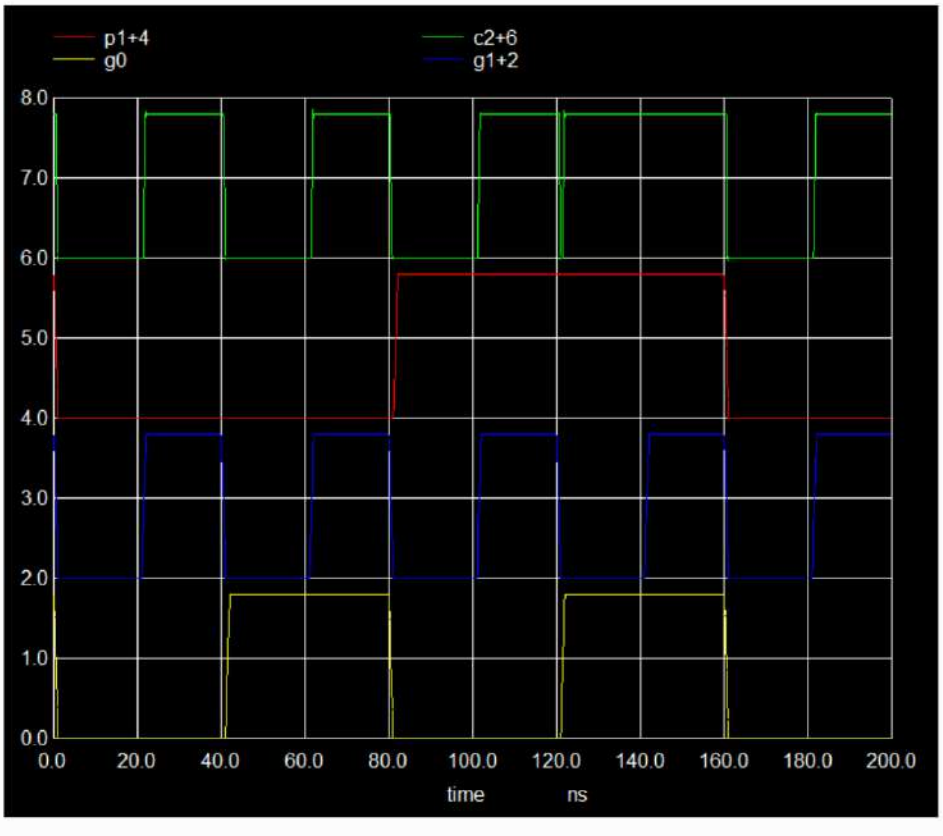


(8) Lavoy 2 :-

```
.include TSMC_180nm.txt

.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd


.option scale=90n


VG1 G1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
Vdd vdd gnd 'SUPPLY'

M1000 a_n15_0# P1 vdd vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.16n ps=48u
M1001 C2 C2_bar gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1002 C2_bar G1 a_n15_0# vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1003 C2_bar P1 a_n8_n34# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=80p ps=28u
M1004 a_n8_n34# G0 gnd Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1005 vdd G0 a_n15_0# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1006 C2 C2_bar vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1007 gnd G1 C2_bar Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
C0 C2_bar G1 0.01018f
C1 gnd C2 0
C2 C2 vdd 0.01479f
C3 vdd a_n15_0# 0.0272f
C4 P1 a_n15_0# 0.008f
C5 C2_bar C2 0.0587f
C6 G0 a_n15_0# 0.00784f
C7 gnd P1 0
C8 P1 vdd 0.05212f
C9 C2_bar a_n15_0# 0.11547f
C10 G1 a_n15_0# 0.00153f
C11 gnd G0 0.00161f
C12 G0 vdd 0.05214f
C13 gnd a_n8_n34# 0
C14 P1 G0 0.05635f
C15 C2_bar gnd 0.00112f
C16 gnd G1 0.00161f
C17 C2_bar vdd 0.05648f
C18 G1 vdd 0.05053f
C19 C2_bar P1 0.00153f
C20 P1 G1 0.05635f
C21 gnd 0 0.18635f
C22 C2 0 0.07523f
C23 C2_bar 0 0.24995f
C24 a_n15_0# 0 0.06039f
C25 G1 0 0.18806f
C26 P1 0 0.1783f
C27 G0 0 0.18806f
C28 vdd 0 4.281f
```

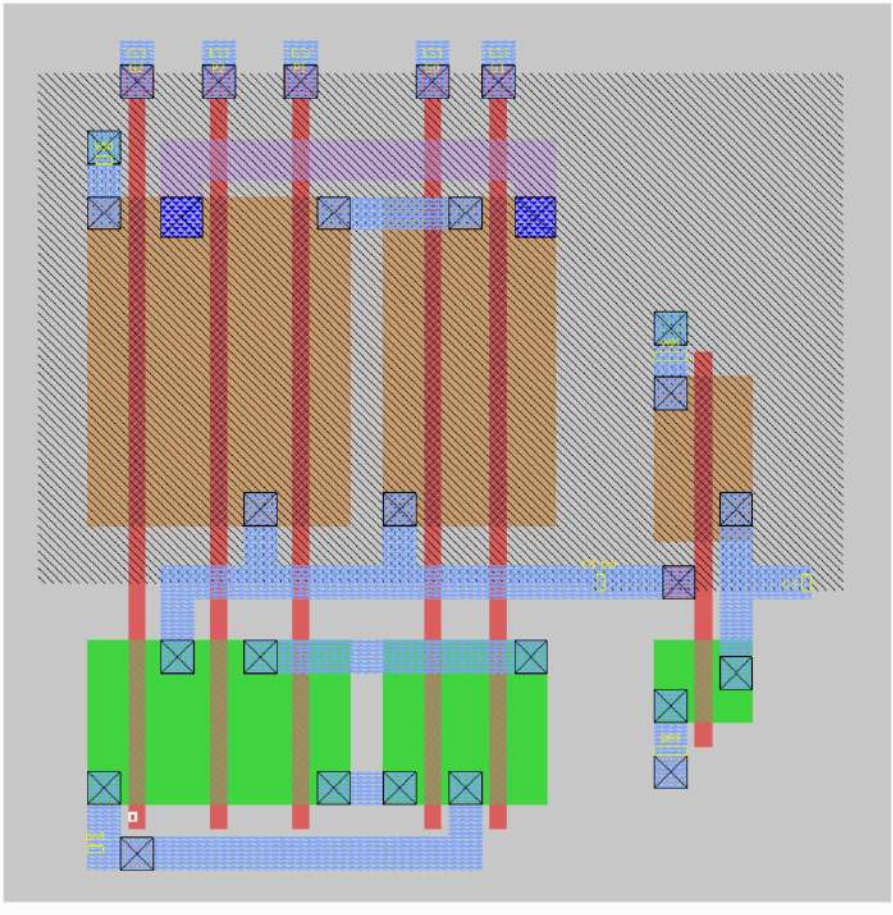


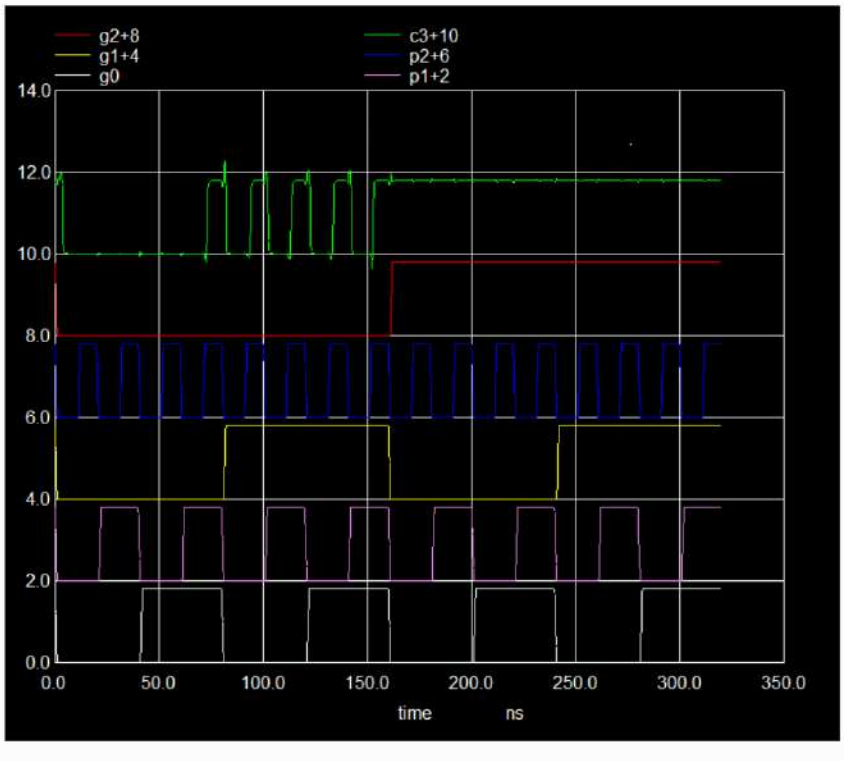
```
.tran 1n 200n

.control
set hcopypscolor = 0
set color0=black
set color1=white
run
plot C2+6 P1+4 G1+2 G0

.endc
.end
```



⑥ Carry 3 :-

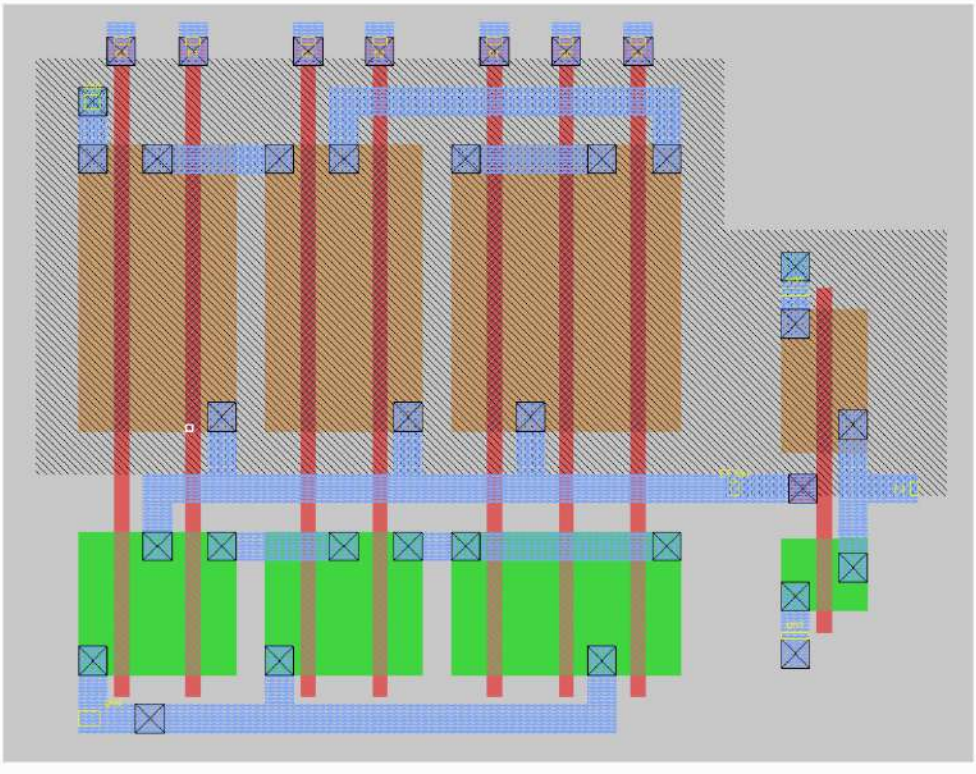
```
.include TSMC_180nm.txt

.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

.option scale=90n


VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
Vdd vdd gnd 'SUPPLY'



M1000 a_22_2# P1 a_12_2# Gnd CMOSN w=180 l=18
+  ad=8.1n pd=0.45m as=6.48n ps=0.252m
M1001 C3 C3_bar vdd vdd CMOSP w=180 l=18
+  ad=8.1n pd=0.45m as=8.1n ps=0.45m
M1002 a_12_2# P2 C3_bar Gnd CMOSN w=180 l=18
+  ad=6.48n pd=0.252m as=6.48n ps=0.252m
M1003 gnd G0 a_22_2# Gnd CMOSN w=180 l=18
+  ad=4.86n pd=0.234m as=8.1n ps=0.45m
M1004 C3_bar P2 a_2_36# vdd CMOSP w=360 l=18
+  ad=12.96n pd=0.432m as=12.96n ps=0.432m
M1005 a_22_36# G0 C3_bar vdd CMOSP w=360 l=18
+  ad=9.72n pd=0.414m as=16.2n ps=0.81m
M1006 a_22_36# P1 C3_bar vdd CMOSP w=360 l=18
+  ad=16.2n pd=0.81m as=12.96n ps=0.432m
M1007 a_2_36# G2 vdd vdd CMOSP w=360 l=18
+  ad=12.96n pd=0.432m as=16.2n ps=0.81m
M1008 a_2_36# G1 a_22_36# vdd CMOSP w=360 l=18
+  ad=19.44n pd=0.828m as=9.72n ps=0.414m
M1009 a_12_2# G1 gnd Gnd CMOSN w=180 l=18
+  ad=8.1n pd=0.45m as=4.86n ps=0.234m
M1010 C3_bar G2 gnd Gnd CMOSN w=180 l=18
+  ad=6.48n pd=0.252m as=8.1n ps=0.45m
M1011 C3 C3_bar gnd Gnd CMOSN w=90 l=18
+  ad=4.05n pd=0.27m as=4.05n ps=0.27m
C0 vdd 0 6.19353f

.tran 1n 320n

.control
set hcopypscolor = 0
set color0=black
set color1=white
run

plot C3+10 G2+8 P2+6 G1+4 P1+2 G0

.endc
.end
```

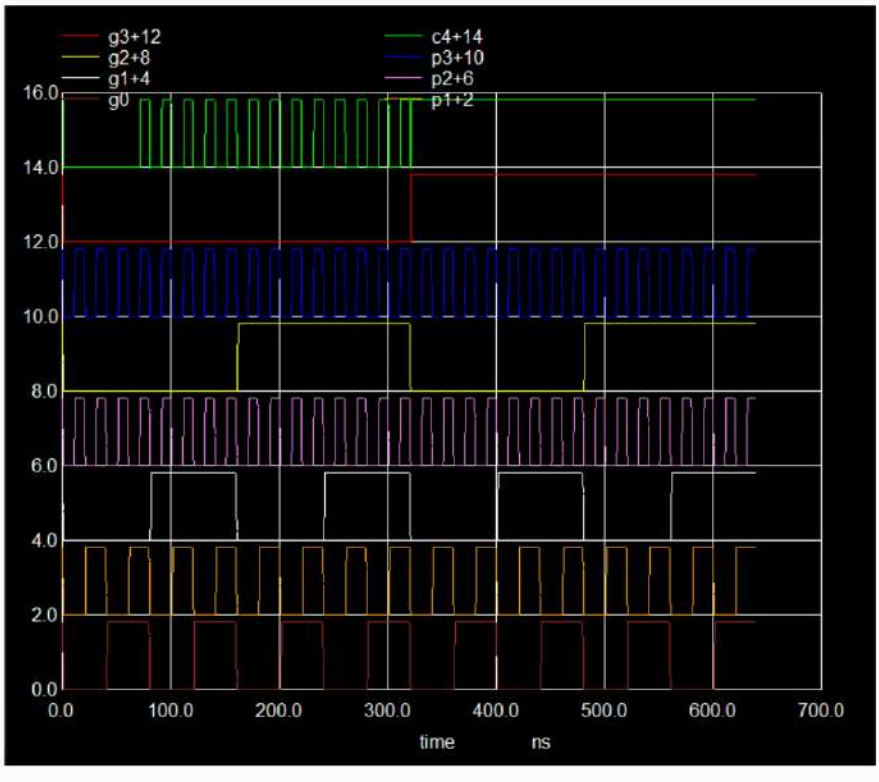




(d) Carry 4 :-

```
.include TSMC_180nm.txt

.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd
.option scale=90n

VP3 P3 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
VG3 G3 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
Vdd vdd gnd 'SUPPLY'

M1000 a_2_n34# G2 gnd Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1001 a_28_n34# G1 gnd Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
M1002 C4_bar P3 a_n8_0# vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1003 C4 C4_bar gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1004 gnd G0 a_44_n34# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=80p ps=28u
M1005 C4_bar P2 a_18_0# vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1006 a_2_n34# P3 C4_bar Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
M1007 a_18_0# G2 a_n8_0# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1008 a_44_n34# P1 a_28_n34# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1009 a_18_0# G1 a_37_0# vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1010 C4 C4_bar vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1011 C4_bar G3 gnd Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1012 a_37_0# G0 C4_bar vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.16n ps=48u
M1013 C4_bar P1 a_37_0# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1014 a_n8_0# G3 vdd vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1015 a_28_n34# P2 a_2_n34# Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
C0 vdd 0 6.80421f


.tran 1n 640n

.control
set hcopypscolor = 0
set color0=black
set color1=white
run
plot C4+14 G3+12 P3+10 G2+8 P2+6 G1+4 P1+2 G0
.endc
.end
```

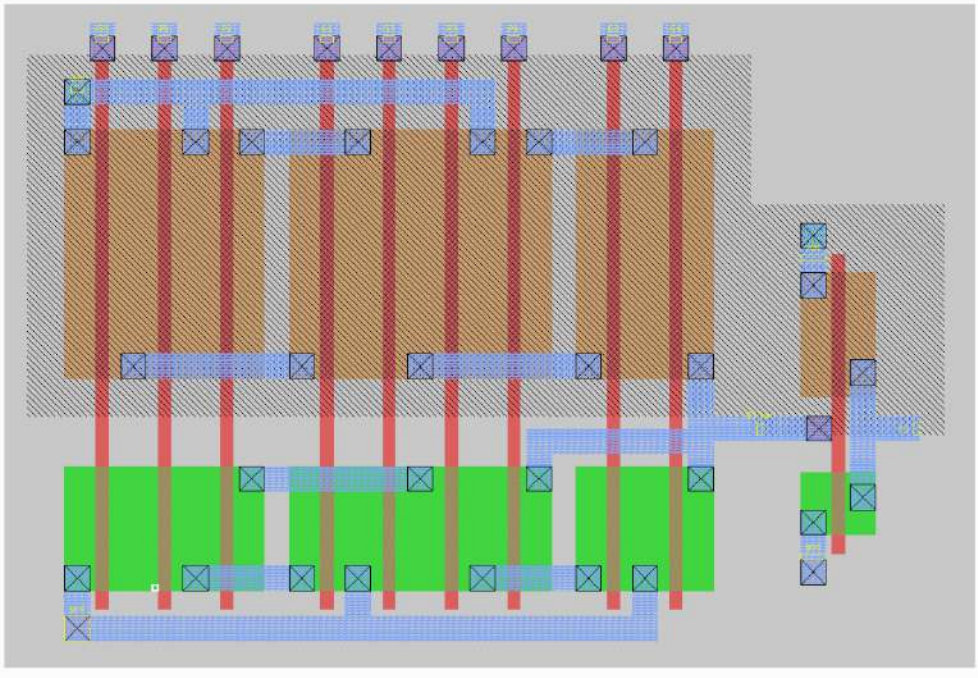


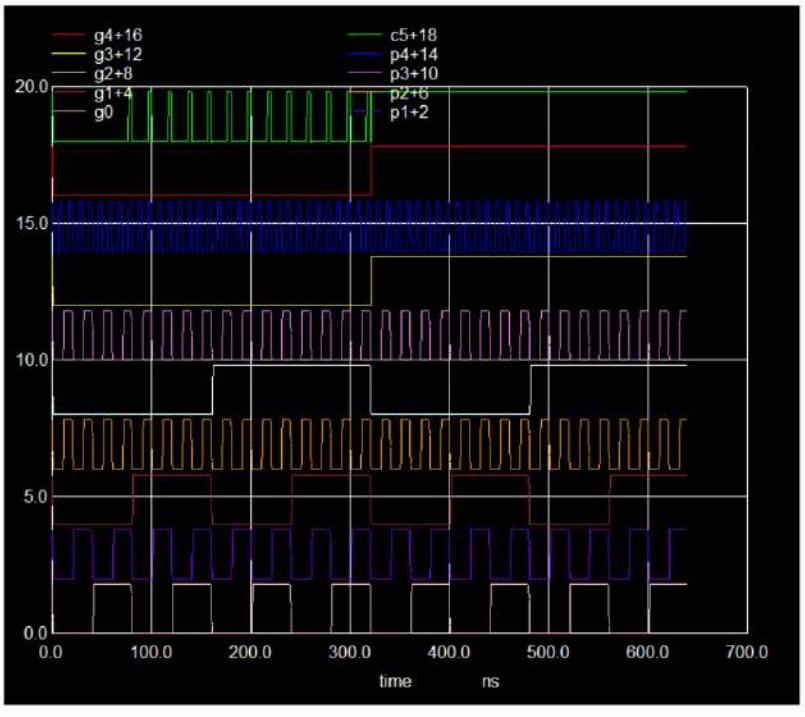


Carry5:-

```
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd
.option scale=90n

VP4 P4 gnd PULSE(1.8 0 0 1n 1n 5n 10n)
VP3 P3 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP2 P2 gnd PULSE(1.8 0 0 1n 1n 10n 20n)
VP1 P1 gnd PULSE(1.8 0 0 1n 1n 20n 40n)
VG0 G0 gnd PULSE(1.8 0 0 1n 1n 40n 80n)
VG1 G1 gnd PULSE(1.8 0 0 1n 1n 80n 160n)
VG2 G2 gnd PULSE(1.8 0 0 1n 1n 160n 320n)
VG3 G3 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
VG4 G4 gnd PULSE(1.8 0 0 1n 1n 320n 640n)
Vdd vdd gnd 'SUPPLY'

M1000 a_n7_0# G0 gnd Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1001 a_13_0# P2 a_3_0# Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
M1002 C5_bar P4 a_49_0# Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
M1003 a_49_0# P3 a_13_0# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=80p ps=28u
M1004 a_13_0# G2 gnd Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=80p ps=28u
M1005 gnd G1 a_3_0# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1006 C5_bar G4 gnd Gnd CMOSN w=20 l=2
+  ad=100p pd=50u as=80p ps=28u
M1007 gnd G3 a_49_0# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=100p ps=50u
M1008 a_13_34# G1 a_n7_34# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1009 C5 C5_bar vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1010 C5 C5_bar gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1011 a_13_34# P2 vdd vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1012 a_59_34# G3 a_39_34# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1013 a_n7_34# G0 vdd vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.2n ps=90u
M1014 a_39_34# G2 a_13_34# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.16n ps=48u
M1015 C5_bar G4 a_59_34# vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
M1016 vdd P1 a_n7_34# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.16n ps=48u
M1017 vdd P3 a_39_34# vdd CMOSP w=40 l=2
+  ad=0.16n pd=48u as=0.16n ps=48u
M1018 a_3_0# P1 a_n7_0# Gnd CMOSN w=20 l=2
+  ad=80p pd=28u as=80p ps=28u
M1019 a_59_34# P4 vdd vdd CMOSP w=40 l=2
+  ad=0.2n pd=90u as=0.16n ps=48u
C0 vdd 0 8.07907f
```

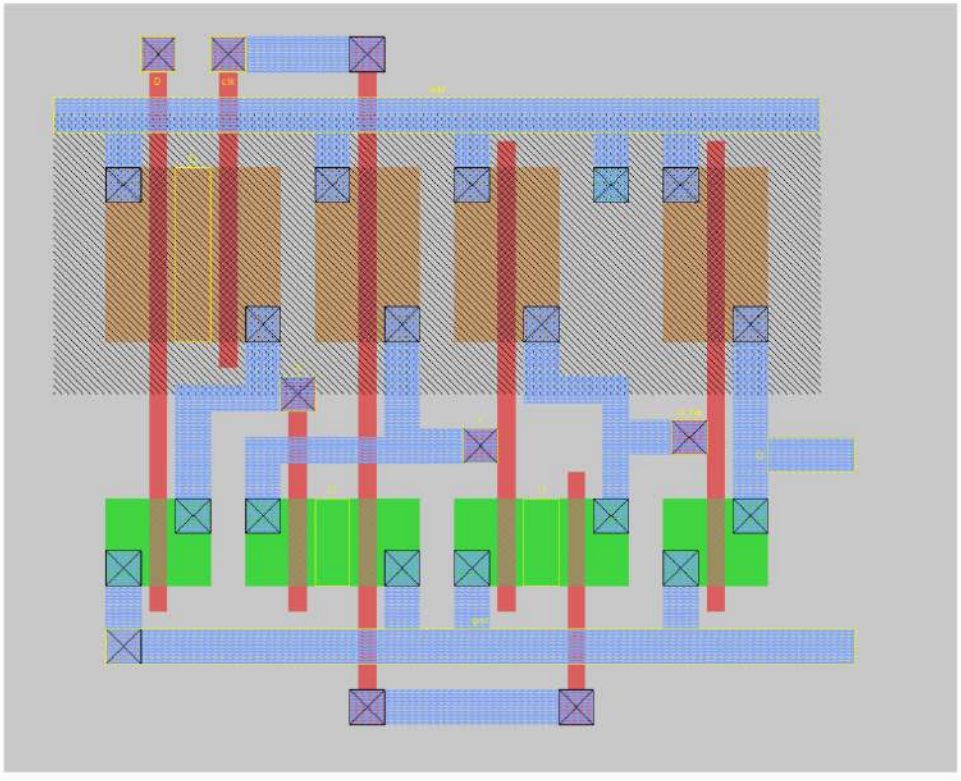
```
.tran 1n 640n

.control
set hcopypscolor = 0
set color0=black
set color1=white
run

plot C5+18 G4+16 P4+14 G3+12 P3+10 G2+8 P2+6 G1+4 P1+2 G0

.endc
.end
```



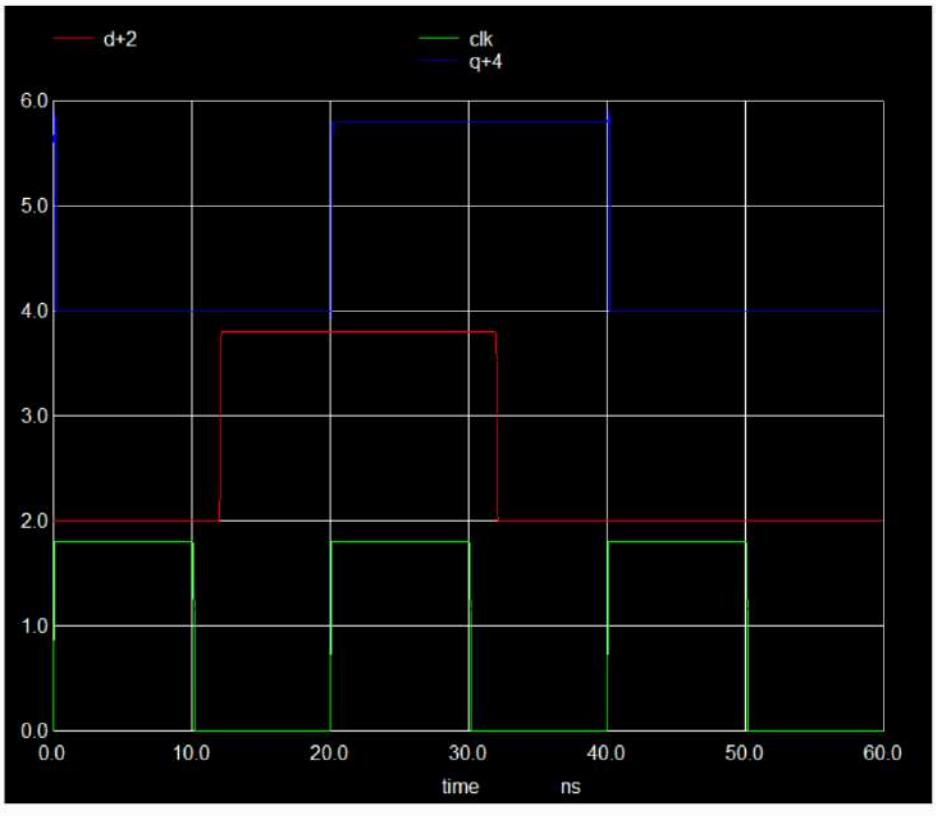


DFF :-

```
.include TSMC_180nm.txt
.global vdd gnd
.option scale=90n
Vdd vdd 0 1.8
Vclk clk 0 pulse(0 1.8 0 100p 100p 10n 20n)
Vdata D 0 pwl(0 0 12n 0 12.1n 1.8 32n 1.8 32.1n 0 60n 0)
M1000 l1 D vdd vdd CMOSP w=20 l=2
+  ad=60p pd=26u as=100p ps=50u
M1001 Q_bar clk l3 Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=30p ps=16u
M1002 l2 X Y Gnd CMOSN w=10 l=2
+  ad=30p pd=16u as=50p ps=30u
M1003 X clk l1 vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=60p ps=26u
M1004 Q Q_bar vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1005 l3 Y gnd Gnd CMOSN w=10 l=2
+  ad=30p pd=16u as=50p ps=30u
M1006 X D gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1007 Y clk vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1008 Q Q_bar gnd Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=50p ps=30u
M1009 Q_bar Y vdd vdd CMOSP w=20 l=2
+  ad=100p pd=50u as=100p ps=50u
M1010 gnd clk l2 Gnd CMOSN w=10 l=2
+  ad=50p pd=30u as=30p ps=16u
C0 clk Y 0.03159f
C1 l2 Y 0
C2 vdd X 0.01725f
C3 clk Q_bar 0
C4 D clk 0.11678f
C5 vdd Y 0.0286f
C6 vdd Q_bar 0.03386f
C7 vdd D 0.08759f
C8 vdd l1 0
C9 vdd clk 0.33388f
C10 Q gnd 0
C11 X gnd 0
C12 Y gnd 0.00175f
C13 Q_bar Q 0.05983f
C14 l3 gnd 0
C15 Y X 0.22972f
C16 Q_bar gnd 0.00164f
C17 D gnd 0.00153f
C18 D X 0.00351f
C19 l1 X 0
C20 clk gnd 0.40146f
C21 Y Q_bar 0.00206f
C22 l2 gnd 0
C23 clk X 0.06868f
C24 vdd Q 0.00806f
C25 gnd 0 0.32996f
C26 Q 0 0.10349f
C27 X 0 0.17941f
C28 Q_bar 0 0.28741f
C29 Y 0 0.28701f
C30 clk 0 0.59967f
C31 D 0 0.20166f
C32 vdd 0 3.10879f
```



```
.tran 0.01n 60n
.measure tran tcpq
+ TRIG v(clk) VAL=0.9 RISE=2
+ TARG v(Q) VAL=0.9 RISE=1

.measure tran tsetup
+ TRIG v(D) VAL=0.9 RISE=1
+ TARG v(X) VAL=0.9 FALL=1

.measure tran thold
+ TRIG v(Y) VAL=0.9 FALL=1
+ TARG v(X) VAL=0.9 RISE=1

.control
run
plot clk D+2 Q+4
.endc

.end
```




```
tcpq                =  6.390828e-11 targ=  2.011391e-08 trig=  2.005000e-08
tsetup              =  3.045591e-11 targ=  1.208046e-08 trig=  1.205000e-08
```

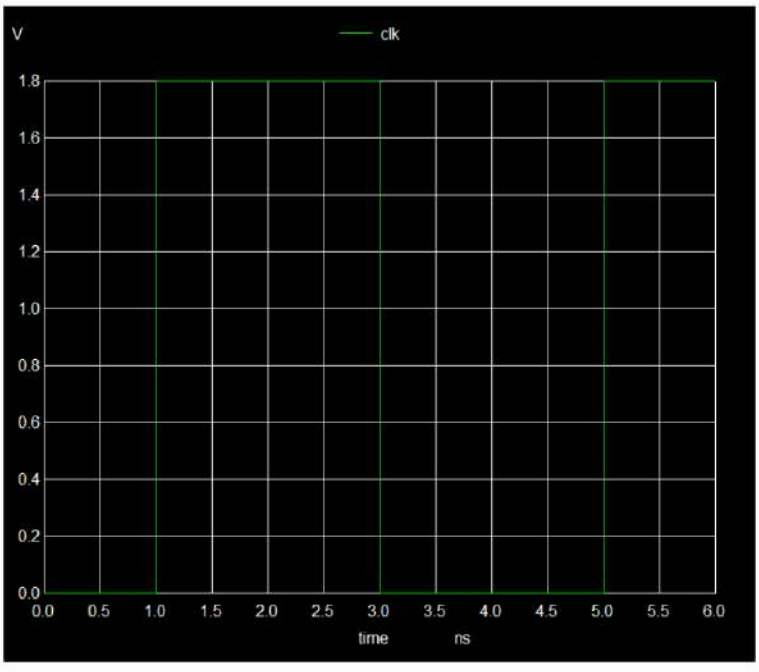
we observe slight more delay due to Capacitors in POST Layout

Q7

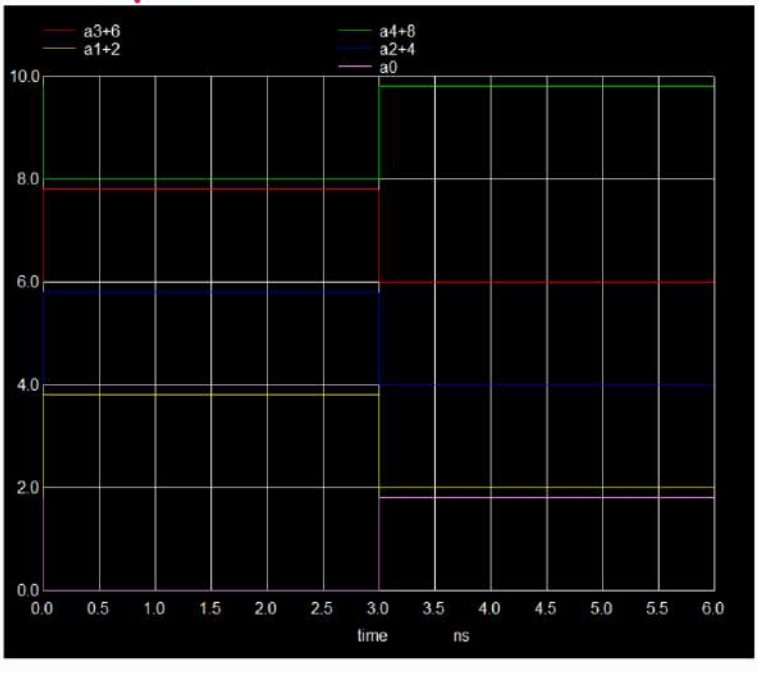
```
.include TSMC_180nm.txt
.include INV.sp
.include AND.sp
.include XOR.sp
.include CARRY2.sp
.include CARRY3.sp
.include CARRY4.sp
.include CARRY5.sp
.include DFF.sp

.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd



VA4 A4 gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VA3 A3 gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA2 A2 gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA1 A1 gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA0 A0 gnd PULSE(1.8 0 0 1p 1p 3n 6n)

VB4 B4 gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VB3 B3 gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB2 B2 gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB1 B1 gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB0 B0 gnd PULSE(1.8 0 0 1p 1p 3n 6n)

Vdd vdd gnd 'SUPPLY'


VCLK CLK gnd PULSE(0 1.8 1n 1p 1p 2n 4n)



X_DFF_A0 A0_reg A0 CLK vdd gnd d_flop
X_DFF_A1 A1_reg A1 CLK vdd gnd d_flop
X_DFF_A2 A2_reg A2 CLK vdd gnd d_flop
X_DFF_A3 A3_reg A3 CLK vdd gnd d_flop
X_DFF_A4 A4_reg A4 CLK vdd gnd d_flop
* Input B registers
X_DFF_B0 B0_reg B0 CLK vdd gnd d_flop
X_DFF_B1 B1_reg B1 CLK vdd gnd d_flop
X_DFF_B2 B2_reg B2 CLK vdd gnd d_flop
X_DFF_B3 B3_reg B3 CLK vdd gnd d_flop
X_DFF_B4 B4_reg B4 CLK vdd gnd d_flop



x_S0 S0 A0_reg B0_reg vdd gnd xor2
x_G0 G0 A0_reg B0_reg vdd gnd and2



X_P1 P1 A1_reg B1_reg vdd gnd xor2
X_G1 G1 A1_reg B1_reg vdd gnd and2
X_S1 S1 G0 P1 vdd gnd xor2
X_C2 C2 G1 P1 G0 vdd gnd carry2
```

```
X_P2 P2 A2_reg B2_reg vdd gnd xor2
X_G2 G2 A2_reg B2_reg vdd gnd and2
X_S2 S2 C2 P2 vdd gnd xor2
X_C3 C3 G2 P2 G1 P1 G0 vdd gnd carry3


X_P3 P3 A3_reg B3_reg vdd gnd xor2
X_G3 G3 A3_reg B3_reg vdd gnd and2
X_S3 S3 C3 P3 vdd gnd xor2
X_C4 C4 G3 P3 G2 P2 G1 P1 G0 vdd gnd carry4


X_P4 P4 A4_reg B4_reg vdd gnd xor2
X_G4 G4 A4_reg B4_reg vdd gnd and2
X_S4 S4 C4 P4 vdd gnd xor2
X_C5 C5 G4 P4 G3 P3 G2 P2 G1 P1 G0 vdd gnd carry5



X_DFF_S0 Sum_out0 S0 CLK vdd gnd d_flop
X_DFF_S1 Sum_out1 S1 CLK vdd gnd d_flop
X_DFF_S2 Sum_out2 S2 CLK vdd gnd d_flop
X_DFF_S3 Sum_out3 S3 CLK vdd gnd d_flop
X_DFF_S4 Sum_out4 S4 CLK vdd gnd d_flop
X_DFF_C5 Cout_out C5 CLK vdd gnd d_flop



.tran 1p 6n
.measure tran t1
+ TRIG v(CLK) VAL=0.9 RISE=1
+ TARG v(S4) VAL=0.9 RISE=1

.measure tran t2
+ TRIG v(CLK) VAL=0.9 RISE=2
+ TARG v(S4) VAL=0.9 FALL=2

.measure tran t3
+ TRIG v(CLK) VAL=0.9 RISE=2
+ TARG v(C4) VAL=0.9 RISE=1

.control
set hcopypscolor = 0
set color0=black
set color1=white
run


plot CLK

plot A4+8 A3+6 A2+4 A1+2 A0
plot B4+8 B3+6 B2+4 B1+2 B0


plot A4_reg+8 A3_reg+6 A2_reg+4 A1_reg+2 A0_reg
plot B4_reg+8 B3_reg+6 B2_reg+4 B1_reg+2 B0_reg


plot C5
plot S4+8 S3+6 S2+4 S1+2 S0

plot Cout_out
plot Sum_out4+8 Sum_out3+6 Sum_out2+4 Sum_out1+2 Sum_out0

.endc
.end
```

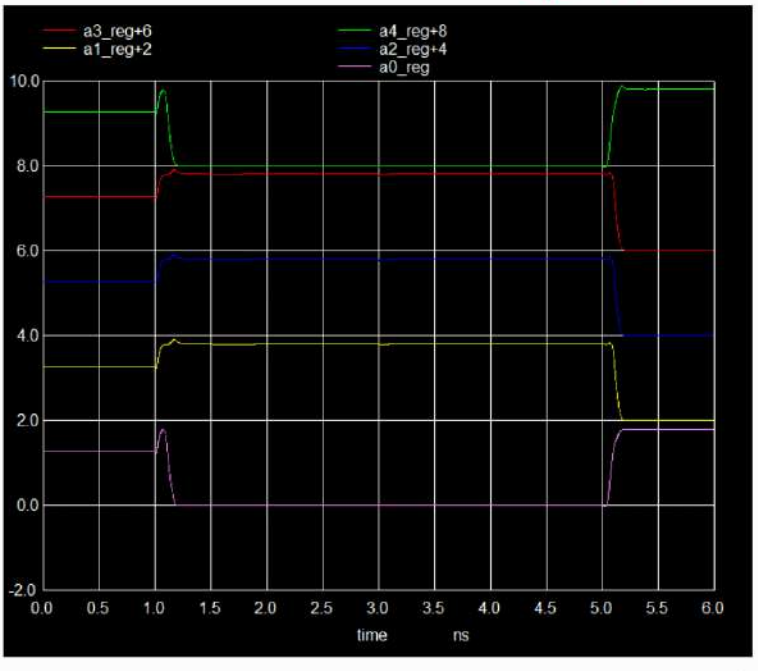
```
t1                     =   5.442689e-10 targ=   1.544769e-09 trig=   1.000500e-09
t2                     =   3.990934e-10 targ=   5.399593e-09 trig=   5.000500e-09
t3                     =   3.559267e-10 targ=   5.356427e-09 trig=   5.000500e-09
```

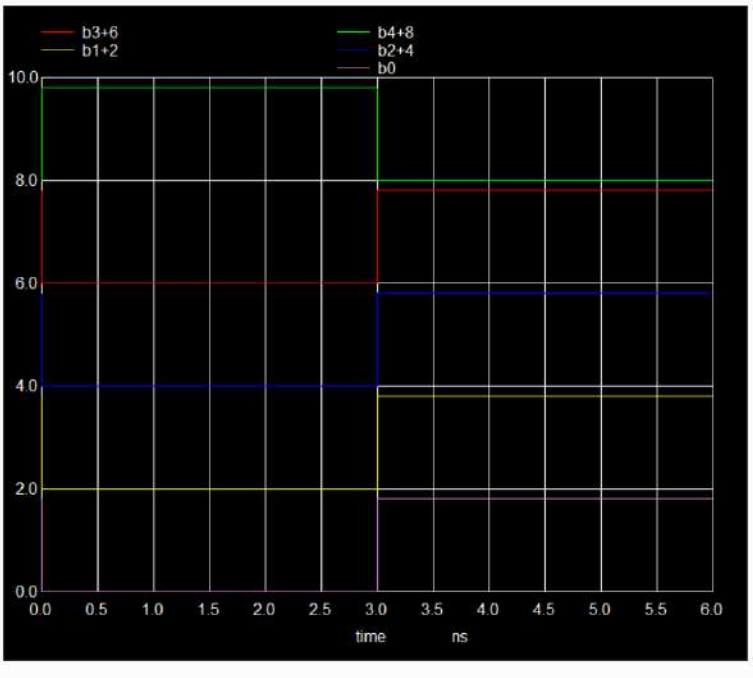


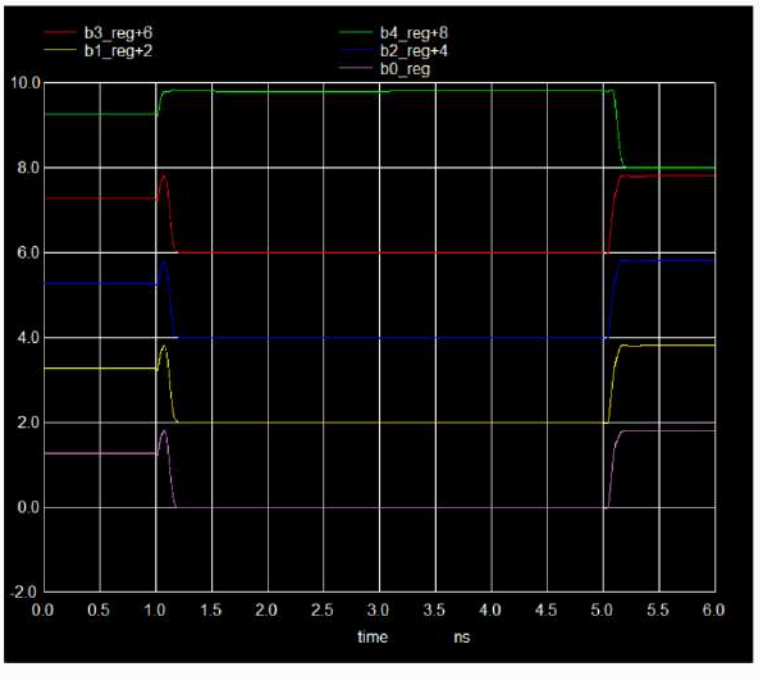
Input



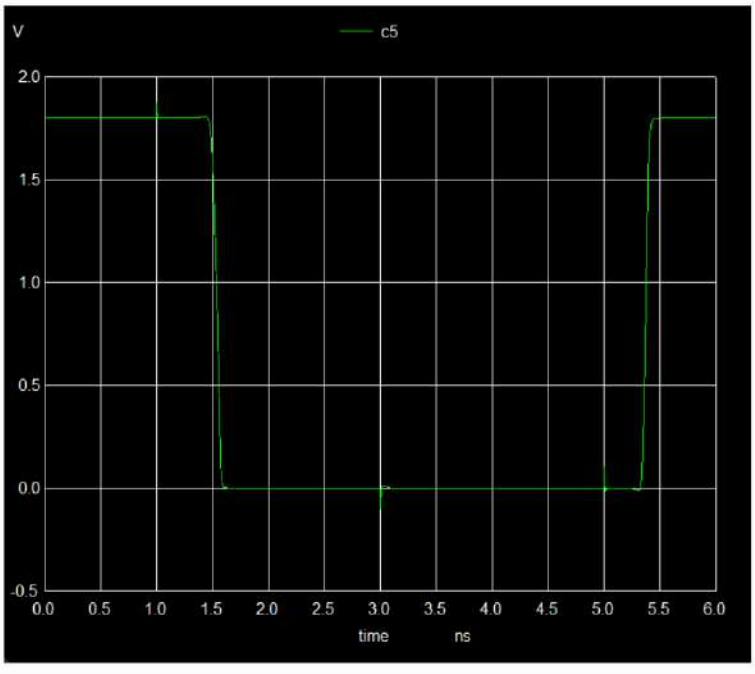
After FF

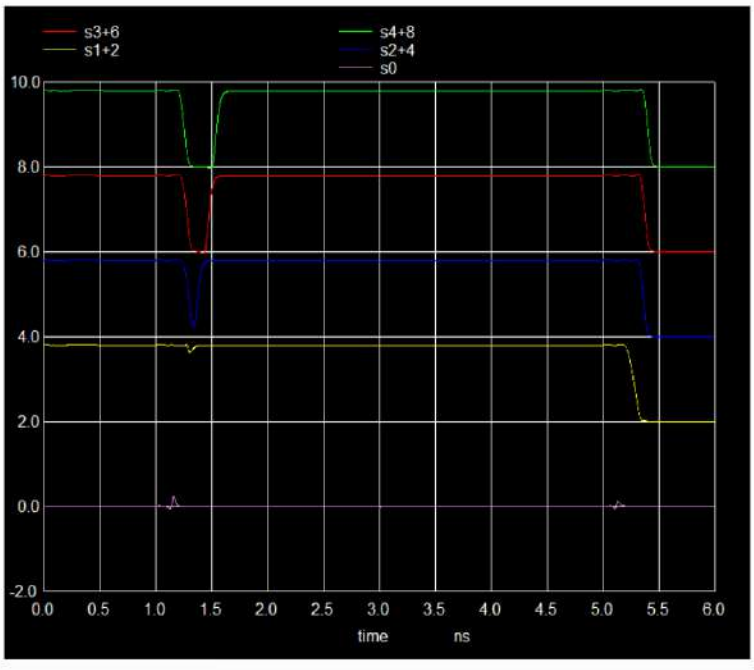




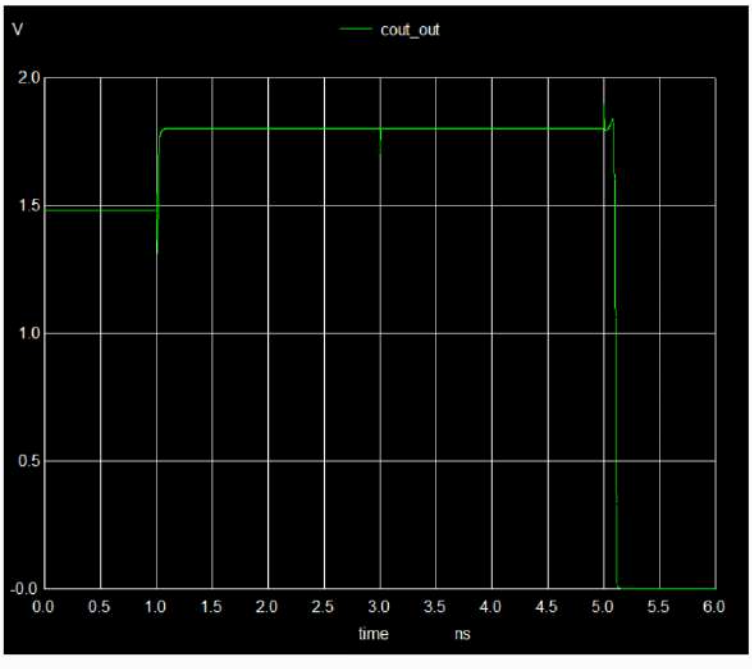


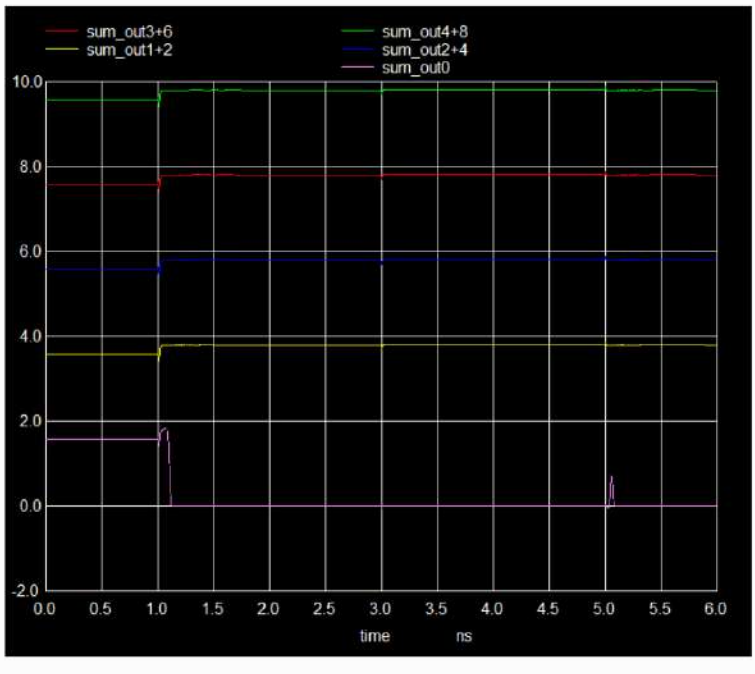
After CLA





After PP





⇒ the, worst case delay is 0.544 ns.

and we have Setup time as 0.0417 ns

So, $T_{clk} \geq 0.544 + 0.0417 =$

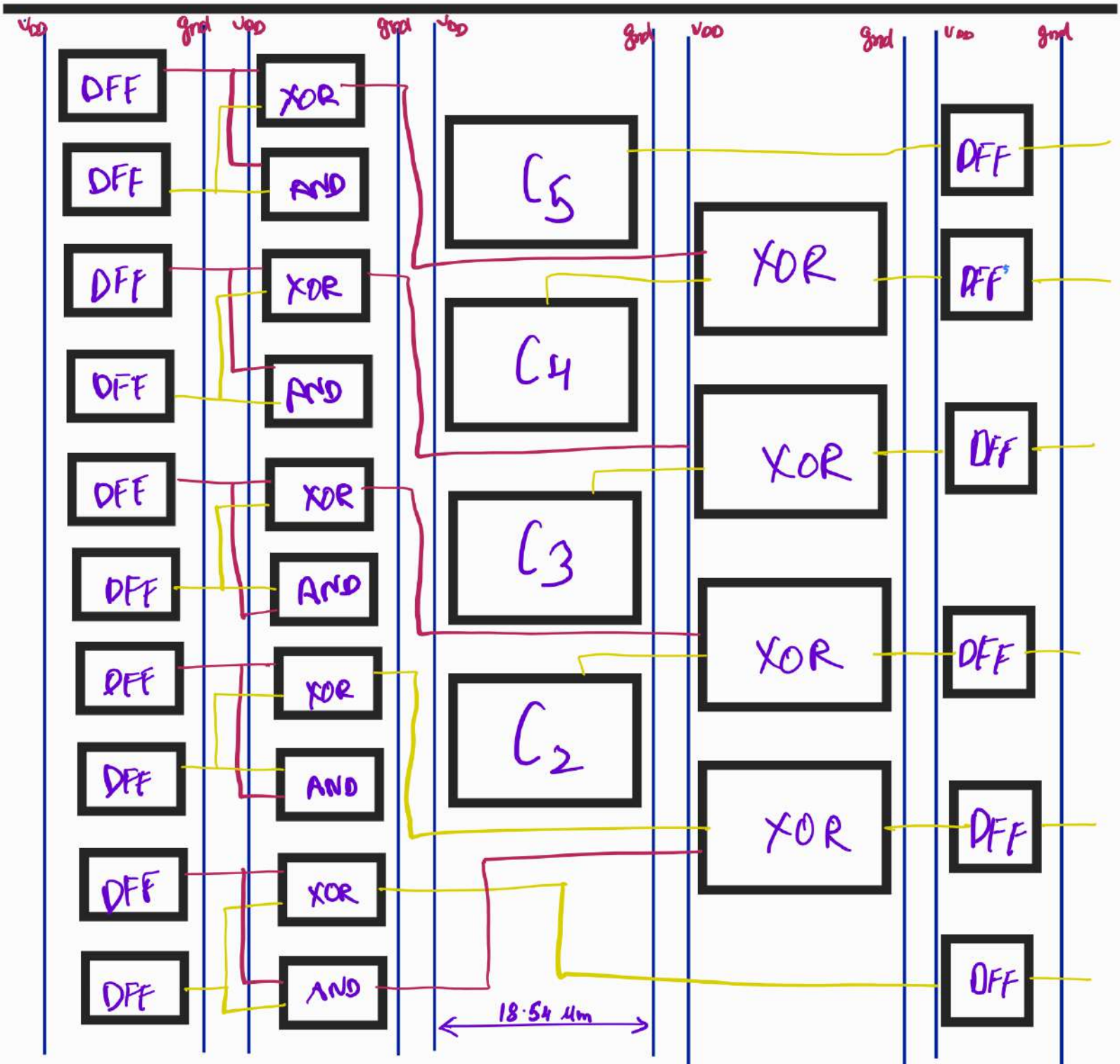
$T_{clk} \geq 0.5857$ ns

$f \leq 1.707$ GHz

So, max clock frequency is 1.7 GHz

08 —> All signals are placed as rails in a vertical lines, VDD & gnd rails are placed every alternate columns.

—> All vertical rails are metal 1, All horizontal connections are metal 2.



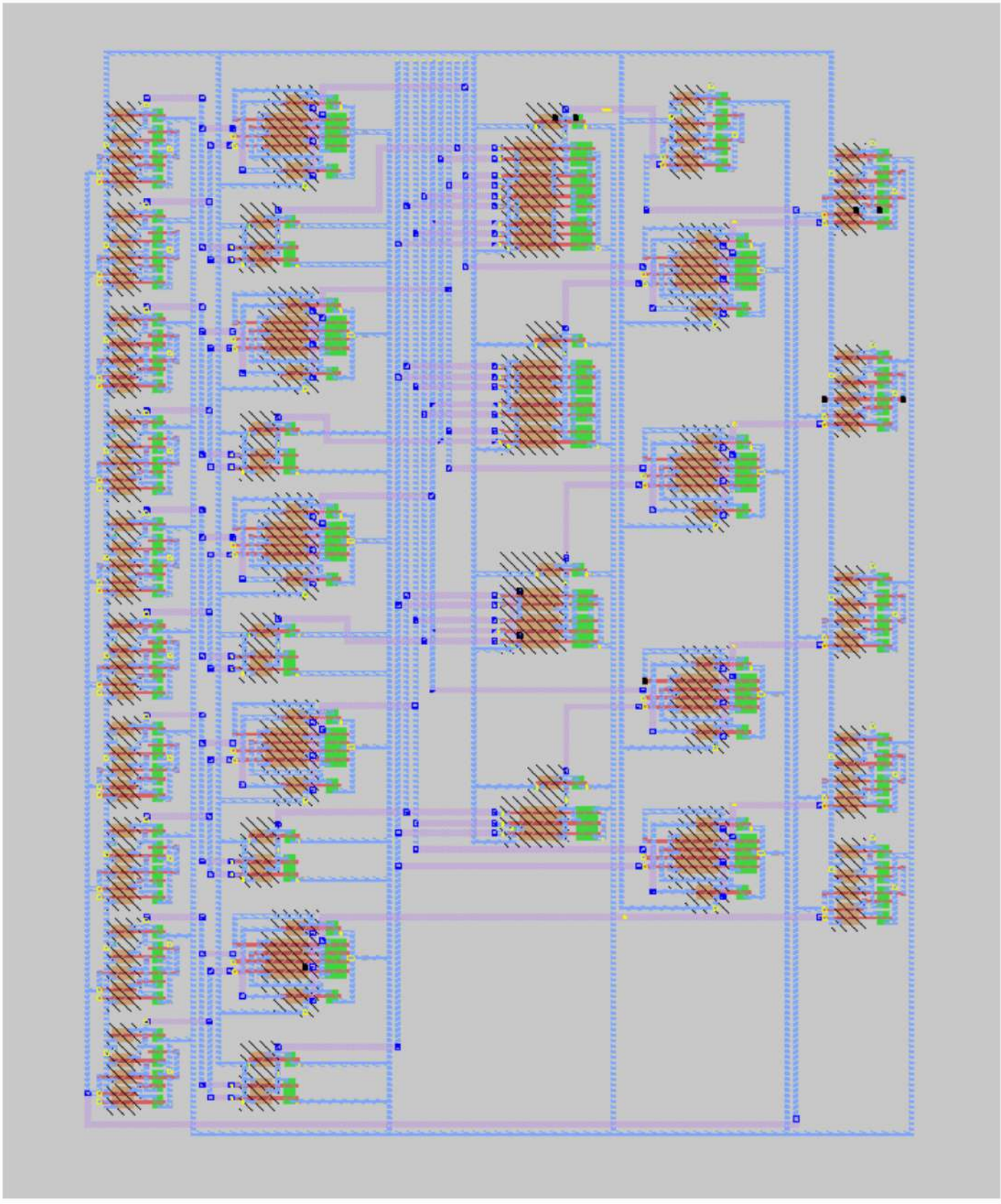
(*) the vertical pitch is distance b/w VDD to gnd Rail

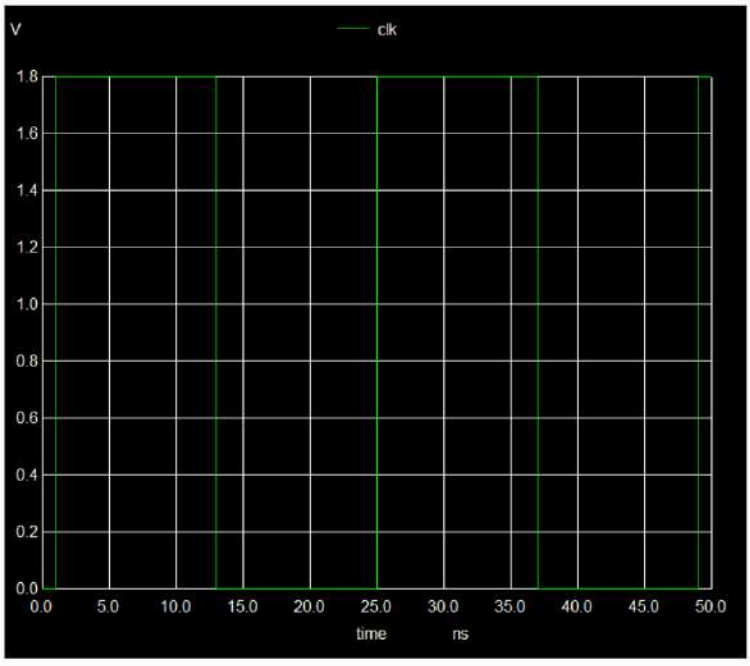
=> got 18.54 um

The Horizontal pitch is distance b/w two neighbouring gates

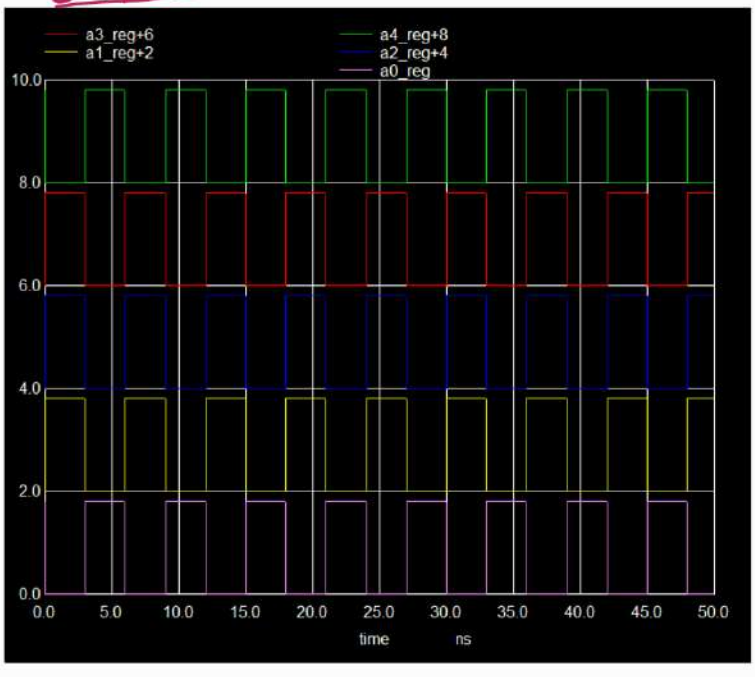
=> got 81 ($\lambda = 0.09$ um).

(89)

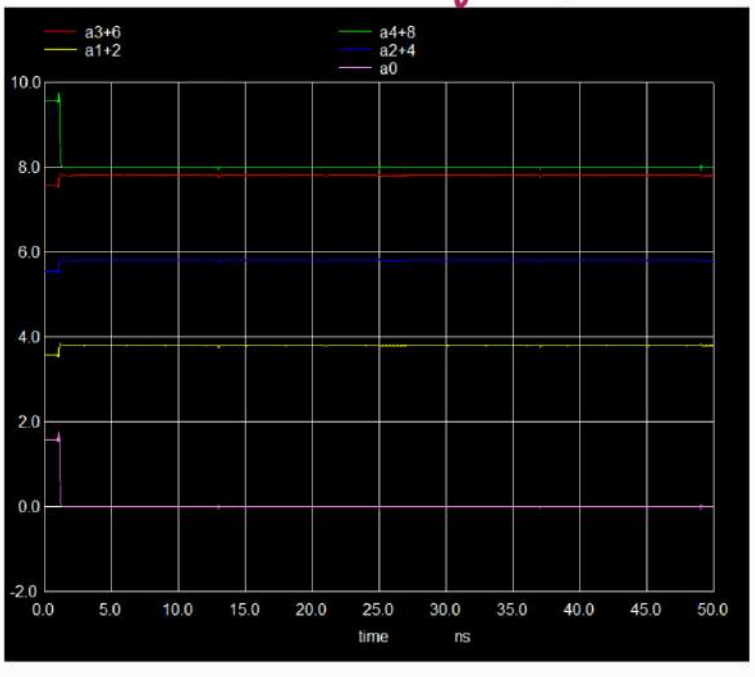


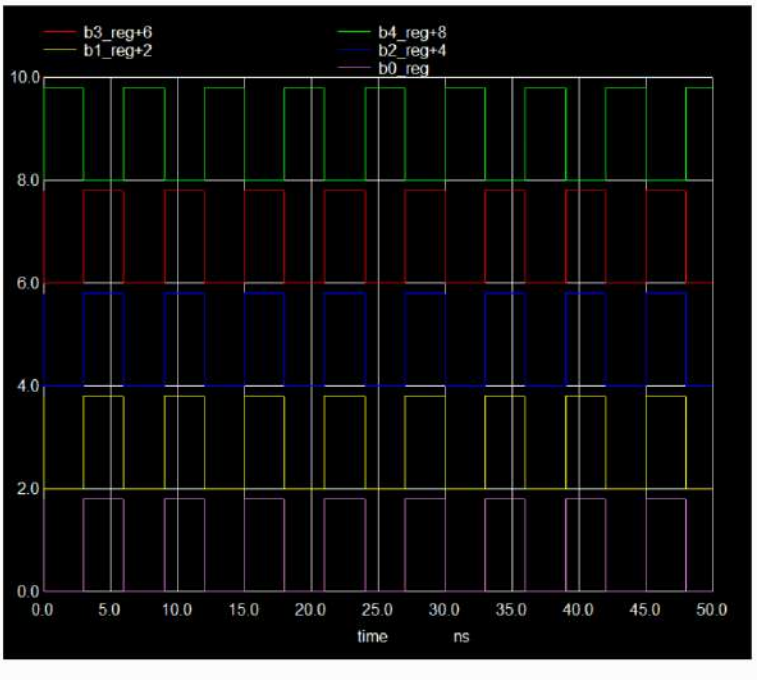


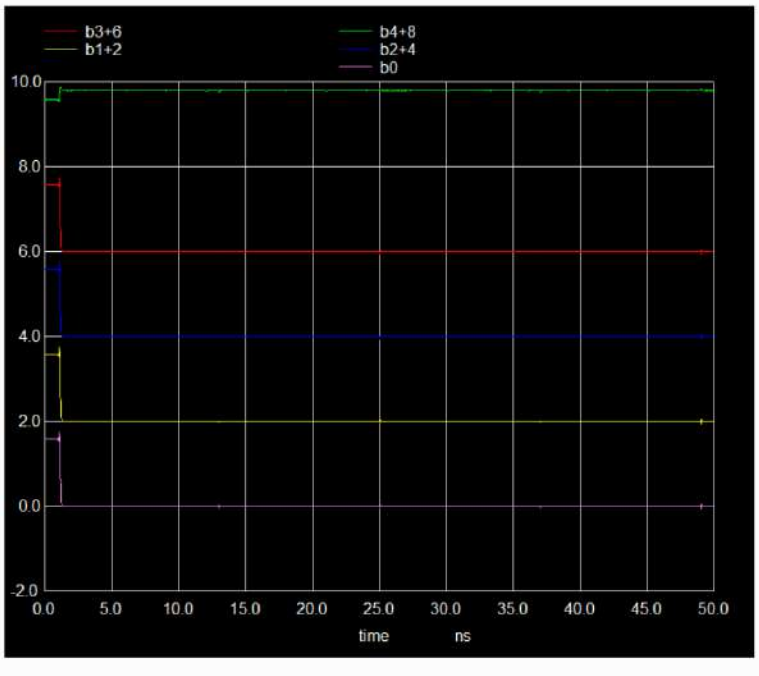
Input



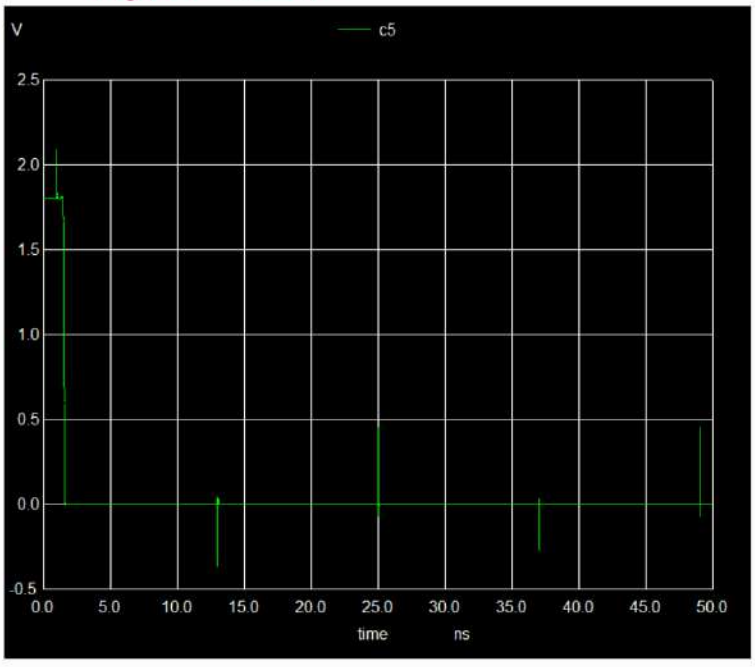
After FF

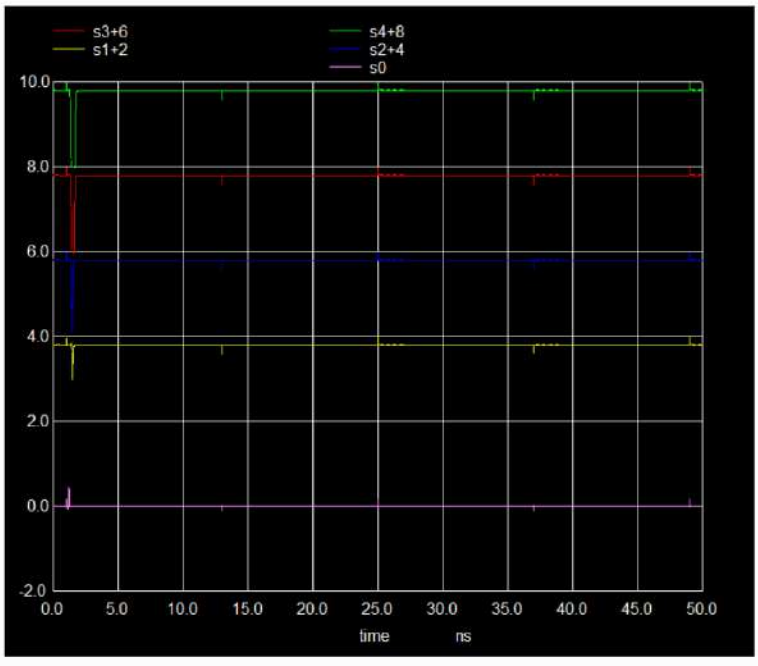




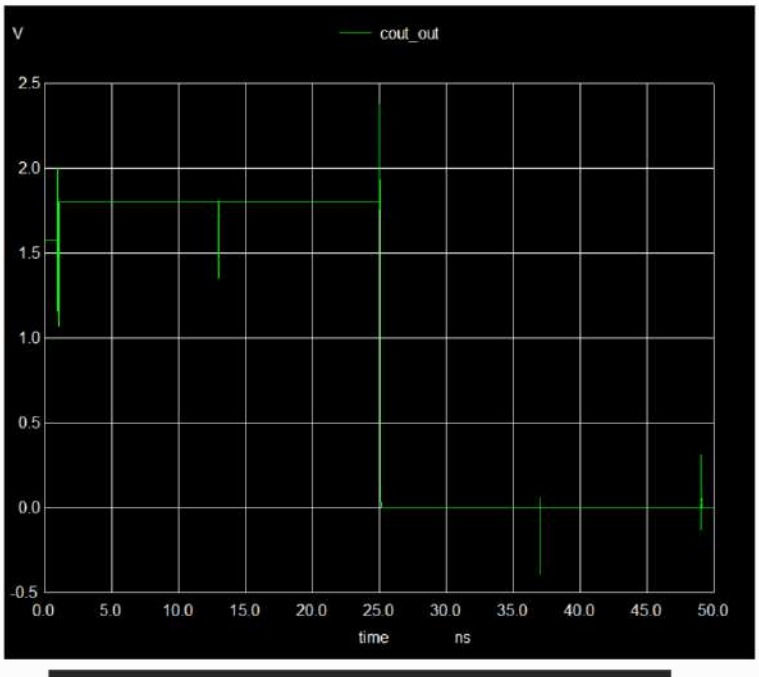


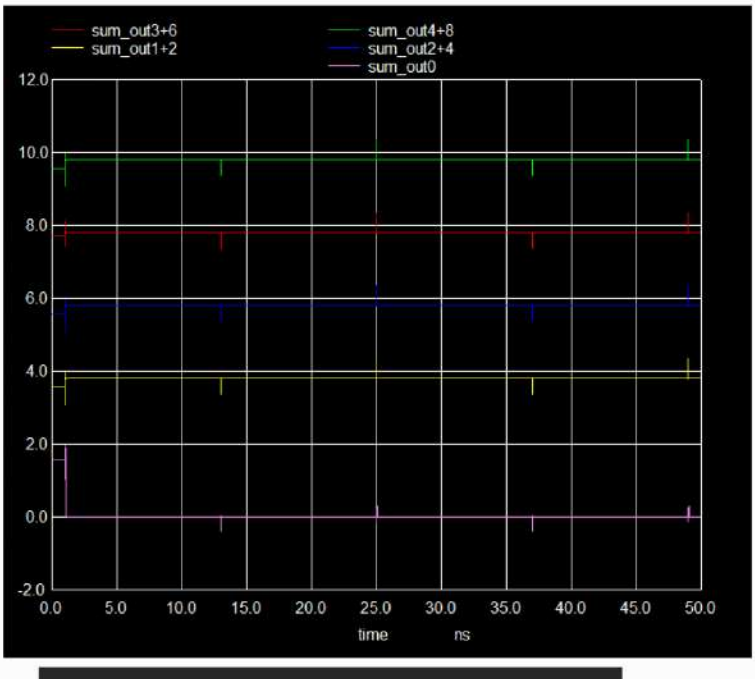
After CLA





After FF






```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd
.option scale=90n


VA4 A4_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VA3 A3_reg gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA2 A2_reg gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA1 A1_reg gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VA0 A0_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)

VB4 B4_reg gnd PULSE(0 1.8 0 1p 1p 3n 6n)
VB3 B3_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB2 B2_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB1 B1_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)
VB0 B0_reg gnd PULSE(1.8 0 0 1p 1p 3n 6n)

Vdd vdd gnd 'SUPPLY'


VCLK CLK gnd PULSE(0 1.8 1n 1p 1p 12n 24n)
```

```
.tran 10p 50n

.measure tran t1
+ TRIG v(CLK) VAL=0.9 RISE=1
+ TARG v(S4) VAL=0.9 RISE=1

.control
set hcopypscolor = 0
set color0=black
set color1=white
run

plot CLK


plot A4+8 A3+6 A2+4 A1+2 A0
plot B4+8 B3+6 B2+4 B1+2 B0


plot A4_reg+8 A3_reg+6 A2_reg+4 A1_reg+2 A0_reg
plot B4_reg+8 B3_reg+6 B2_reg+4 B1_reg+2 B0_reg


plot C5
plot S4+8 S3+6 S2+4 S1+2 S0


plot Cout_out
plot Sum_out4+8 Sum_out3+6 Sum_out2+4 Sum_out1+2 Sum_out0


.endc
.end
```

Q10

```
t1                    =  7.115171e-10 targ=  1.712017e-09 trig=  1.000500e-09
```

=> The worst case delay is 0.711 ns.

=> The setup time for post layout D flip flop is 0.0304 ns

$T_{clk} \geq 0.711 + 0.0304$

$T_{clk} \geq 0.7414$ ns.

$f_{clk} \leq 1.348$ GHz

	Pre Layout	Post Layout
worst case delay	0.544 ns	0.711 ns
Tclk	0.588 ns	0.741 ns
clk speed	1.71 GHz	1.38 GHz

(11)

Verilog file :-

```
module CLA_5bit(
  input [4:0] A,
  input [4:0] B,
  input Cin,
  output [4:0] S,
  output Cout
);
  wire [4:0] G, P;
  wire c1, c2, c3, c4;


  assign G = A & B;
  assign P = A ^ B;


  assign c1 = G[0] | (P[0] & Cin);

  assign c2 = G[1] | (P[1] & G[0]) | (P[1] & P[0] & Cin);

  assign c3 = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2] & P[1] & P[0] & Cin);

  assign c4 = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0]) | (P[3] & P[2] & P[1] & P[0] & Cin);

  assign Cout = G[4] | (P[4] & G[3]) | (P[4] & P[3] & G[2]) | (P[4] & P[3] & P[2] & G[1]) | (P[4] & P[3] & P[2] & P[1] & G[0]) | (P[4] & P[3] & P[2] & P[1] & P[0] & Cin);

  assign S[0] = P[0] ^ Cin;
  assign S[1] = P[1] ^ c1;
  assign S[2] = P[2] ^ c2;
  assign S[3] = P[3] ^ c3;
  assign S[4] = P[4] ^ c4;

endmodule
```

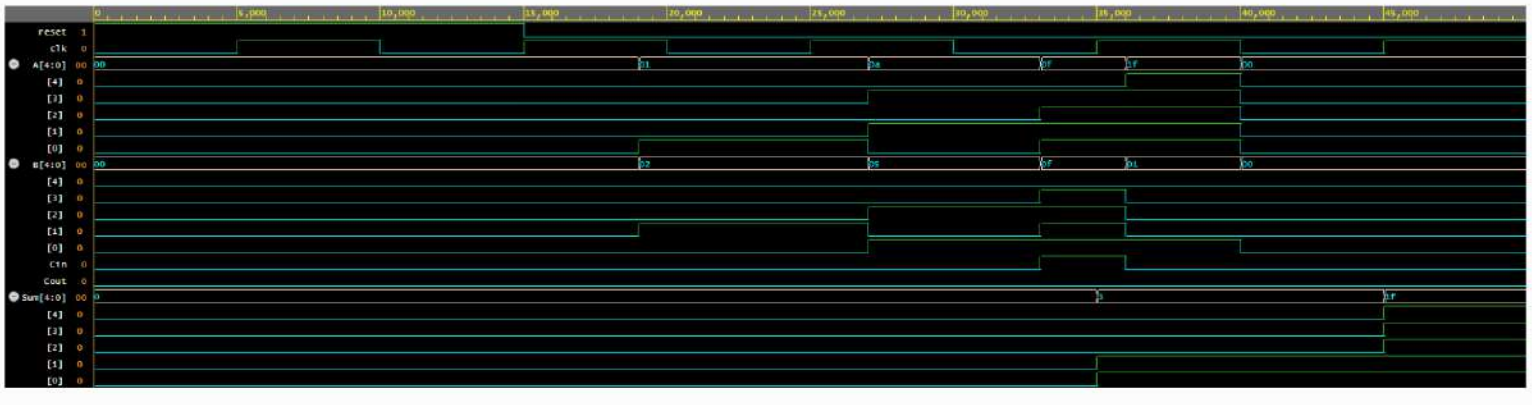
```
module D_FF_5bit(
  input [4:0] D,
  input clk,
  input reset,
  output reg [4:0] Q
);
  always @(posedge clk or posedge reset) begin
    if (reset)
      Q <= 5'b00000;
    else
      Q <= D;
  end
endmodule
```

```
`include "D_FF_5bit.v"
`include "CLA_5bit.v"

module DFF_CLA_5bit(
  input [4:0] A,
  input [4:0] B,
  input Cin,
  input clk,
  input reset,
  output [4:0] Sum,
  output Cout
);

  wire [4:0] A_reg, B_reg;
  reg Cin_reg;

  wire [4:0] S_comb;
  wire Cout_comb;

  reg Cout_reg;

  D_FF_5bit input_reg_A (
    .D(A),
    .clk(clk),
    .reset(reset),
    .Q(A_reg)
  );

  D_FF_5bit input_reg_B (
    .D(B),
    .clk(clk),
    .reset(reset),
    .Q(B_reg)
  );
```

```
  always @(posedge clk or posedge reset) begin
    if (reset)
      Cin_reg <= 1'b0;
    else
      Cin_reg <= Cin;
  end

  CLA_5bit adder_inst (
    .A(A_reg),
    .B(B_reg),
    .Cin(Cin_reg),
    .S(S_comb),
    .Cout(Cout_comb)
  );

  D_FF_5bit output_reg_S (
    .D(S_comb),
    .clk(clk),
    .reset(reset),
    .Q(Sum)
  );

  always @(posedge clk or posedge reset) begin
    if (reset)
      Cout_reg <= 1'b0;
    else
      Cout_reg <= Cout_comb;
  end

  assign Cout = Cout_reg;

endmodule
```

Test Bench :-

```
`timescale 1ns / 1ps
module DFF_CLA_5bit_tb;
  reg [4:0] A;
  reg [4:0] B;
  reg Cin;
  reg clk;
  reg reset;

  wire [4:0] Sum;
  wire Cout;

  DFF_CLA_5bit uut (
    .A(A),
    .B(B),
    .Cin(Cin),
    .clk(clk),
    .reset(reset),
    .Sum(Sum),
    .Cout(Cout)
  );

  always #5 clk = ~clk;

  initial begin
    $dumpfile("pipeline_wave.vcd");
    $dumpvars(0, DFF_CLA_5bit_tb);

    clk = 0;
    reset = 1;
    A = 0;
    B = 0;
    Cin = 0;
    #15;
    reset = 0;
    #4 A = 5'd1; B = 5'd2; Cin = 0;
    #8 A = 5'd10; B = 5'd5; Cin = 0;
    #6 A = 5'd15; B = 5'd15; Cin = 1;
    #3 A = 5'd31; B = 5'd1; Cin = 0;
    #4 A = 0; B = 0; Cin = 0;
    #10 $finish;
  end
endmodule
```

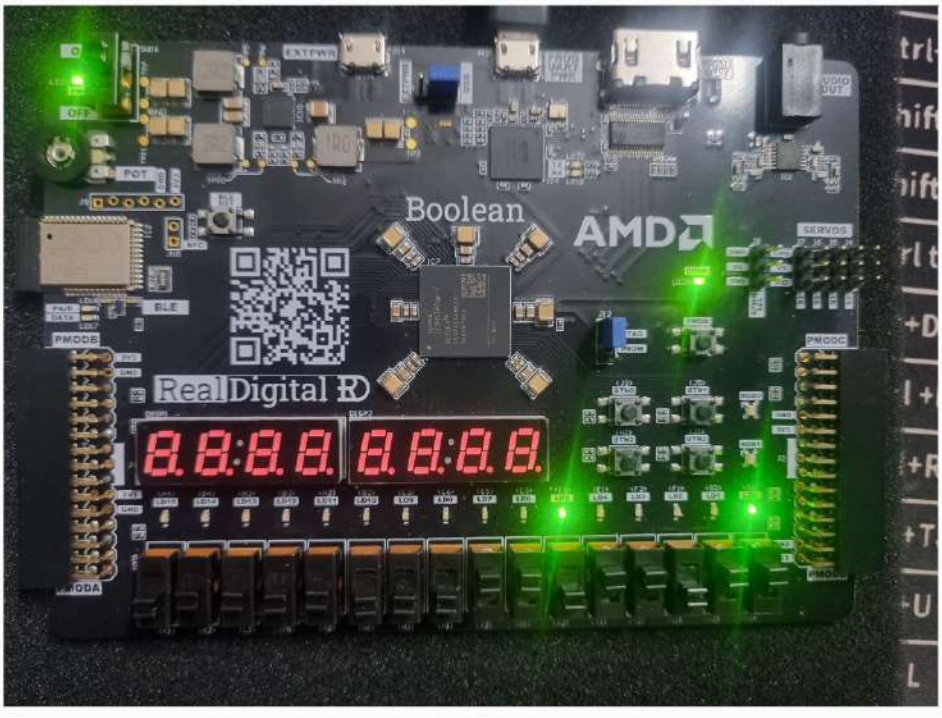


Q12

(d) Test Signals for FPGA

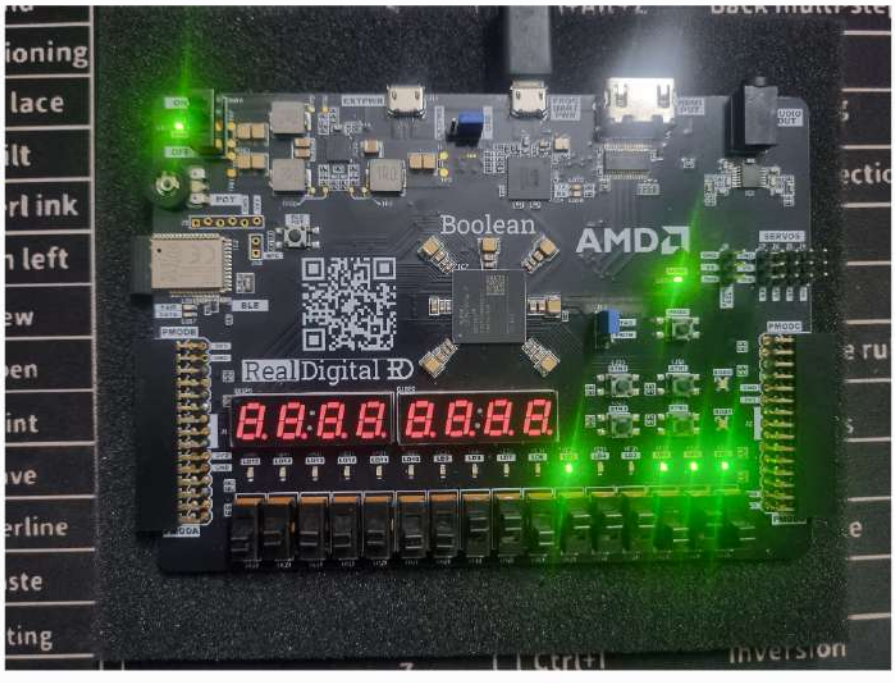
(1)

```
  1 1 1
  1 1 0 1 1
  0 0 1 1 0
-------------
1 0 0 0 0 1
```



(2)

```
    1
  1 1 0 1 0
  0 1 1 0 1
-------------
1 0 0 1 1 1
```



③

```
  1111
  10101
  01010
      1
 ------
 100000
```